18-Line Plug and Play SCSI Terminator

The 18-channel IMP5226 SCSI terminator is part of IMP's family of high-performance SCSI terminators that deliver true UltraSCSI performance. The BiCMOS design offers superior performance over first generation linear regulator / resistor based terminators.

IMP's new architecture employs high-speed adaptive elements for each channel, thereby providing the fastest response possible - typically 35MHz, which is 100 times faster than the older linear regulator terminator approach. The bandwidth of terminators based on the older regulator / resistor terminator architecture is limited to 500kHz since a large output stabilization capacitor is required.

The IMP architecture eliminates the external output compensation capacitor and the need for transient output capacitors while maintaining pin compatibility with first generation designs. Reduced component count is inherent with the IMP5226.

The IMP5226 architecture tolerates marginal system designs. A key improvement offered by the IMP5226 lies in its ability to insure reliable, error-free communications even in systems which do not adhere to recommended SCSI hardware design guidelines, such as improper cable lengths and impedance. Frequently, this situation is not controlled by the peripheral or host designer.

The IMP5226 can be placed in a sleep mode with a high logic signal. In the sleep mode the outputs are in a high impedance state. Quiescent current is less than 150µA when disabled.

The IMP5226 is a superior pin-for-pin replacement for the LX5226, LX5207, UC5601 / 5602 and the UCC5610.

Key Features

- Ultra-Fast response for Fast-20 SCSI
- 35MHz channel bandwidth
- Sleep-mode current less than 150µA — Disconnects terminator from lows
- NO external compensation capacitors
- Compatible with active negation drivers
- Compatible with passive and active terminations
- Approved for use with SCSI 1, 2, 3 and Ultra SCSI
- Hot-swap compatible
- Pin-for-pin compatible with LX5226, LX5207 and UCC5610

IMP SCSI Terminators

Part	Channels	Type
IMP5111	9	SE
IMP5112	9	SE
IMP5115	9	SE
IMP5121	27	SE
IMP5218	9	SE
IMP5219	9	SE
IMP5225	18	SE
IMP5226	18	SE
IMP5241	8	SE/LVD
IMP5242	8	SE/LVD

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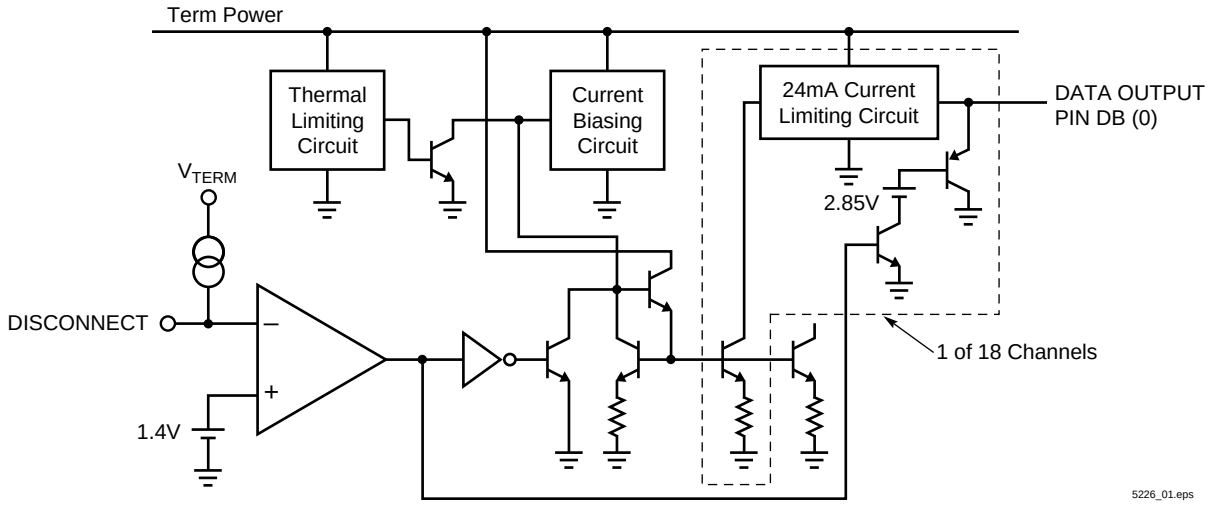
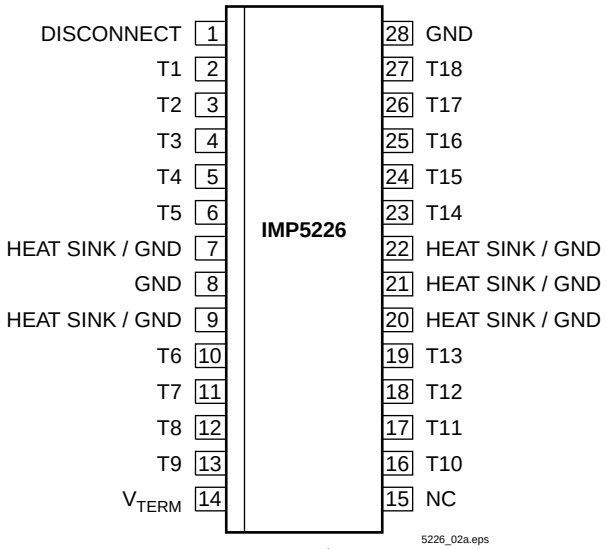
Block Diagrams



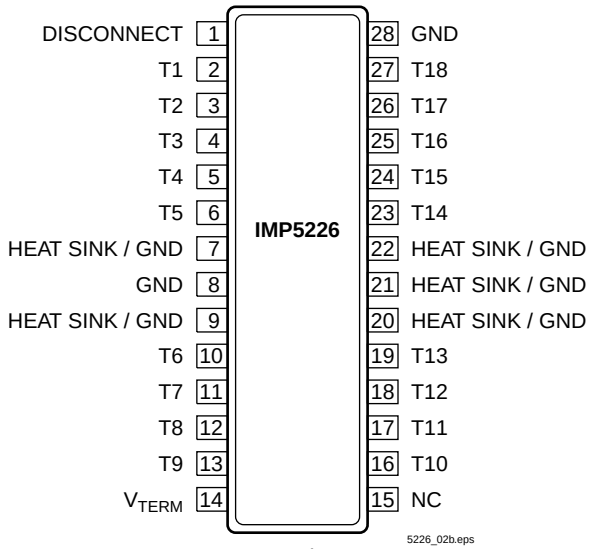
Pin Configuration

SOWB-28



DWP Package

SSOP-28



DB Package

Ordering Information

Part Number	Temperature Range	Package
IMP5226CDWP	0°C to 70°C	28-pin Plastic SOWB
IMP5226CDWPT	0°C to 70°C	Tape and Reel, 28-pin Plastic SOWB
IMP5226CDB	0°C to 70°C	28-pin Plastic SSOP
IMP5226CDBT	0°C to 70°C	Tape and Reel, 28-pin Plastic SSOP

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Absolute Maximum Ratings[1]

TermPwr Voltage . . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Operating Junction Temperature . . . . . 150°C
Storage Temperature Range . . . . . –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

Note: 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

Thermal Data

DWP Package
Thermal Resistance Junction-to-Leads, θ_{JL} . . . . . 18°C / W
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 40°C / W
DB Package
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 117°C / W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device / pc-board system. All of the ambient airflow is assumed.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Termpwr Voltage	V_{TERM}	4.0		5.5	V
Signal Line Voltage		0		5.0	V
Disconnect Input Voltage		0		V_{TERM}	V
Operating Junction Temperature Range – IMP5226C		0		125	°C

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Note: 2. Recommended operating conditions indicate the range over which the device is functional.

Electrical Characteristics

Unless otherwise specified, these specifications apply at an ambient operating temperature of T_A = 25°C. TermPwr = 4.75V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage	V_{OUT}		2.65	2.85		V
TermPwr Supply Current	I_{CC}	All data lines = Open		10	15	mA
		All data lines = 0.2V		424	450	
		DISCONNECT Pins > 2.0V		50	150	µA
Output Current	I_{OUT}	V_{OUT} = 0.5V	–20	–22	–24	mA
Disconnect Input Current	I_{IN}	DISCONNECT Pins = 0V			–10	µA
Output Leakage Current	I_{OL}	DISCONNECT Pins > 2.0V, V_O = 0.2V			1	µA
Channel Bandwidth	BW			35		MHz
Termination Sink Current, per Channel	I_{SINK}	V_{OUT} = 4V	7			mA

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Application Information

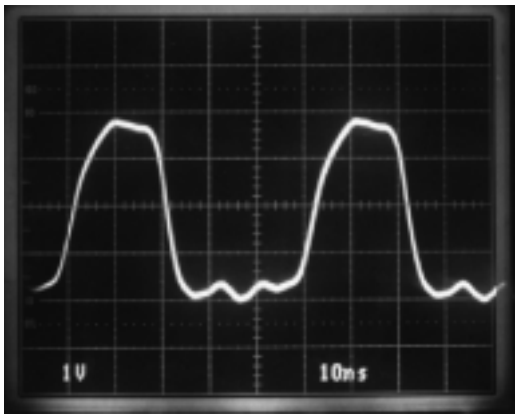

Figure 1. Receiving Waveform – 20MHz

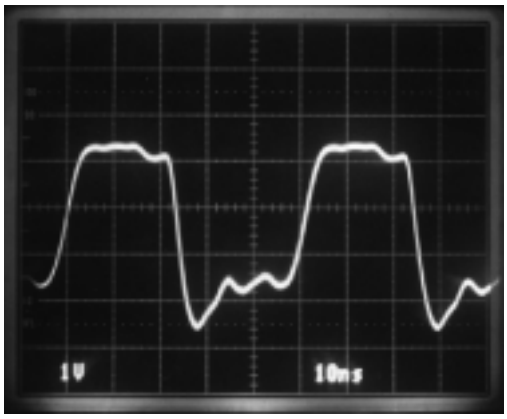

Figure 2. Driving Waveform – 20MHz

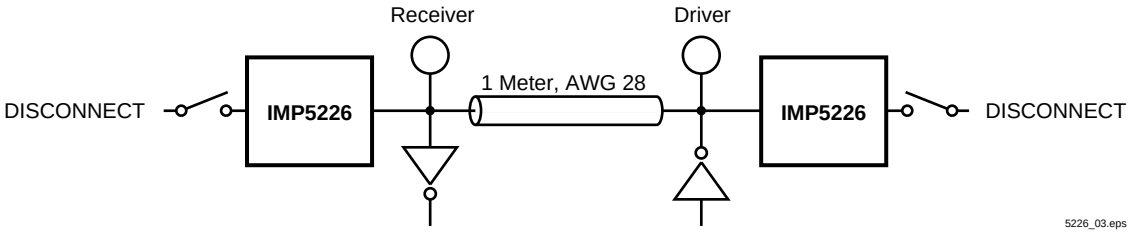

Figure 3.

Cable transmission theory suggests to optimize signal speed and quality, the termination should act both as an ideal voltage reference when the line is released (deasserted) and as an ideal current source when the line is active (asserted). Common active terminators which consist of linear regulators in series with resistors (typically 110Ω) are a compromise. With coventional linear terminators as the line voltage increases the amount of current decreases linearly by the equation;

$$\frac{(V_{REF} - V_{LINE})}{R} = I.$$

The IMP5226, with its unique new architecture, applies the maximum amount of current regardless of line voltage until the termination high threshold (2.85V) is reached.

Table 1. Power Up/ Power Down Function Table

DISCONNECT	Outputs	Maximum Quiescent Current
L	Enabled	15mA
H	HI Z	150µA
Open	HI Z	150µA

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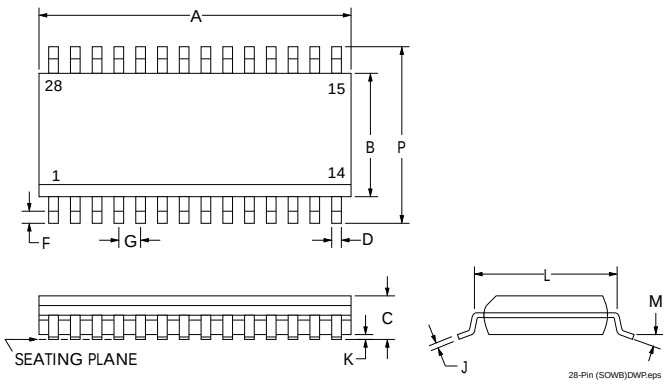
Acting as a near ideal line terminator, the IMP5226 closely reproduces the optimum case when the device is enabled. To enable the device the disconnect pin is pulled LOW. During this mode of operation, quiescent current is 10mA, and the device will respond to line demands by delivering 24mA on assertion and by imposing 2.85V on deassertion.

In order to disable the device, the disconnect pin must be driven HIGH In the disable mode, the device is in a sleep state with quiescent current less than 150µA. When disabled, all outputs are in a high impedance state. Sleep mode can be used for power conservation or to remove the terminator from the SCSI chain.

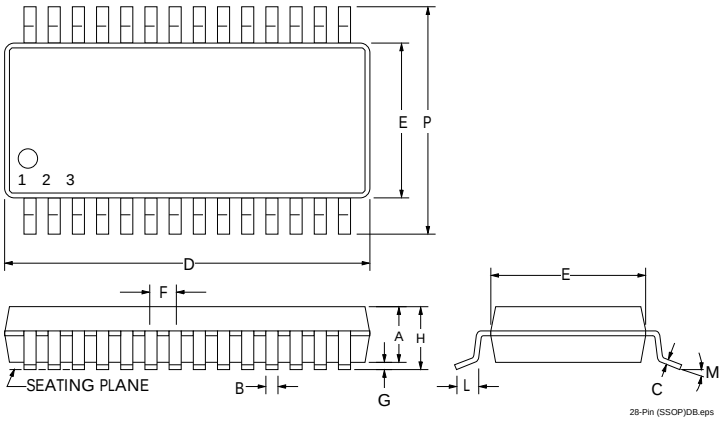
An additional feature of the IMP5226 is its compatibility with active negation drivers.

Package Dimensions

SOWB (28-Pin)



SSOP (28-Pin)



	Inches		Millimeters	
	Min	Max	Min	Max
SOWB (28-Pin)*				
A	0.698	0.713	17.70	18.10
B	0.291	0.299	7.40	7.60
C	0.093	0.104	2.35	2.65
D	0.013	0.018	0.33	0.51
F	0.016	0.050	0.40	1.27
G	0.050 BSC		1.27 BSC	
J	0.009	0.013	0.23	0.32
K	0.004	0.012	0.10	0.30
M	0°	8°	0°	8°
P	0.394	0.419	10.00	10.65
SSOP (28-Pin)				
A	0.068	0.078	1.73	1.99
B	0.009	0.015	0.25	0.38
C	0.005	0.008	0.13	0.22
D	0.396	0.407	10.07	10.33
F	0.205	0.212	5.20	5.38
G	0.25 BSC		0.65 BSC	
J	0.002	0.008	0.05	0.21
K	0.064	0.072	1.63	1.83
L	0.025	0.037	0.65	0.95
M	0°	8°	0°	8°
P	0.301	0.311	7.65	7.90

5226_t05.at3

** JEDEC Drawing MO-013AE*

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