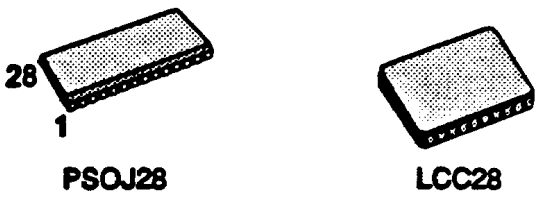
SGS-THOMSON MICROELECTRONICS

IMS 1824

APR 22 19

64KX4 CMOS SRAM with Output Enable

- VERY HIGH SPEED DOUBLE METAL CMOS SRAM
- ADVANCED PROCESS- 1.2 MICRON DESIGN RULES
- 64K×4 BIT ORGANISATION
- 25, 30, 35 AND 45ns ADDRESS ACCESS TIMES
- 25, 30, 35 AND 45ns CHIP ENABLE ACCESS TIMES
- FULLY TTL COMPATIBLE
- THREE STATE OUTPUT
- COMMON DATA INPUTS AND OUTPUTS
- SINGLE +5V ±10% OPERATION
- PACKAGES INCLUDE: 28 PIN SOJ AND 28 PIN LCC
- POWER DOWN FUNCTION



PSOJ28 LCC28

(Ordering information at the end of the datasheet)

DESCRIPTION

The IMS 1824 is a high performance 64K×4 CMOS Static RAM. The IMS 1824 provides maximum density and speed enhancements with the additional benefits of lower power and superior reliability.

The IMS 1824 features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. The IMS 1824 provides a Chip Enable function ($\overline{E}$) that can be used to place the device into a low-power standby mode. The IMS 1824 also includes an Output Enable ($\overline{G}$) for fast access to data and enhanced bus contention control.

PIN NAMES

A_0–A_{15}	Address Inputs
$\overline{W}$	Write Enable
I/O_1–I/O_4	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
VCC	Power (+5V)
VSS	Ground

Figure 1. Pin configuration and logic symbol

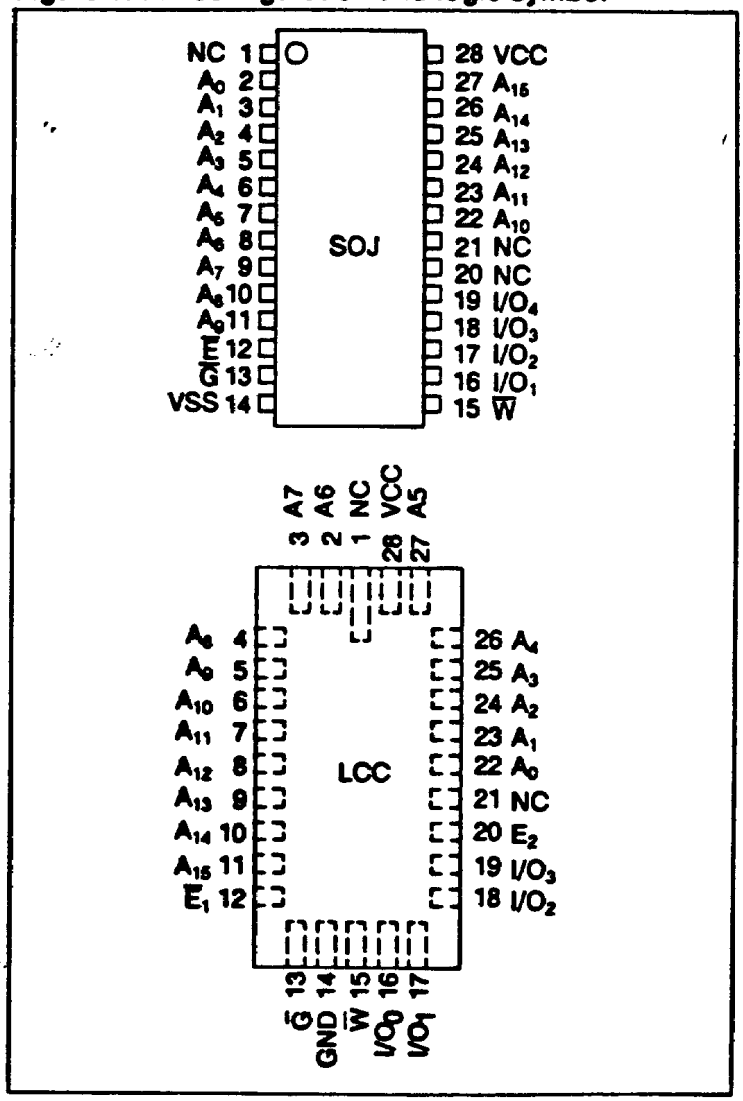
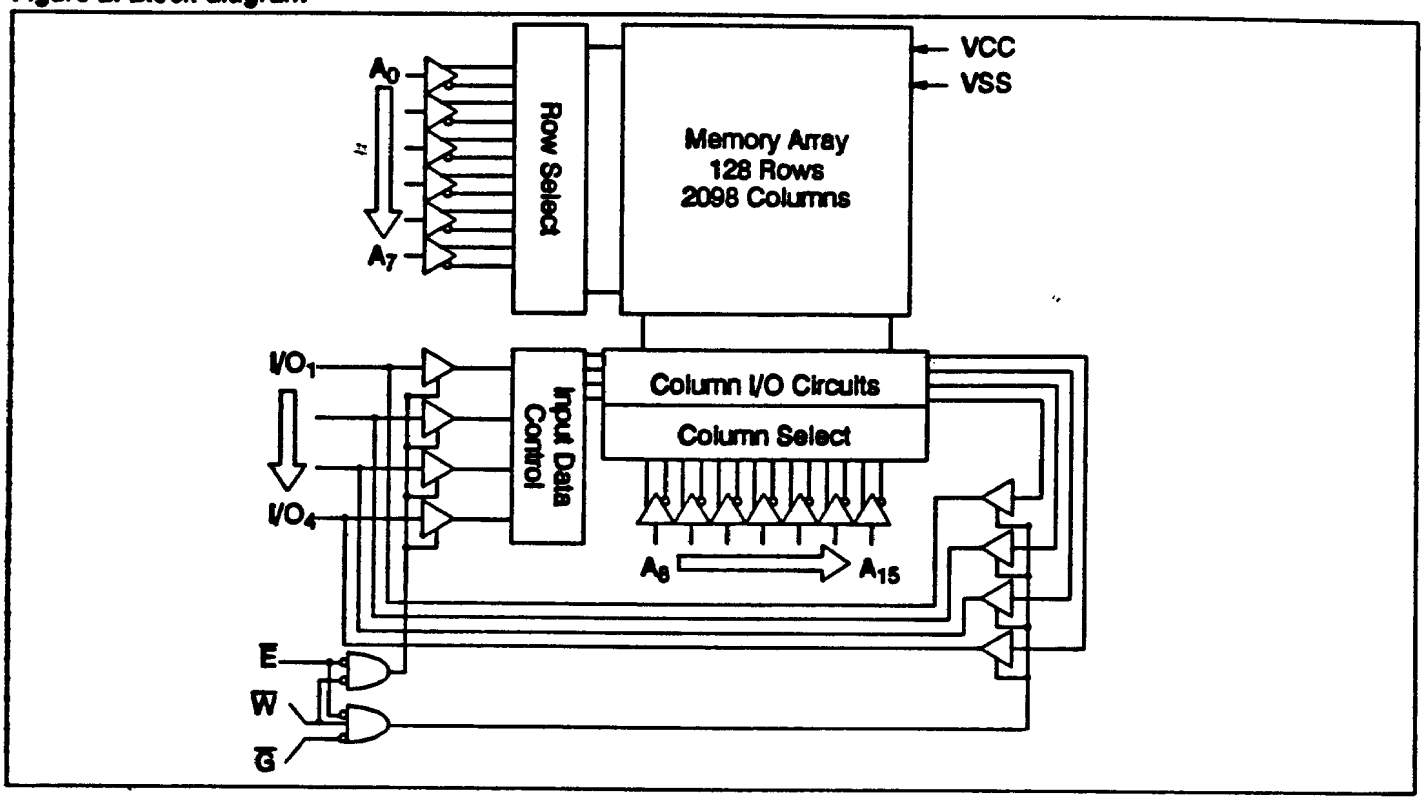


Figure 2. Block diagram

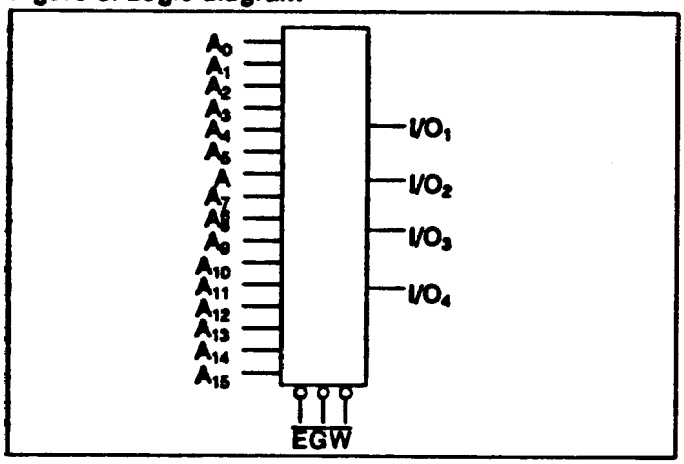


ABSOLUTE MAXIMUM RATINGS*

Parameter	Value		Unit
	Min	Max	
VCC with respect to VSS	-2.0	7.0	V
Voltage on any pin with respect to VSS	-1.0	VCC+0.5	V
Temperature under bias (TA)	-55	125	°C
Storage temperature	-65	150	°C
Power dissipation		1	W
DC output current		25	mA

*Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Figure 3. Logic diagram



TRUTH TABLE

Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	I/O
Standby (Isb)	H	X	X	HI-Z
Output disable	L	H	H	HI-Z
Read	L	H	L	DOUT
Write	L	L	X	DIN

DEVICE OPERATION

The IMS 1824 has three control inputs, Chip Enable ($\overline{E}$), Output Enable ($\overline{G}$) and Write Enable ($\overline{W}$) . There are also 16 address inputs (A_0-A_{15}) and 4 Data I/O lines. The Enable inputs control device selection as well as active and standby modes. The $\overline{W}$ input controls the mode of operation (Read or Write).

With $\overline{E}$ low, the device is selected and the 16 address inputs are decoded to select one 4 bit word out of 64K words. Read and Write operations on the memory cells are controlled by the $\overline{W}$ and $\overline{G}$ inputs. With $\overline{E}$ high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-third of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq$ VIH min with $\overline{E}$ and $\overline{G} \leq$ VIL max. Read access time is measured from the latter of $\overline{E}$ or $\overline{G}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ and $\overline{G}$ are low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and as long as $\overline{E}$ and $\overline{G}$ remain low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by the latter of $\overline{E}$ or $\overline{G}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

Since $\overline{G}$ controls the output buffers, $\overline{G}$ is required to be low in order for the outputs to be active.

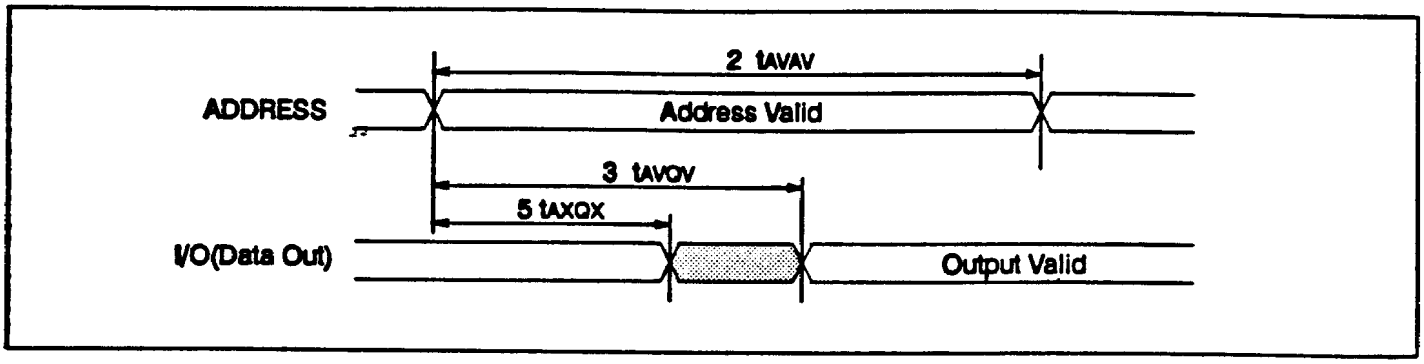
READ CYCLE AC OPERATING CONDITIONS ($0°C \leq TA \leq 70°C$)($VCC = 5.0V \pm 10\%$)[7]

No	Symbol		Parameter	IMS 1824-25		IMS 1824-30		IMS 1824-35		IMS 1824-45		Unit	Note
	Stand	Alt		min	max	min	max	min	max	min	max		
1	tELQV	tACS	Chip Enable Access Time		25		30		35		45	ns	
2	tAVAV	tRC	Read Cycle Time	25		30		35		45		ns	1
3	tAVQV	tAA	Address Access Time		25		30		35		45	ns	2
4	tGLQV	tOE	Output Enable Access Time		15		15		20		20	ns	
5	tAXQX	tOH	O/P Hold After Add's Change	3		3		3		3		ns	
6	tELQX	tLZ	Chip Enable to O/P Active	3		3		3		3		ns	3
7	tGLQX	tOLZ	Output Enable to O/P Active	0		0		0		0		ns	3
8	tEHQZ	tHZ	Chip Disable to O/P inactive	0	12	0	15	0	15	0	20	ns	4, 5
9	tGHQZ	tOHZ	Output Disable to O/P inactive	0	12	0	15	0	15	0	20	ns	4, 5
10	tELICCH	tPU	Chip Enable to Power Up	0		0		0		0		ns	5
11	tEHICCL	tPD	Chip Disable to Power Down		30		30		30		30	ns	5
		tT	Input rise and fall times		50		50		50		50	ns	5, 6

NOTES

1 For Read Cycle 1 and 2, $\overline{W}$ is high for entire cycle.
2 Device is continually selected, $\overline{E}$ low.
3 tELQX is always greater than tEHQZ
4 Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
5 Parameter guaranteed but not tested.
6 Measured between VIL max. and VIH min.
7 $\overline{E}$ and $\overline{W}$ must transition between VIH to VIL or VIL to VIH in a monotonic fashion.
8 Device is continually selected, $\overline{E}$ low.

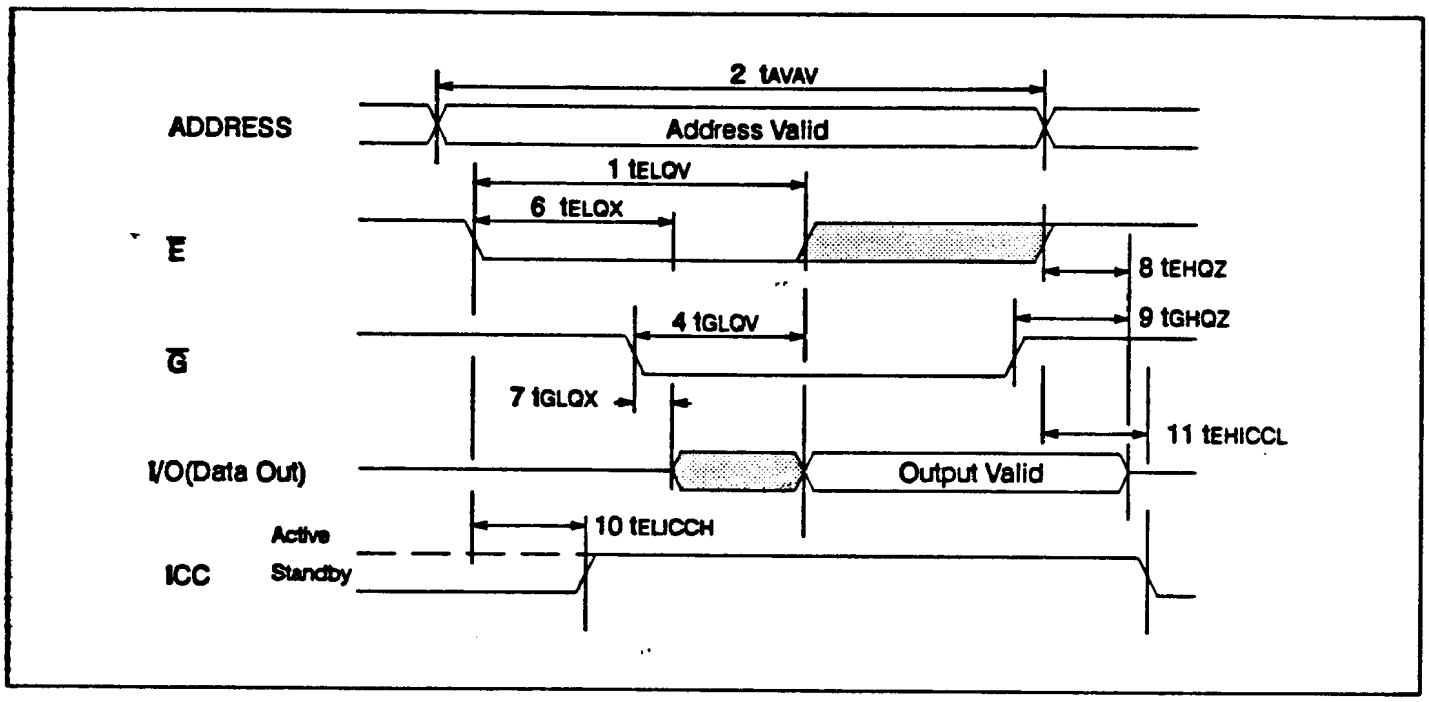
Figure 4. Read cycle1[1,2]



NOTES

1 For Read Cycle 1, $\overline{W}$ is high for entire cycle.

Figure 5. Read cycle2[1]



NOTES

1 For Read Cycle 2, $\overline{W}$ is high for entire cycle.

WRITE CYCLE

The write cycle of the IMS 1824 is initiated by the later of $\overline{E}$ or $\overline{W}$ to transition from a high to a low. In the case of $\overline{W}$ falling last, the output buffer will be turned on tELQX after the falling edge of $\overline{E}$ or $\overline{G}$ (just as in a read cycle). The output buffer is then turned off within twLQZ of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common input/output connections. Therefore input data should not be active until twLQZ. To avoid bus contention, the $\overline{G}$ input can be held high throughout the write operation.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active (if $\overline{G}$ is low). The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high the output remains in the high impedance state.

No	Symbol Stand	Symbol Alt	Parameter	IMS 1824-25 min	IMS 1824-25 max	IMS 1824-30 min	IMS 1824-30 max	IMS 1824-35 min	IMS 1824-35 max	IMS 1824-45 min	IMS 1824-45 max	Unit	Note
12	tAVAV	tWC	Write Cycle Time	25		30		35		45		ns	
13	tWLWH	tWP	Write Pulse Width	20		25		30		40		ns	
14	tELWH	tCW	Chip Enable to End of Write	20		25		30		40		ns	
15	tDVWH	tDW	Data Setup to End of Write	12		12		15		20		ns	
16	tWHDX	tDH	Data Hold after End of Write	0		0		0		0		ns	
17	tAVWH	tAW	Address Setup to End of Write	20		25		30		40		ns	
18	tAVWL	tAS	Address Setup to Start of Write	0		0		0		0		ns	
19	tWHAX	tWR	Address Hold After End of Write	2		2		0		0		ns	
20	tWLQZ	tWZ	Write Enable to Output Disable	0	10	0	15	0	15	0	20	ns	3, 4
21	tWHQX	tOW	Output Active After End of Write	5		5		5		5		ns	5

NOTES

1 $\overline{E}$ and $\overline{W}$ must transition between VIH to VIL or VIL to VIH in a monotonic fashion.

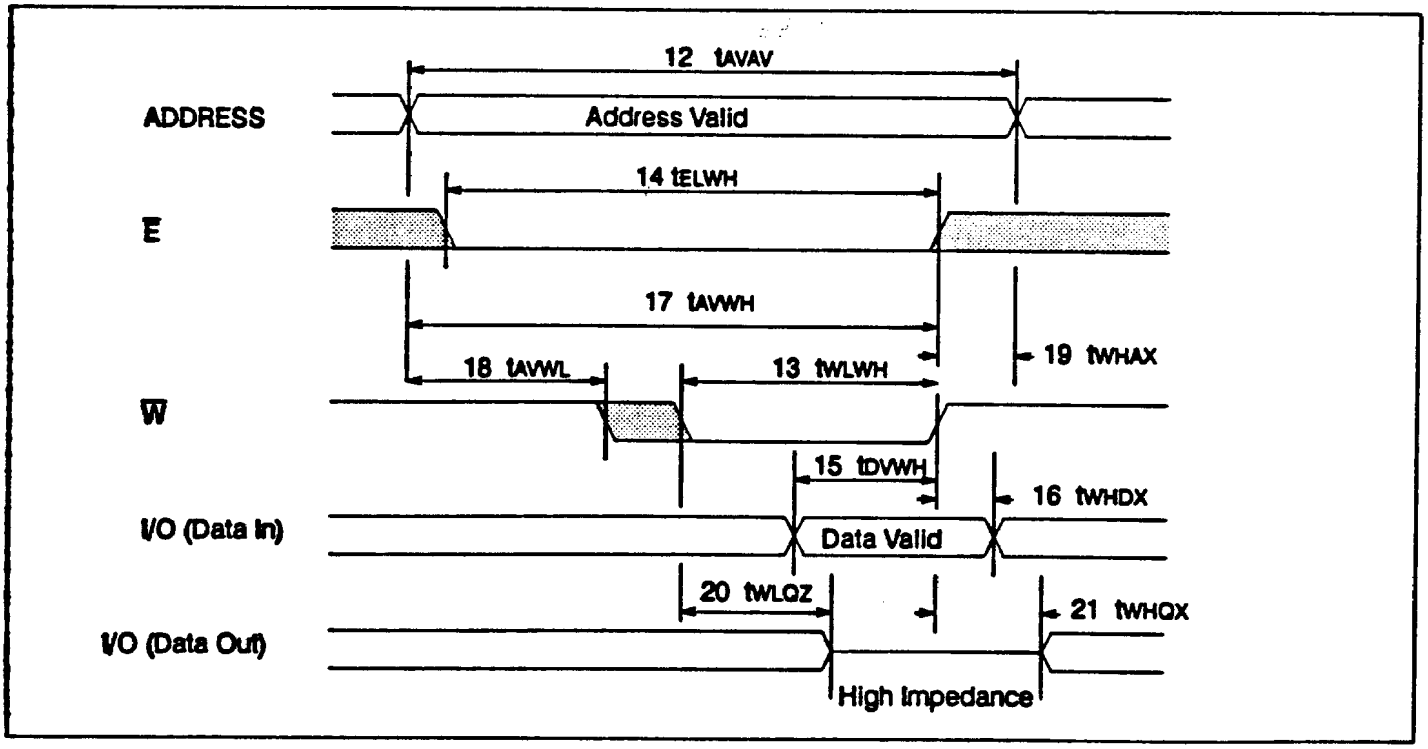
2 $\overline{E}$ or $\overline{W}$ must be $\geq$ VIH during address transitions.

3 Measured $\pm$200mV from steady state output voltage. Load capacitance is 5pF.

4 Parameter guaranteed but not tested.

5 If $\overline{W}$ is low when the later of $\overline{E}$ goes low, the outputs remain in the high impedance state.

Figure 6. Write cycle 1



WRITE CYCLE 2 AC OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C)(VCC = 5.0V ± 10%)[1,2]

No	Symbol Stand	Symbol Alt	Parameter	IMS 1824-25 min	IMS 1824-25 max	IMS 1824-30 min	IMS 1824-30 max	IMS 1824-35 min	IMS 1824-35 max	IMS 1824-45 min	IMS 1824-45 max	Unit	Note
22	tAVAV	tWC	Write Cycle Time	25		30		35		45		ns	
23	tWLEH	tWP	Write Pulse Width	20		25		30		40		ns	
24	tELEH	tCW	Chip Enable to End of Write	20		25		30		40		ns	
25	tDVEH	tDW	Data Setup to End of Write	12		12		15		20		ns	
26	tEHDX	tDH	Data Hold after End of Write	0		0		0		0		ns	
27	tAVEH	tAW	Address Setup to End of Write	20		25		30		40		ns	
28	tEHAX	tWR	Address Hold After End of Write	0		0		0		0		ns	
29	tAVEL	tAS	Address Setup to Start of Write	2		2		0		0		ns	
30	tWLQZ	tWZ	Write Enable to Output Disable	0	10	0	15	0	15	0	20	ns	3, 4

NOTES

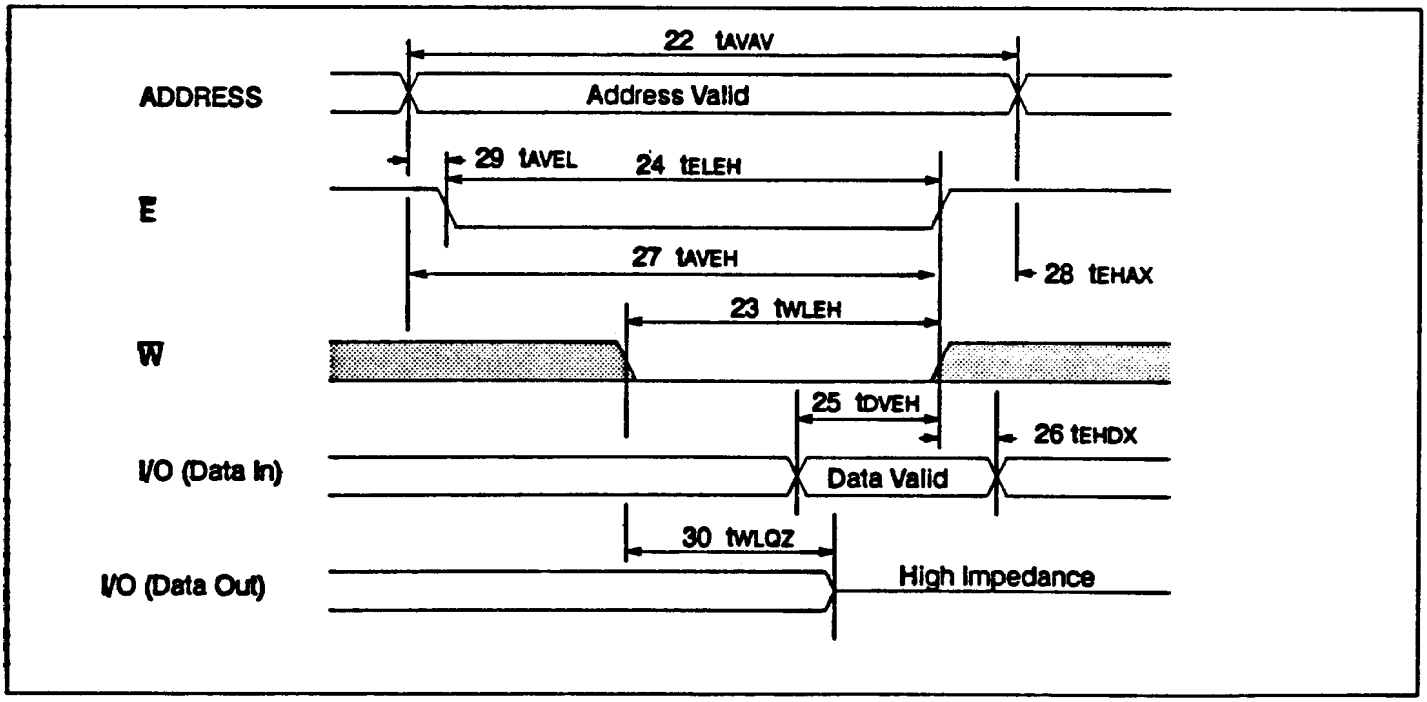
1 $\overline{E}$ and $\overline{W}$ must transition between VIH to VIL or VIL to VIH in a monotonic fashion.

2 $\overline{E}$ or $\overline{W}$ must be ≥ VIH during address transitions.

3 Measured ±200mV from steady state output voltage. Load capacitance is 5pF.

4 Parameter guaranteed but not tested.

Figure 7. Write cycle 2



DC OPERATING CONDITIONS

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
VCC	Supply Voltage	4.5	5.0	5.5	V	
VSS	Supply Voltage	0	0	0	V	
VIH	Input Logic '1' Voltage	2.0		VCC+0.5	V	1
VIL	Input Logic '0' Voltage	-0.5		0.8	V	1, 2
TA	Ambient Operating Temperature	0		70	°C	3

NOTES
1 All inputs.
2 VIL min = -3.0V for pulse width <20ns.(Sampled and not 100% tested)
3 400 linear ft/min air flow.

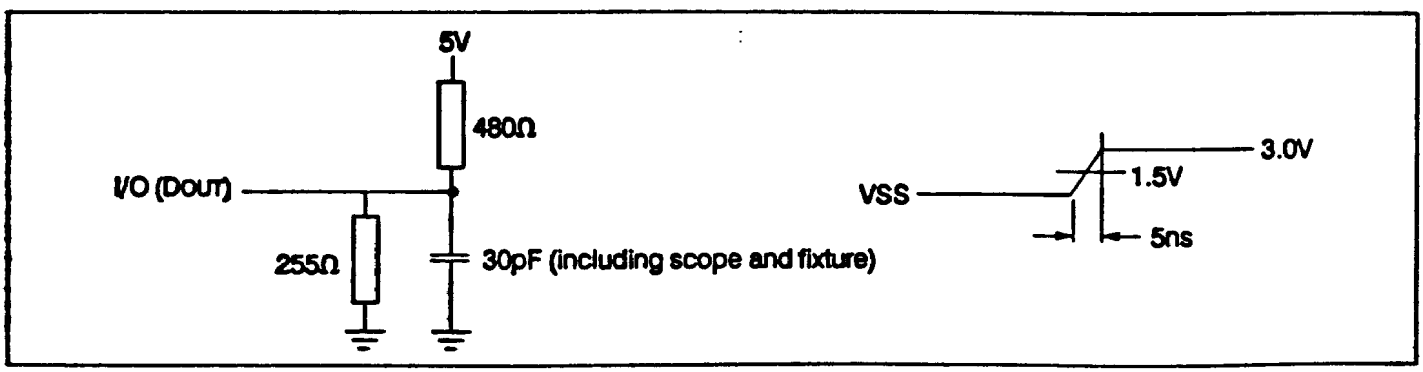
DC ELECTRICAL CHARACTERISTICS (0°C ≤ TA ≤ 70°C)(VCC = 5.0V ± 10%)[1]

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
ICC1	Average VCC Power Supply Current		120	mA	2
ICC2	VCC Power Supply Current (Standby, Stable TTL Input Levels)		30	mA	3
ICC3	VCC Power Supply Current (Standby, Stable CMOS Input Levels)		10	mA	4
ICC4	VCC Power Supply Current (Standby, Cycling CMOS Input Levels)		15	mA	5
IILK	Input Leakage Current (any input)		±1	µA	6
IOLK	Off State Output Leakage Current		±10	µA	6
VOH	Output Logic '1' Voltage	2.4		V	7
VOL	Output Logic '0' Voltage		0.4	V	8

NOTES
1 ICC is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.
2 tAVAV = tAVAV(min).
3 E ≥ VIH. All other inputs at VIN ≤ VIL or ≥ VIH.
4 E ≥ (VCC -0.2V). All other inputs at VIN ≤ 0.2 or ≥ (VCC -0.2V).
5 E ≥ (VCC -0.2V). Inputs cycling at VIN ≤ 0.2 or ≥ (VCC -0.2V).
6 VCC = max. VIN = VSS to VCC.
7 IOH = -4mA.
8 IOL = 8mA.

AC TEST CONDITION

Figure 8. Output load and AC test condition



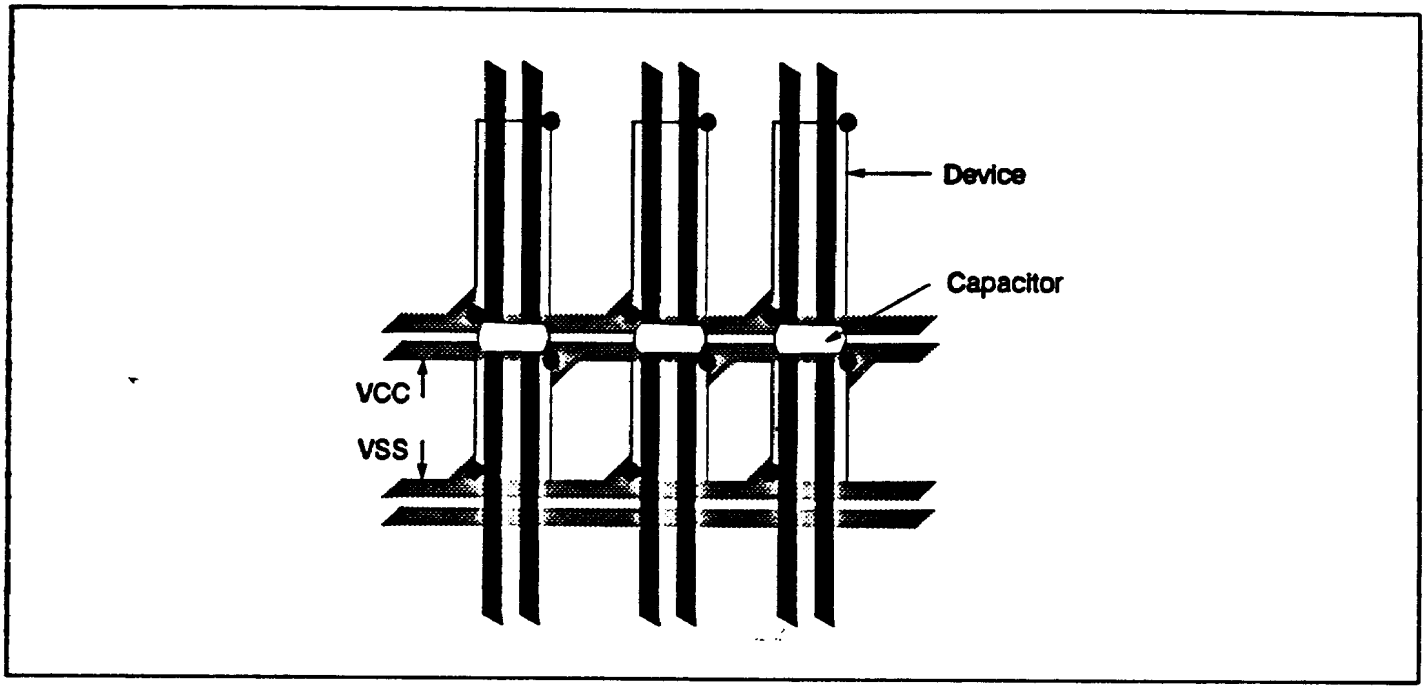
CAPACITANCE (TA = 25°C, F = 1.0MHZ)

Symbol	Parameter	Value		Unit	Conditions
		Min	Max		
CIN	Input Capacitance		4	pF	ΔV = 0 to 3V
COUT	Output Capacitance		4	pF	ΔV = 0 to 3V

NOTES

1 These parameters are sampled not 100% tested.

Figure 9. Grid showing decoupling capacitors



Pin-outs and packages

Figure 10. 28 pin plastic J-leaded small outline package dimensions

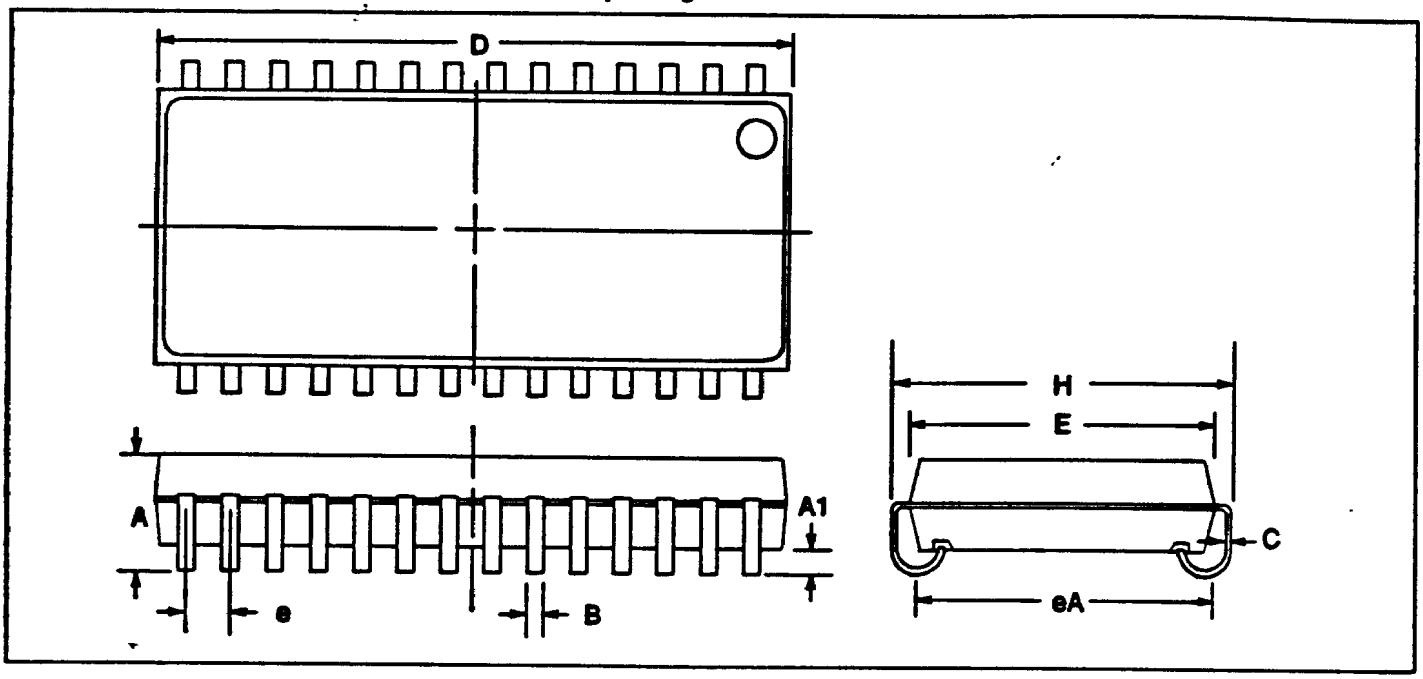


Table 1. 28 pin plastic J-leaded small outline package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	3.556	4.064	0.140	0.160	
B1	0.356	0.483	0.014	0.019	
C	0.203	0.305	0.008	0.012	
D	17.805	18.060	0.701	0.711	
E	8.509	8.814	0.335	0.347	
E1	7.417	7.595	0.292	0.299	
e1	1.270		0.050		Typical
eA	6.650	6.910	0.262	0.272	
L	0.711	0.914	0.028	0.036	

Figure 11. 28 pin leadless chip carrier package dimensions

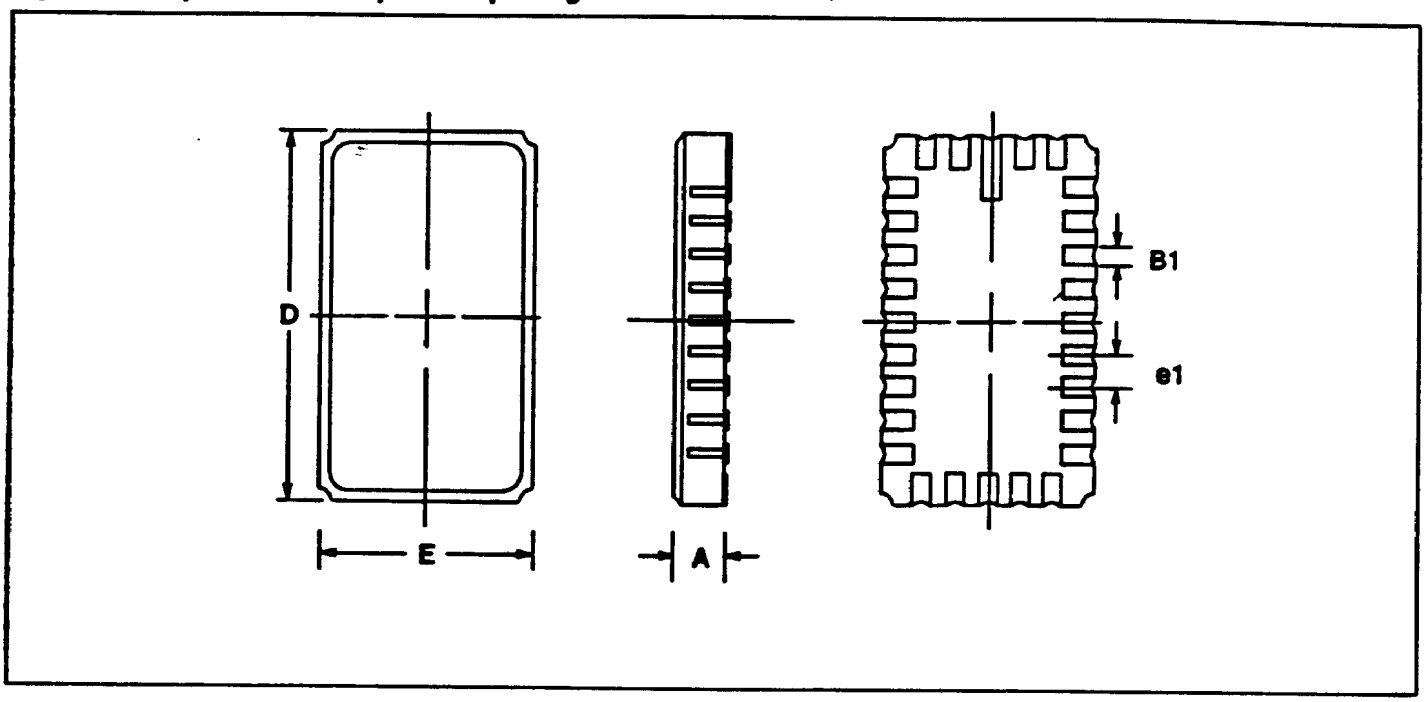


Table 2. 28 pin leadless chip carrier package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	1.625	1.981	0.064	0.078	
B1	0.559	0.711	0.022	0.028	
D	13.716	14.224	0.540	0.560	
E	8.636	9.144	0.340	0.360	
e1	1.219	1.321	0.048	0.052	

ORDERING INFORMATION

Device	Speed	Package	Part Number
IMS 1824	25ns	Plastic SOJ	IMS1824E-25
IMS 1824	30ns	Plastic SOJ	IMS1824E-30
IMS 1824	35ns	Plastic SOJ	IMS1824E-35
IMS 1824	45ns	Plastic SOJ	IMS1824E-45
IMS 1824	25ns	Ceramic LCC	IMS1824N-25
IMS 1824	30ns	Ceramic LCC	IMS1824N-30
IMS 1824	35ns	Ceramic LCC	IMS1824N-35
IMS 1824	45ns	Ceramic LCC	IMS1824N-45