IMS2600M

High Performance 64Kx1 Dynamic RAM MIL-STD-883C

FEATURES

- Full Military DRAM Temperature Operating Range (-55°C to +110°C)
- MIL-STD-883C Processing
- 100, 120 and 150nsec $\overline{RAS}$ Access Times
- Cycle Times of 160, 190 and 230ns
- Low Power:
  - 28mW Standby
  - 358mW Active (350ns Cycle Time)
  - 468mW Active (160ns Cycle Time)
- On-Chip Refresh using $\overline{CAS}$-before-$\overline{RAS}$
- 4ms / 256 Cycle Refresh, Pin 1 left as N/C for 256K expansion
- $\overline{RAS}$-Only Refresh Capability
- D_{OUT} Hold under $\overline{CAS}$ control
- JEDEC Standard 16-pin Configuration
- Read, Write Read-Modify-Write Capability both on Single Bit and in Nibble Mode Operation

DESCRIPTION

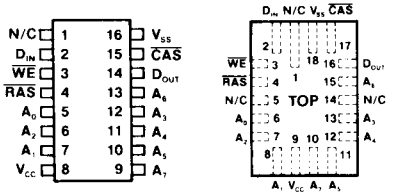
The INMOS IMS2600M 64Kx1 Dynamic RAM is processed in full compliance to MIL-STD-883C. This RAM is fabricated with INMOS' proprietary NMOS technology and utilizes innovative circuit techniques to achieve high performance, low power and wide operating margins.

Multiplexed addresses allows the IMS2600M to be packaged in the conventional 16 pin DIP. Additionally, the IMS2600M features new functional enhancements that make it more versatile than previous dynamic RAMs. CAS-before-RAS Refresh is an "on-chip" refresh mechanism that is upward compatible to 256K generations because pin 1 is left as a no connect. "Nibble Mode" also provides high speed serial access of 4 bits of data, thus providing the system equivalent of 4-way interleaving on chip.

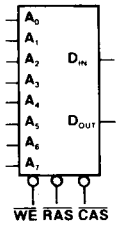
The IMS2600M is fully TTL compatible on all inputs and the output, and operates from a single +5V ±10% power supply.

The IMS2600M is a high speed VLSI RAM intended for military applications which demand high density as well as superior performance and reliability.

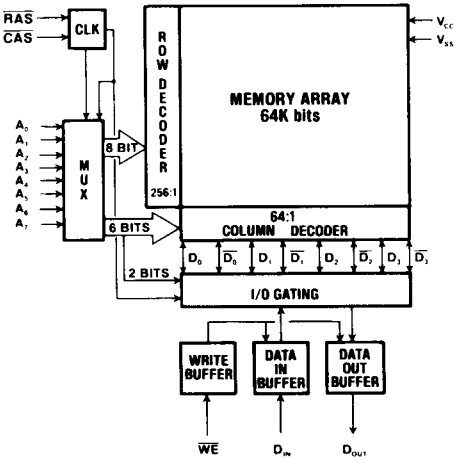
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5 VOLT SUPPLY INPUT
V_{SS}	GROUND

DEVICE OPERATION

The IMS2600M contains 65536 (2^{16}) bits of information as 256 (2^8) rows by 256 (2^8) columns. The sixteen addresses for unique bit selection are time-division multiplexed over eight address lines under control of the Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$) clocks. The normal sequence of $\overline{RAS}$ and $\overline{CAS}$ requires that $\overline{CAS}$ is high as $\overline{RAS}$ goes low. This causes the eight address inputs to be latched and decoded for selection of one of the 256 rows. The row addresses must be held for the specified period [t_{RAH} (min)] and then they may be switched to the appropriate column address. After the column addresses are stable for the specified column address setup time, $\overline{CAS}$ may be brought low. This causes the eight address inputs to be latched and used to select a single column in the specified row. The cycle is terminated by bringing $\overline{RAS}$ high. A new cycle may be initiated after $\overline{RAS}$ has been high for the specified precharge interval [t_{RP} (min)]. $\overline{RAS}$ and $\overline{CAS}$ must be properly overlapped and once brought low they must remain low for their specified pulse widths.

READ CYCLE

A read cycle is performed by sequencing $\overline{RAS}$ and $\overline{CAS}$ as described above while holding the $\overline{WE}$ input high during the period when $\overline{RAS}$ and $\overline{CAS}$ are both low. The read access time will be determined by the actual timing relationship between $\overline{RAS}$ and $\overline{CAS}$. If $\overline{CAS}$ goes low within the specified $\overline{RAS}$-to-$\overline{CAS}$ delay [t_{RCD} (max)], then the access time will be determined by $\overline{RAS}$ and be equal to t_{RAC} (max). If $\overline{CAS}$ occurs later than t_{RCD} (max) then the access time is measured from $\overline{CAS}$ and will be equal to t_{CAC} (max).

WRITE CYCLE

The IMS2600M will perform three types of write cycles: Early-Write, Late-Write or Read-Modify-Write. The difference between these cycles is that on an Early-Write D_{OUT} will remain open and on a Late-Write or Read-Modify-Write D_{OUT} will reflect the contents of the addressed cell before it was written.

The type of write cycle that is performed is determined by the relationship between $\overline{CAS}$ and $\overline{WE}$. For Early-Write cycles $\overline{WE}$ occurs before $\overline{CAS}$ goes low, and D_{IN} setup is referenced to the falling edge of $\overline{CAS}$. For Late-Write or Read-Modify-Write cycles $\overline{WE}$ occurs after $\overline{CAS}$, and D_{IN} setup is referenced to the falling edge of $\overline{WE}$.

The choice of write cycle timing is usually very system dependent and the different modes are made available to accommodate these differences. In general, the Early-Write timing is most appropriate for systems that have a bidirectional data bus. Because D_{OUT} remains inactive during Early-Write cycles, the D_{IN} and D_{OUT} pins may be tied together without bus contention.

DEVICE SELECTION AND OUTPUT CONTROL

Selection of a memory device for a read or write operation requires that both $\overline{RAS}$ and $\overline{CAS}$ be sequenced. A device is not selected if $\overline{RAS}$ is sequenced while $\overline{CAS}$ remains high or if $\overline{CAS}$ is sequenced while $\overline{RAS}$ remains high. The device must receive a properly overlapped $\overline{RAS}$/$\overline{CAS}$ sequence to be selected.

Once a device is selected the state of D_{OUT} becomes entirely controlled by $\overline{CAS}$. If $\overline{CAS}$ remains low when $\overline{RAS}$ goes high, D_{OUT} will remain in the state it was in when $\overline{RAS}$ went high. The output will remain unchanged even if a $\overline{RAS}$ sequence occurs while $\overline{CAS}$ is held low.

REFRESH

The IMS2600M remembers data by storing charge on a capacitor. Because the charge will leak away over a period of time it is necessary to access the data in the cell (capacitor) periodically in order to fully restore the stored charge while it is still at a sufficiently high level to be properly detected. For the IMS2600M any $\overline{RAS}$ sequence will fully refresh an entire row of 256 bits. To ensure that all cells remain sufficiently refreshed, all 256 rows must be refreshed every 4 ms.

The addressing of the rows for refresh may be sourced either externally or internally. If the row refresh addresses are to be provided from an external source, $\overline{CAS}$ must be high when $\overline{RAS}$ goes low. If $\overline{CAS}$ is high when $\overline{RAS}$ goes low, any type of cycle (Read, Write, Read-Modify-Write or $\overline{RAS}$ only) will cause the addressed row to be refreshed.

If $\overline{CAS}$ is low when $\overline{RAS}$ falls, the IMS2600M will use an internal 8-bit counter as the source of the row addresses and will ignore the address inputs. This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh-only mode and no data access is allowed. Also, $\overline{CAS}$-before-$\overline{RAS}$ refresh does not cause device selection and the state of D_{OUT} will remain unchanged.

NIBBLE MODE

The IMS2600M is designed to allow high-speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during Nibble Mode are determined by the eight row addresses and the most significant 6 bits of the column address. The low-order 2 bits of the column address (A_3, A_6) are used to select one of the 4 nibble bits for initial access. After the first bit is accessed the remaining nibble bits may be accessed by bringing $\overline{CAS}$ high then low (toggle) while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes A_3 and A_6 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for read, write and/or read-modify-write access (See Table 1 for example). If more than 4 bits are accessed during Nibble Mode, the address sequence will begin to repeat. If any bit is written during an access, the new value will be read on any subsequent accesses.

In Nibble Mode, read, write and read-modify-write operations may be performed in any desired combination. (e.g., first bit read, second bit write, third bit read-modify-write, etc.)

Table 1
NIBBLE MODE ADDRESSING SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	ROW ADDRESSES	COLUMN ADDRESSES A_3, A_6	
$\overline{RAS}$/$\overline{CAS}$	1	10101010	10101010	generated externally
toggle $\overline{CAS}$	2	10101010	10101011	
toggle $\overline{CAS}$	3	10101010	10101000	generated internally
toggle $\overline{CAS}$	4	10101010	10101001	
toggle $\overline{CAS}$	1	10101010	10101010	repeats

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc relative to Vss.....-1.0 to +7.0V
Storage Temperature (Ceramic)....-65° C to +150°C
Power Dissipation.....1W
Short Circuit Output Current.....50mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS [a, b]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	Logic "1" Voltage	2.4		Vcc+1	V	
V_{IL}	Logic "0" Voltage	-2.0		0.8	V	
T_A	Ambient Operating Temperature	-55°		110	°C	Still Air

DC Electrical Characteristics ($-55°C \le T_A \le 110°C$, $V_{CC} = 5.0V \pm 10\%$) [c]

SYM	PARAMETER		MIN	MAX	UNIT	NOTES
I_{CC_1}	Average Vcc Power Supply (Dynamic Operating) Current	IMS2600M-10		85	mA	tRC = 160ns, tRAS = 100ns
		IMS2600M-10		65		tRC = 350ns, tRAS = 100ns
		IMS2600M-12		85		tRC = 190ns, tRAS = 120ns
		IMS2600M-12		65		tRC = 350ns, tRAS = 120ns
		IMS2600M-15		75		tRC = 230ns, tRAS = 150ns
		IMS2600M-15		65		tRC = 350ns, tRAS = 150ns
I_{CC_2}	Supply Current (Active)			20	mA	RAS & CAS ≤ VIL (max)
I_{CC_3}	Standby Current			5.0	mA	RAS & CAS ≤ VIH (max)
I_{ILK}	Input Leakage Current (any input)			±10	µA	0V ≤VIN ≤ 5.5V (others = 0 V)
I_{OLK}	Output Leakage Current			±10	µA	DOUT = Hi-Z, 0V ≤ DOUT ≤ 5.5V
VOH	Output High Voltage		2.4		V	IOH = -5.0 mA
VOL	Output Low Voltage			0.4	V	IOL =+5.0 mA

Note a: All voltage values in this data sheet are with respect to Vss.
b: After power-up, a pause of 500 µs followed by eight initialization memory cycles is required to achieve proper device operation. Any interval greater than 4 ms with RAS inactivity requires eight reinitialization cycles to achieve proper device operation.
c: Icc is dependent on output loading and cycle rates. Specified values are obtained with output open.

AC TEST CONDITIONS

Input Pulse Levels.....0 to 3V
Input Rise and Fall Times.....5ns between 0.8 and 2.4V
Input and Output Timing Ref. Levels.....0.8 and 2.4V
Output Load.....Equivalent to 2 TTL Loads and 50pF

CAPACITANCE

SYM.	PARAMETER	MAX	UNITS	COND.
CIN	I/P Cap RAS, CAS, WE	6	pF	d
CIN	I/P Cap. Addresses	5	pF	d
COUT	O/P Capacitance	7	pF	d o

Note d: Capacitance measured with BOONTON METER.
o: CAS = VIH to disable DOUT

AC OPERATING CONDITIONS ($-55°C \leq T_A \leq +110°C$) ($V_{CC} = 5.0V \pm 10\%$)

NO.	SYM.	PARAMETER	IMS2600M-10		IMS2600M-12		IMS2600M-15		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{RC}	Random Read Cycle Time	160		190		230		ns	
2	t_{RAC}	Access Time from RAS		100		120		150	ns	h
3	t_{CAC}	Access Time from CAS		60		75		90	ns	i
4	t_{RAS}	RAS Pulse Width	100	10K	120	10K	150	10K	ns	
5	t_{RSH}	RAS Hold Time	60		75		90		ns	
6	t_{CAS}	CAS Pulse Width	60		75		90		ns	
7	t_{CSH}	CAS Hold Time	100		120		150		ns	
8	t_{RCD}	RAS to CAS Delay Time	15	40	17	45	20	60	ns	e, j
9	t_{CRS}	CAS to RAS Set-up Time	0		0		0		ns	
10	t_{RP}	RAS Precharge Time	50		60		70		ns	
11	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
12	t_{RAH}	Row Address Hold Time	10		12		15		ns	
13	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
14	t_{CAH}	Column Address Hold Time (Ref. CAS)	25		35		45		ns	
15	t_{AR}	Column Address Hold Time (Ref. RAS)	55		75		95		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
17	t_{RCH}	Read Command Hold Time (Ref. CAS)	0		0		0		ns	k
18	t_{RRH}	Read Command Hold Time (Ref. RAS)	0		0		0		ns	k
19	t_{OFF}	Output Buffer Turn-off Delay	0	25	0	25	0	30	ns	f
20	t_{WCS}	Write Command Set-up Time	0		0		0		ns	m
21	t_{WCH}	Write Command Hold Time (Ref. CAS)	25		30		35		ns	
22	t_{WCR}	Write Command Hold Time (Ref. RAS)	65		70		85		ns	
23	t_{WP}	Write Pulse Width	20		25		30		ns	
24	t_{DS}	Data-in Set-up Time	0		0		0		ns	l
25	t_{DH}	Data-in Hold Time (Ref. CAS)	25		30		35		ns	l
26	t_{DHR}	Data-in Hold Time (Ref. RAS)	55		70		85		ns	
27	t_{RW}	Read-Write Cycle Time	180		215		260		ns	
27	t_{RMW}	Read-Modify-Write Cycle Time	190		225		270		ns	
28	t_{RRW}	Read-Write Cycle RAS Pulse Width	120		145		180		ns	
28	t_{RRW}	Read-Modify-Write Cycle RAS P. W.	130		155		190		ns	
29	t_{CRW}	Read-Write Cycle CAS Pulse Width	90		105		130		ns	
29	t_{CRW}	Read-Modify-Write Cycle CAS P. W.	100		115		140		ns	
30	t_{RDW}	RAS to Write Delay	100		110		140		ns	m
31	t_{CWD}	CAS to Write Delay	60		70		90		ns	m
32	t_{RWL}	Write Command to RAS Lead Time	25		30		35		ns	

AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 110°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYM.	PARAMETER	IMS2600M-10		IMS2600M-12		IMS2600M-15		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
33	t_{CWL}	Write Command to CAS Lead Time	25		30		35		ns	
34	t_{NC}	Nibble Mode Read Cycle Time	55		65		75		ns	
35	t_{NCAC}	Nibble Mode Acces Time from CAS		25		30		35	ns	
36	t_{NCAS}	Nibble Mode CAS Pulse Width	25		30		35		ns	
37	t_{NCP}	Nibble Mode CAS Precharge Time	20		25		30		ns	
38	t_{NRSH}	Nibble Mode RAS Hold Time	25		30		35		ns	
39	t_{NRMW}	Nibble Mode RMW Cycle Time	80		95		110		ns	
40	t_{NCRW}	Nibble Mode RMW CAS Pulse Width	45		60		70		ns	
41	t_{NCWD}	Nibble Mode CAS to Write Delay	20		25		30		ns	
42	t_{FCS}	Refresh Set-up for CAS (Ref. RAS)	0		0		0		ns	
43	t_{FCH}	Refresh Hold Time (Ref. RAS)	15		17		20		ns	
	t_{REF}	Refresh Period		4		4		4	ms	
	t_T	Input Rise and Fall Times	3	50	3	50	3	50	ns	n

NOTES:

e: t_{RCD} (max) is a derived parameter; t_{RCD} (max) = t_{RAC} (max) − t_{CAC} (max); t_{RCD} (min) is a restrictive parameter due to CAS-before-RAS refresh.

f: t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition.

h: Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).

i: Assumes that $t_{RCD} \geq t_{RCD}$ (max).

j: Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is determined exclusively by t_{CAC}.

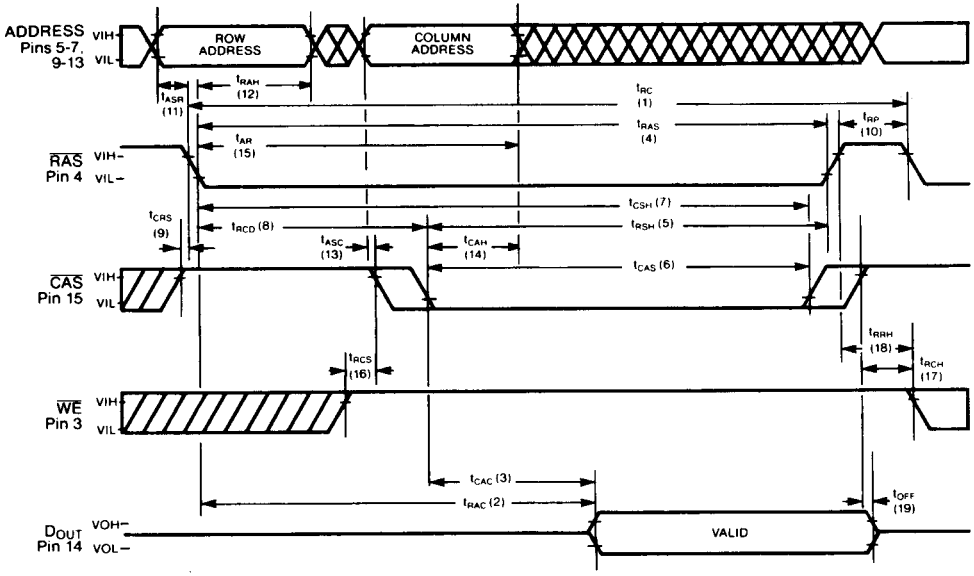
k: Either t_{RRH} or t_{RCH} must be satisfied for a Read cycle.

l: These parameters are referenced to CAS leading edge in Early-Write cycles, and to WE leading edge in Read-Write or Read-Modify-Write cycles.

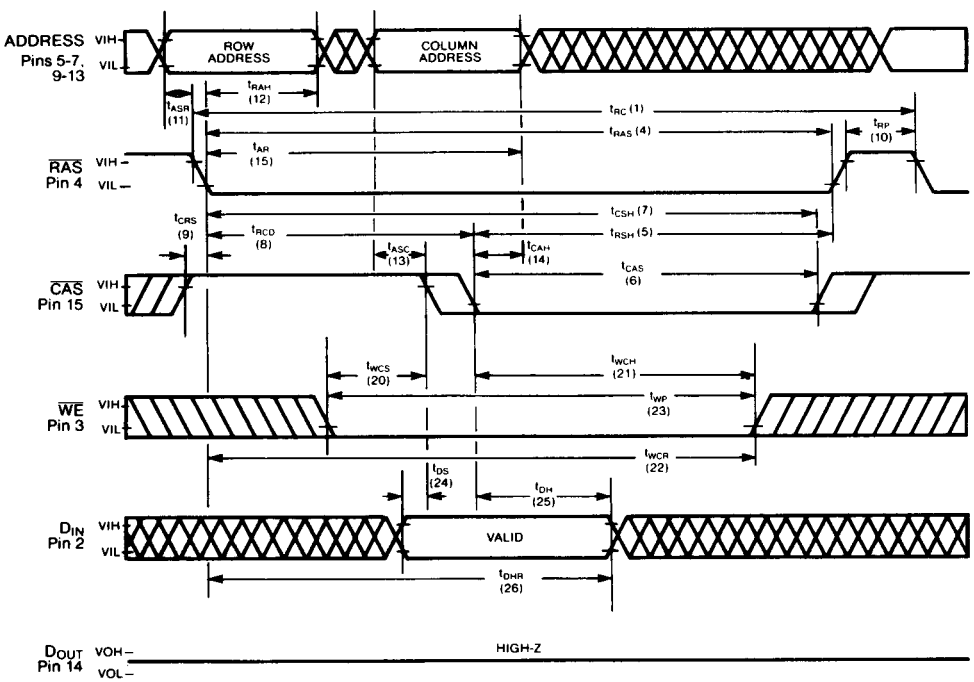
m: t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an Early-Write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions is met the condition of the data out is indeterminate at access time and remains so until CAS returns to V_{IH}.

n: The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Transition time measured between V_{IL} (max) and V_{IH} (min).

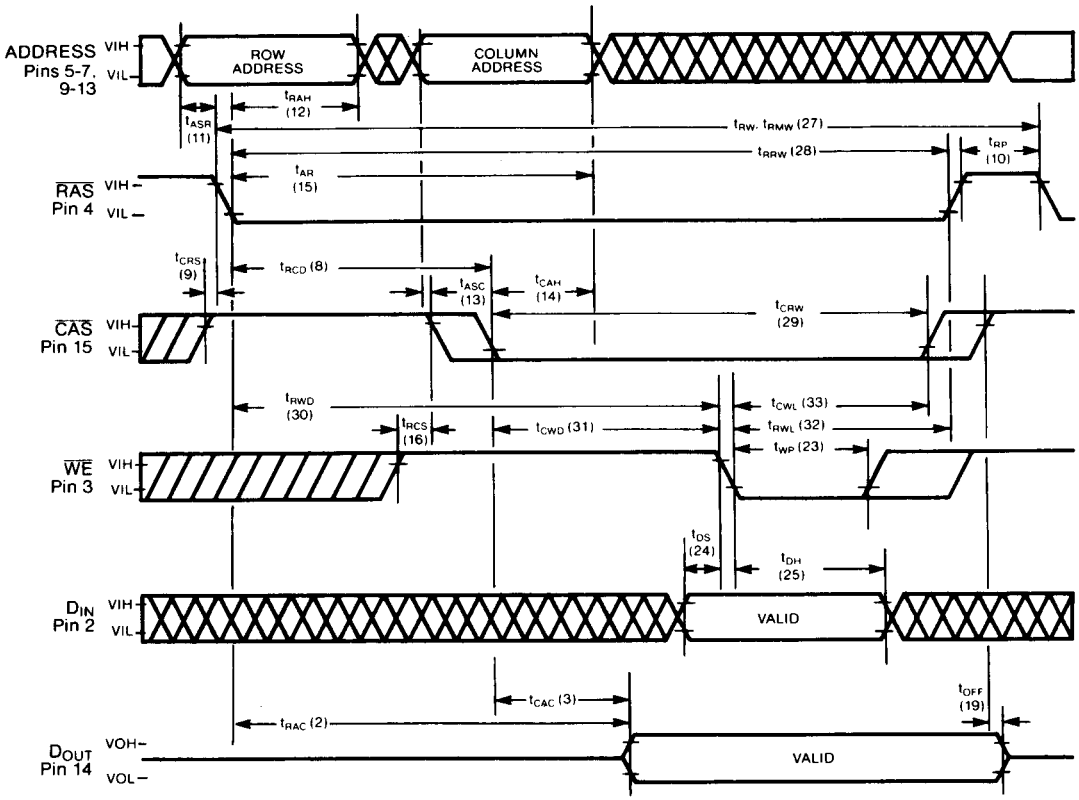
READ CYCLE



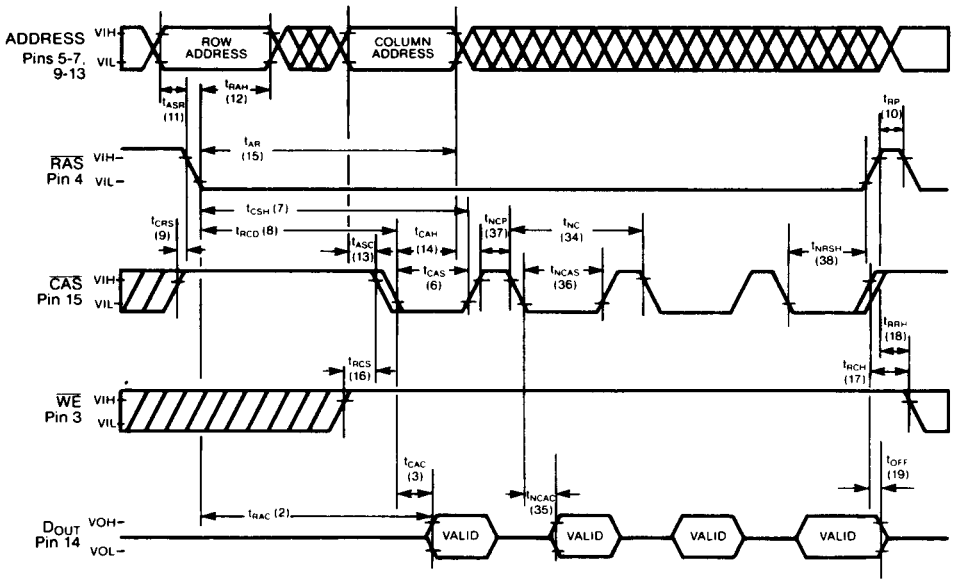
WRITE CYCLE



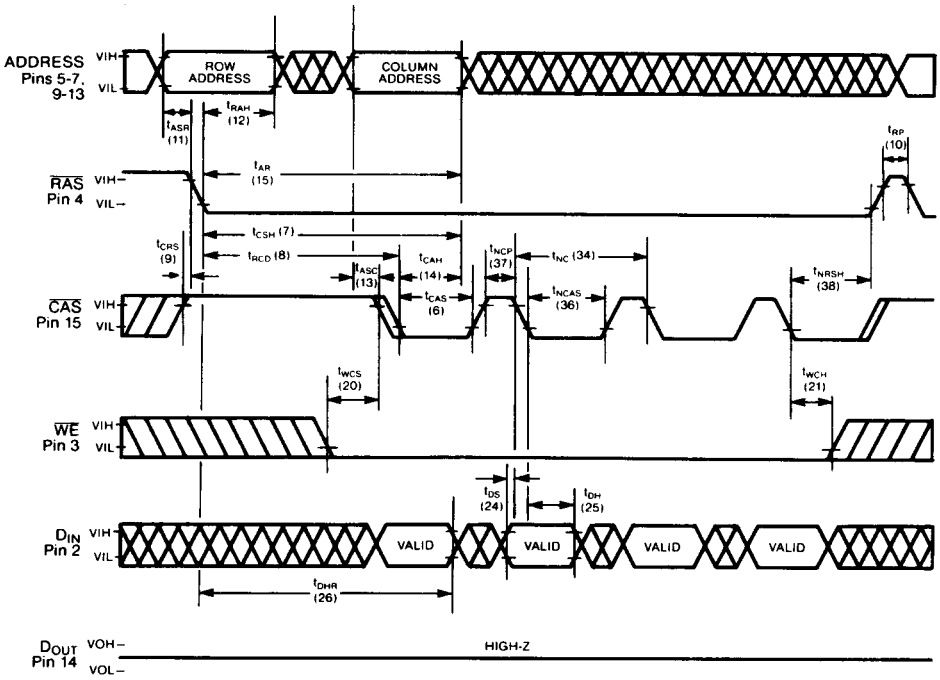
READ-WRITE/READ-MODIFY-WRITE CYCLE



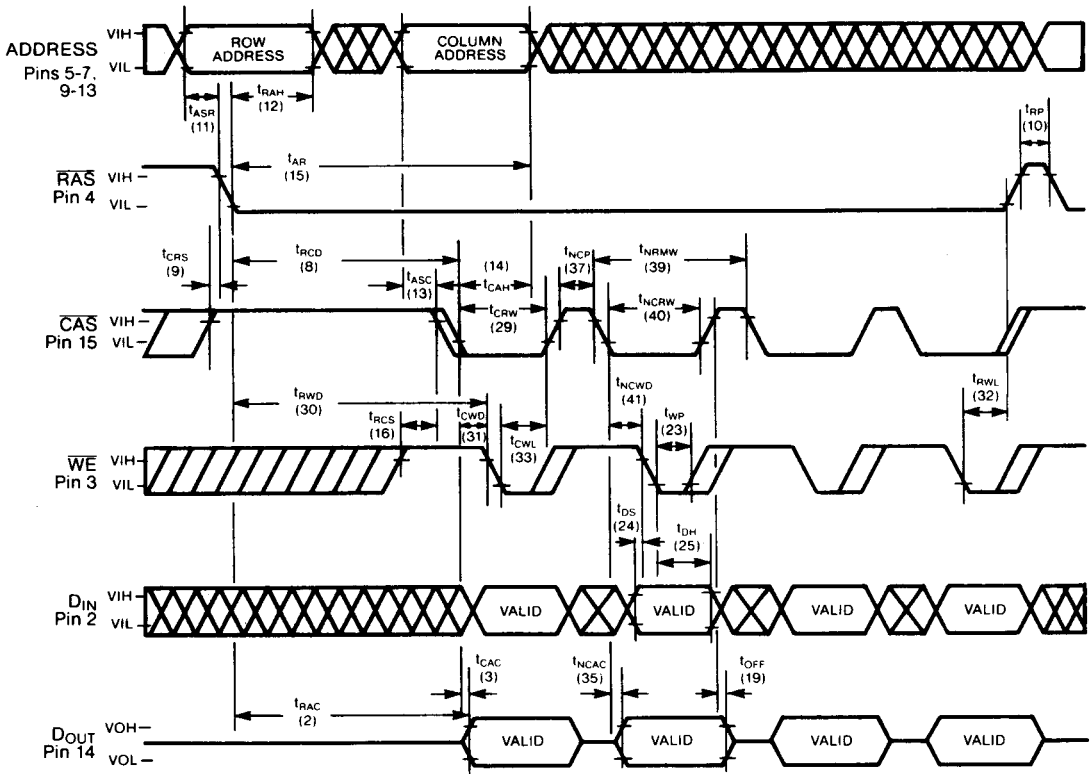
NIBBLE MODE READ CYCLE



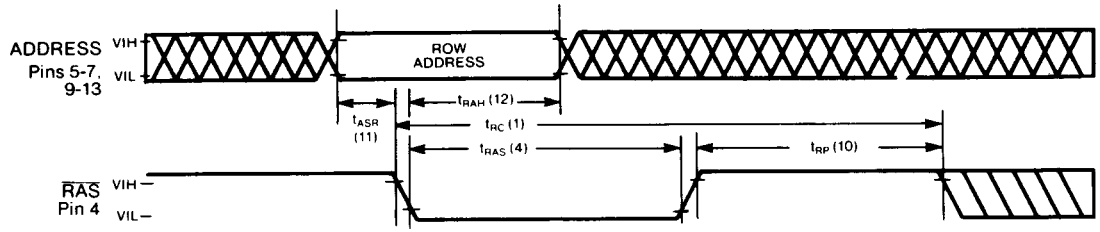
NIBBLE MODE WRITE CYCLE



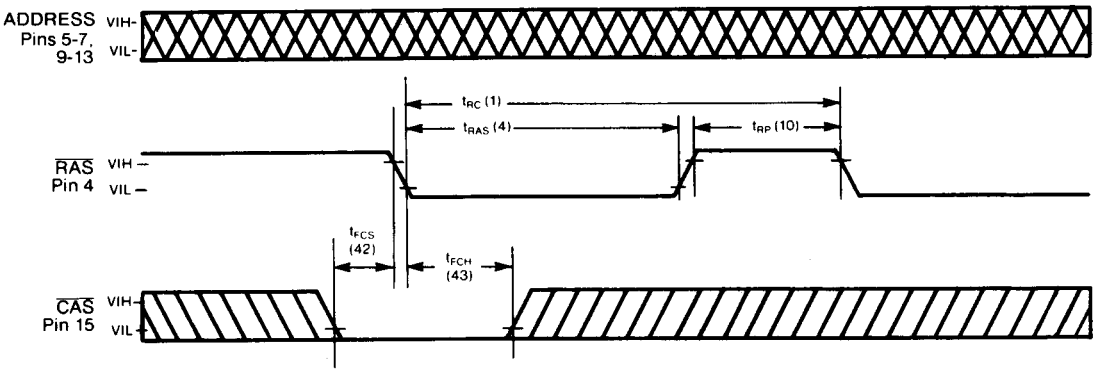
NIBBLE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH [CAS ≥ V_{IH} (min)]



CAS-BEFORE-RAS REFRESH



APPLICATION

To ensure proper operation of the IMS2600M in a system environment it is recommended that the following guidelines on board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (8) through the decoupling capacitor, to the ground pin (16) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line and the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. To prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry. A high-frequency decoupling capacitor with a value of 0.1μF should be placed between the rows of memory devices in the array. A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propogating down the lines, especially low-going TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver/termination combination close to the memory array. Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are among the most important, yet basic guidelines to be followed. These guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 2600M	100ns	CERAMIC DIP	IMS2600S-100M
	100ns	CERAMIC LCC	IMS2600N-100M
	100ns	CERAMIC DIP	IMS2600K-100M
	120ns	CERAMIC DIP	IMS2600S-120M
	120ns	CERAMIC LCC	IMS2600N-120M
	120ns	CERAMIC DIP	IMS2600K-100M
	150ns	CERAMIC DIP	IMS2600S-150M
	150ns	CERAMIC LCC	IMS2600N-150M
	150ns	CERAMIC DIP	IMS2600K-100M