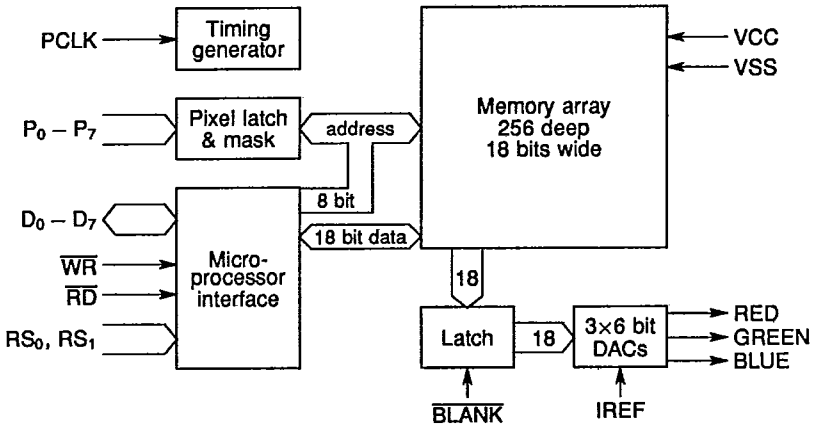
IMS G171
High performance CMOS colour look-up table

Designed to be compatible with IBM PS/2[1], VGA graphics systems



FEATURES

- Compatible with the RS170 video standard.
- Pixel rates up to 50MHz.
- 256K possible colours.
- Single monolithic, high performance CMOS.
- Up to 8 bits per pixel.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun, composite blank.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single +5V ±10% power supply.
- Low power dissipation, 880mW max. at maximum pixel rate.
- Standard 600 mil 28 pin DIL package.

DESCRIPTION

The IMS G171 integrates the functions of a colour look-up table (or colour palette), digital to analogue converters (designed to drive into a doubly terminated 75Ω line) and bi-directional microprocessor interface into a single 28 pin package.

Capable of displaying 256 colours from a total of 262,144 colours, the IMS G171 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

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3.1 Pin designations

3.1.1 Pixel interface

Signal	Pin	I/O	Signal name	Description
PCLK	13	I	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address and Blank inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the colour look-up table to the analogue outputs.
$P_0 - P_7$	5–12	I	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel mask register and then used as the address into the colour look-up table.
$\overline{\text{BLANK}}$	16	I	Blank	A low value on this input, when sampled, will cause a colour value of zero to be applied to the inputs of the DACs regardless of the colour value of the current pixel.

3.1.2 Analogue interface

Signal	Pin	I/O	Signal name	Description
RED GREEN BLUE	1 2 3	O O O		These signals are the outputs of the 6 bit DACs. Each DAC is composed of 63 current sources whose outputs are summed. The number of current sources active is controlled by the 6 bit binary value applied to each DAC.
IREF	4	I	Reference current	The reference current drawn from VCC via the IREF pin determines the current sourced by each of the current sources in the DACs.

3.1.3 Microprocessor interface

Signal	Pin	I/O	Signal name	Description
$\overline{WR}$	25	I	Write enable	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
$\overline{RD}$	15	I	Read enable	Most of the operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the colour look-up table. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behaviour. The Read and Write Enable signals should not be asserted at the same time.
RS_0, RS_1	26,27	I	Register select	The values on these inputs are sampled on the falling edge of the active enable signal ($\overline{RD}$ or $\overline{WR}$); they specify which one of the internal registers is to be accessed. See Internal Register description for the function of these registers.
$D_0 - D_7$	17–24	I/O	Program Data	Data is transferred between the 8 bit wide Program Data bus and the registers within the IMS G171 under control of the active enable signal ($\overline{RD}$ or $\overline{WR}$). In a write cycle the rising edge of $\overline{WR}$ validates the data on the program data bus and causes it to be written to the register selected. The rising edge of the $\overline{RD}$ signal signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register selected and will go to a high impedance state.

3.1.4 Power supply

Signal	Pin	Signal name	Description
VCC	28	Power supply	Digital and analogue supply pads are bonded out to a single pin. The package contains a high-frequency decoupling capacitor between VCC and VSS to ensure a high quality analogue supply.
VSS	14	Ground	

3.1.5 Internal registers

RS_1	RS_0	Size (bits)	Register name	Description
				There is a single Address register within the IMS G171. This register can be accessed through either register select 0,0 or register select 1,1
0	0	8	Address (write mode)	Writing a value to register 0,0 performs the following operations which would normally precede writing one or more new colour definitions to the colour look-up table: a) Specifies an address within the colour look-up table. b) Initialises the Colour Value register.
1	1	8	Address (read mode)	Writing a value to register 1,1 performs the following operations which would normally precede reading one or more colour definitions from the colour look-up table: a) Specifies an address within the the colour look-up table. b) Loads the Colour Value register with the contents of the location in the colour look-up table addressed and then increments the Address register. A read from register 0,0 is identical to a read from 1,1.
0	1	18	Colour Value	The Colour Value register is internally an 18 bit wide register used as a buffer between the microprocessor interface and the colour look-up table. A value can be read from or written to this register by a sequence of three byte transfers at this register address. When a byte is written only the least significant six bits ($D_0 - D_5$) are used. When a byte is read only the least significant six bits contain information — the most significant two bits being set to zero. The sequence of data transfer is red first, green second and blue last. After writing three values to this register its contents are written to the location in the colour look-up table specified by the Address register. The Address register then increments. After reading three values from this register the contents of the location in the colour look-up table specified by the Address register are copied into the Colour Value register. The Address register then increments. Each transfer between the Colour Value register and the colour look-up table replaces the normal pixel mapping operation of the IMS G171 for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs ($P_0 - P_7$). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, a zero setting that bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed, via that interface.

3.2 Device description

The IMS G171 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store (or look-up table) of 256 × 18 bit words, three 6 bit high speed DACs, a microprocessor interface and a pixel word mask.

An 8 bit value read in on the Pixel Address inputs is used as a read address for the look-up table and results in an 18 bit data word being output from the table. This data is partitioned as three fields of 6 bits, each field being applied to the inputs of a 6 bit DAC.

Pixel rates of up to 50 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the IMS G171. This signal acts on all three of the analogue outputs. The $\overline{\text{BLANK}}$ signal is delayed internally so that it appears at the analogue outputs with the correct relationship to the pixel stream.

The contents of the look-up table can be accessed via an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows colour value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the colour look-up table to facilitate such operations as animation and flashing objects. The pixel mask register is directly in the pixel stream, thus operations on the contents of the mask register should be synchronised to the pixel stream.

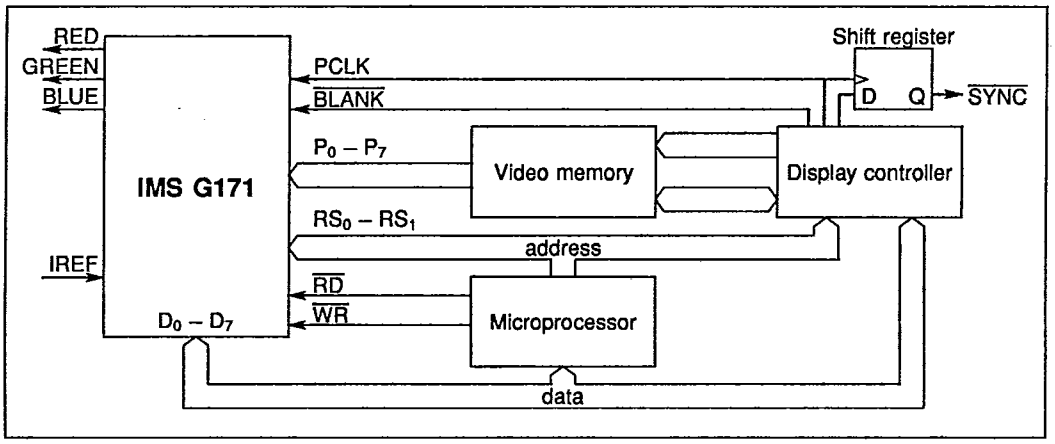

Figure 3.1 Typical IMS G171 application

3.2.1 Video path

Pixel address and $\overline{\text{BLANK}}$ inputs are sampled on the rising edge of Pixel Clock, their effect appears at the analogue outputs after three further rising edges of Pixel Clock (see figure 3.2).

3.2.2 Analogue outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an IREF of 8.88 mA when driving a doubly terminated 75Ω load . This corresponds to an effective DAC output loading ($R_{EFFECTIVE}$) of 37.5Ω.

The $\overline{\text{BLANK}}$ input to the IMS G171 acts on all three of the analogue outputs. When the $\overline{\text{BLANK}}$ input is low a binary zero is applied to the inputs of the DACs.

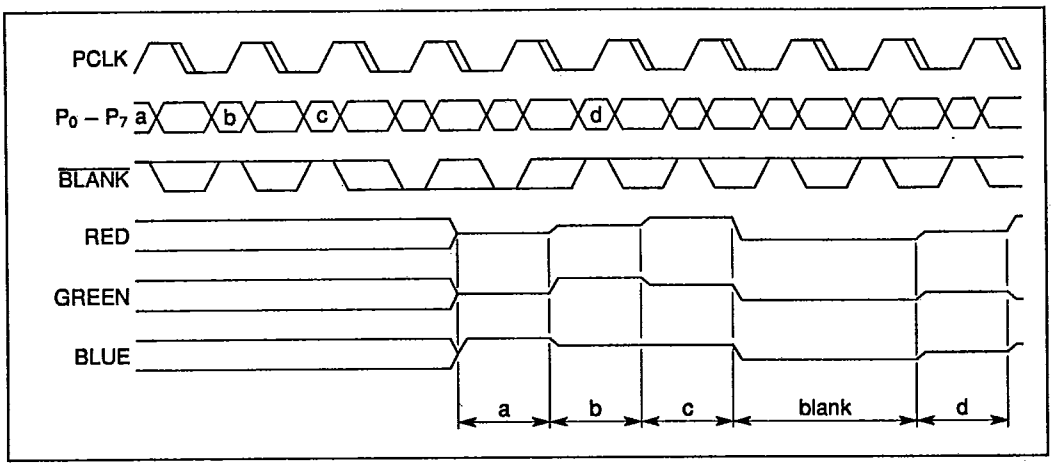

Figure 3.2

The expression for calculating IREF with various peak white voltage/output loading combinations is given below:

$$IREF = \frac{V_{PEAK\,WHITE}}{2.058 \times R_{EFFECTIVE}}$$

Note that for all values of IREF and output loading:

$$V_{BLACKLEVEL} = 0$$

3.2.3 Microprocessor Interface

Below are listed the three microprocessor interface registers within the IMS G171 and the four locations through which they can be accessed:

RS_1	RS_0	Register name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Colour Value
1	0	Pixel Mask

The contents of the colour look-up table can be accessed via the Colour Value register and the Address registers.

Writing to the look-up table

To set a new colour definition a value specifying a location in the colour look-up table is first written to the write mode Address register. The values for the red, green and blue intensities are then written in succession to the Colour Value register. After the blue data is written to the Colour Value register the new colour definition is transferred to the colour look-up table and the Address register is automatically incremented.

As the Address register increments after each new colour definition has been transfered from the Colour Value register to the colour look-up table, it is simple to write a set of consecutive locations with new colour definitions. First the start address of the set of locations is written to the write mode Address register; then the colour definitions for each location are written sequentially to the Colour Value register.

Reading from the look-up table

To read a colour definition a value specifying the location in the look-up table to be read is written to the read mode Address register. After this value has been written, the contents of the location specified are copied to the Colour Value register and the Address register is then automatically incremented.

The red, green and blue intensity values can be read by a sequence of three reads from the Colour Value register. After the blue value has been read the location in the look-up table currently specified by the Address register is copied to the Colour Value register and the Address register is again incremented automatically.

Thus a set of colour definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Address register and then sequentially reading the colour definitions for each location in the set.

Whenever the Address register is updated any unfinished colour definition read or write is aborted and a new one may begin.

Asynchronous look-up table access

Accesses to the Address and Colour Value registers may occur without reference to the high speed timing of the pixel stream being processed by the IMS G171. Internal logic synchronizes data transfers, between the look-up table and the Colour Value register, to the Pixel Clock in the period between the microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers to take place.

The Pixel Mask register

The pixel address used to access the colour look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colours without altering the video memory or the look-up table contents. Thus, by partitioning the colour definitions by one or more bits in the pixel address such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is independent of the Address and Colour Value registers. Operations on the Pixel Mask register are required to be synchronous to the pixel stream. The requirements for Pixel Mask register synchronisation are described in section 3.4.8.

3.3 Electrical specifications

3.3.1 Absolute maximum ratings *

Symbol	Parameter	Min.	Max.	Units	Notes
VCC	DC supply voltage		7.0	volts	
	Voltage on input and output pins	−1.0	VCC+0.5	volts	
TS	Storage temperature	−65	150	°C	
TA	Ambient temperature under bias	−40	85	°C	
PDmax	Power dissipation		1	W	
	Reference current	−15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

Notes

* Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3.3.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
VCC	Positive supply voltage	4.5	5.0	5.5	volts	2
VSS	Ground		0		volts	
VIH	Input logic '1' voltage	2.0		VCC+0.5	volts	
VIL	Input logic '0' voltage	−0.5		0.8	volts	3
TA	Ambient operating temperature	0		70	°C	4
IREF	Reference current	−7.0		−10	mA	5

Notes

1 All voltages are with respect to VSS unless otherwise specified.

2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

3 VIL(min) = −1.0V for a pulse width not exceeding 25% of the duty cycle (t_{CHCH}) or 10ns, whichever is the smaller value.

4 With a 400 linear ft/min transverse air flow.

5 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
ICC	Average power supply current		160	mA	4, IMS G171-50
ICC	Average power supply current		150	mA	4, IMS G171-35
VREF	Voltage at IREF input (pin 4)	VCC−3	VCC	volts	
IIN	Digital input current (any input)		±10	μA	5,6
IOZ	Off state digital output current		±50	μA	5,7
VOH	Output logic '1'	2.4		volts	IO = −5mA
VOL	Output logic '0'		0.4	volts	IO = 5mA

1 All voltages are with respect to VSS unless otherwise specified.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Over the range of the DC operating conditions unless specified otherwise.

4 IO = IO(max). ICC is dependent on digital loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

5 VCC = max, VSS ≤ VIN ≤ VCC.

6 On digital inputs, pins 5–13, 15, 16, 25–27.

7 On digital input/output, pins 17–24.

3.3.3 DAC characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
	Resolution	6		bits	
VO(max)	Output voltage		1.5	volts	IO≤10mA
IO(max)	Output current		−21	mA	VO≤1V
	Full scale error		±5	%	4
	DAC to DAC correlation error		±2	%	5
	Integral linearity error		±0.5	LSB	6
	Rise time (10% to 90%)		8	ns	7
	Full scale settling time		20	ns	7,8,9, IMS G171-50
	Full scale settling time		28	ns	7,8,9, IMS G171-35
	Glitch energy		200	pVsec	7,9

Notes

1 All voltages are with respect to VSS unless otherwise specified.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Tested over the operating temperature range and at nominal supply voltage with IREF = −8.88mA.

4 Full scale error from the value predicted by the design equations.

5 About the mid point of the distribution of the three DACs measured at full scale deflection.

6 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

7 Load = 37.5Ω + 30pF with IREF = −8.88mA.

8 From a 2% change in the output voltage until settling to within 2% of the final value.

9 This parameter is sampled, not 100% tested.

3.3.4 AC test conditions

Input pulse levels	VSS to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see figure 3.3

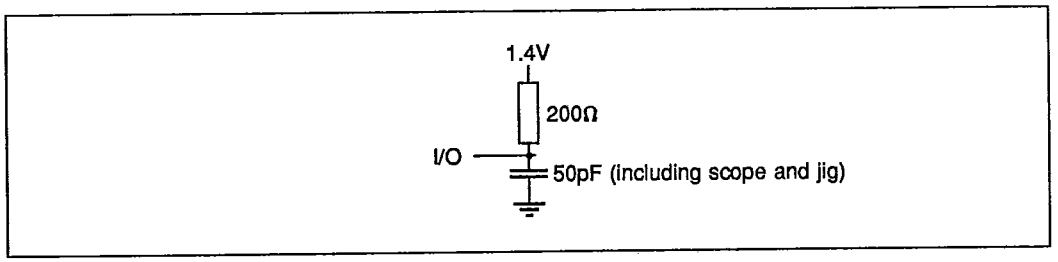

Figure 3.3 Digital output load

3.3.5 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes (1,2)
CI	Digital input		7	pF	
CO	Digital output		7	pF	3
COA	Analogue output		10	pF	4

Notes

1 These parameters are sampled, not 100% tested.

2 Measured on a BOONTON METER.

3 $\overline{RD} \geq$ VIH(min) to disable $D_0 - D_7$.

4 $\overline{BLANK} \leq$ VIL(max) to disable RED, GREEN and BLUE.

3.3.6 Video operation (figure 3.4)

Symbol	Parameter	All Max	35 MHz Min	50 MHz Min	Units	Notes
t_{CHCH}	PCLK period	10000	28	20	ns	
Δt_{CHCH}	PCLK jitter	±2.5			%	1
t_{CLCH}	PCLK width low	10000	9	6	ns	
t_{CHCL}	PCLK width high	10000	7	6	ns	
t_{PVCH}	Pixel address set-up time		5	4	ns	2
t_{CHPX}	Pixel address hold time		5	4	ns	2
t_{BVCH}	$\overline{BLANK}$ setup time		5	4	ns	
t_{CHBX}	$\overline{BLANK}$ hold time		5	4	ns	
t_{CHAV}	PCLK to valid DAC output	30	5	5	ns	3
Δt_{CHAV}	Differential output delay	2			ns	4
	Pixel clock transition time	50			ns	

Notes

1 This parameter allows for variation in the Pixel Clock frequency, but does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (t_{CHCH}) period specified above.

2 It is required that the Pixel Address input to the colour look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising edge of PCLK (this requirement must be met during the blanking period).

3 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

4 Between different analogue outputs on the same device.

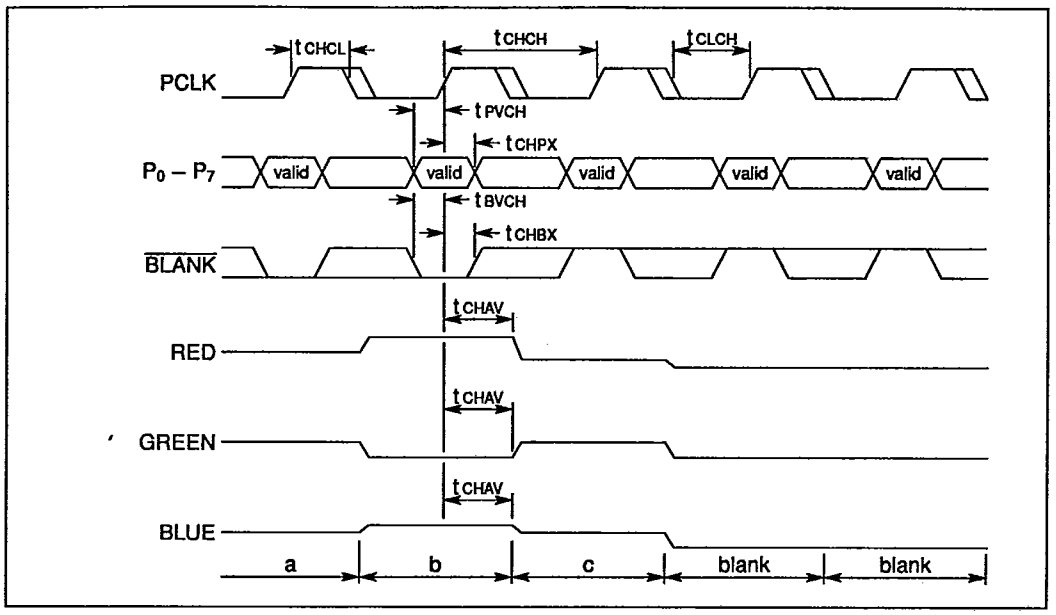

Figure 3.4 Video operation

3.3.7 Microprocessor interface operation (figures 3.5–3.13)

Symbol	Parameter	All Max	35 MHz Min	50 MHz Min	Units	Notes
t_{WLWH}	$\overline{WR}$ pulse width low		50	50	ns	
t_{RLRH}	$\overline{RD}$ pulse width low		50	50	ns	
t_{SVWL}	Register select setup time		15	10	ns	
t_{SVRL}	Register select setup time		15	10	ns	
t_{WLSX}	Register select hold time		15	10	ns	
t_{RLSX}	Register select hold time		15	10	ns	
t_{DVWH}	Write data setup time		15	10	ns	
t_{WHDX}	Write data hold time		15	10	ns	
t_{RLQX}	Output turn-on delay		5	5	ns	
t_{RLQV}	Read enable access time	40			ns	
t_{RHQX}	Output hold time		5	5	ns	
t_{RHQZ}	Output turn-off delay	20			ns	1
t_{WHWL1}	Successive write interval		$T1$	$T1$	ns	3
t_{WHRL1}	Write followed by read interval		$T1$	$T1$	ns	3
t_{RHRL1}	Successive read interval		$T1$	$T1$	ns	3
t_{RHWL1}	Read followed by write interval		$T1$	$T1$	ns	3
t_{WHWL2}	Write after colour write		$T1$	$T1$	ns	2,3
t_{WHRL2}	Read after colour write		$T1$	$T1$	ns	2,3
t_{RHRL2}	Read after colour read		$T2$	$T2$	ns	2,3
t_{RHWL2}	Write after colour read		$T2$	$T2$	ns	2,3
t_{WHRL3}	Read after read access write		$T2$	$T2$	ns	2,3
	Write/Read enable transition time	50			ns	

Notes

1 Measured ±200mV from steady output voltage.

2 This parameter allows for synchronisation between operations on the microprocessor interface and the pixel stream being processed by the colour look-up table.

3 $T1 = (3 \times t_{CHCH})$, $T2 = (6 \times t_{CHCH})$.

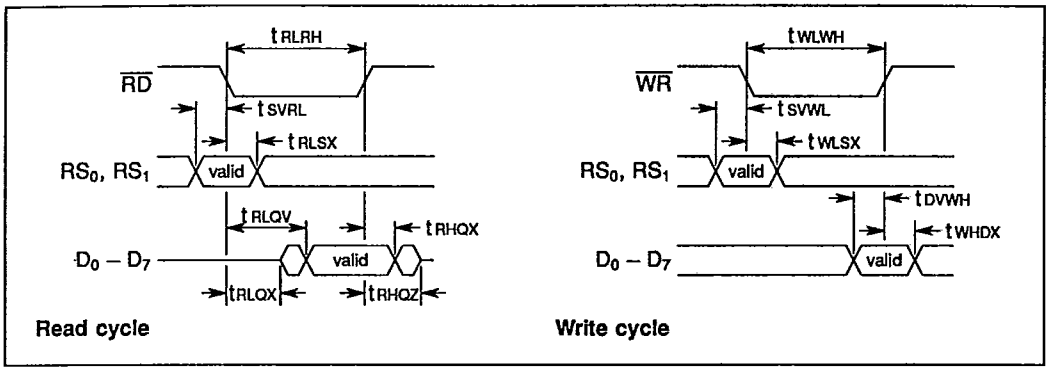

Figure 3.5 Basic read/write cycles

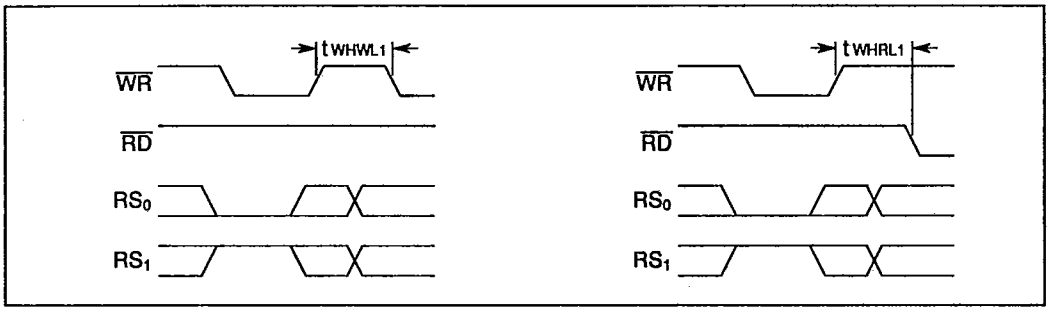

Figure 3.6 Write to pixel mask register followed by any access

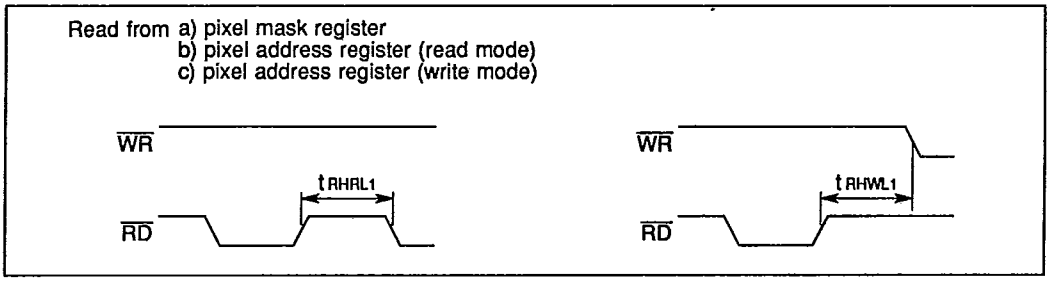

Figure 3.7 Read from register followed by any access

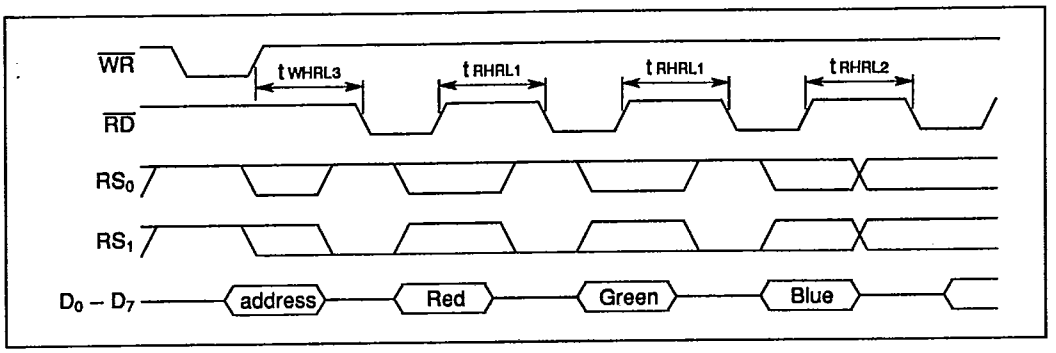

Figure 3.8 Colour value read followed by any read

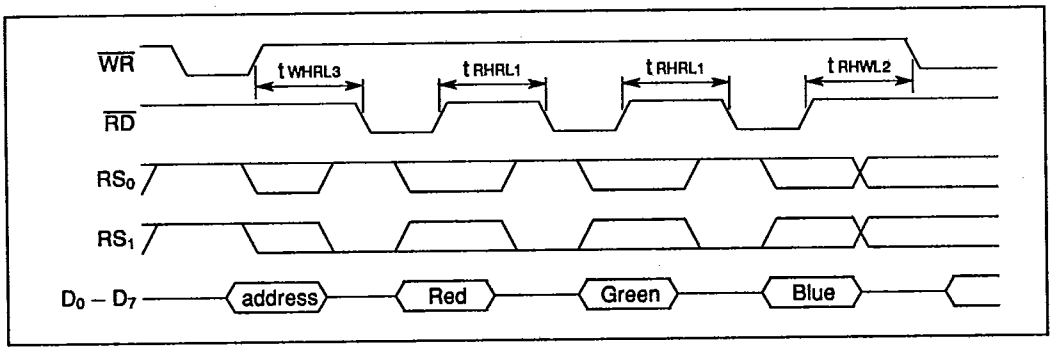

Figure 3.9 Colour value read followed by any write

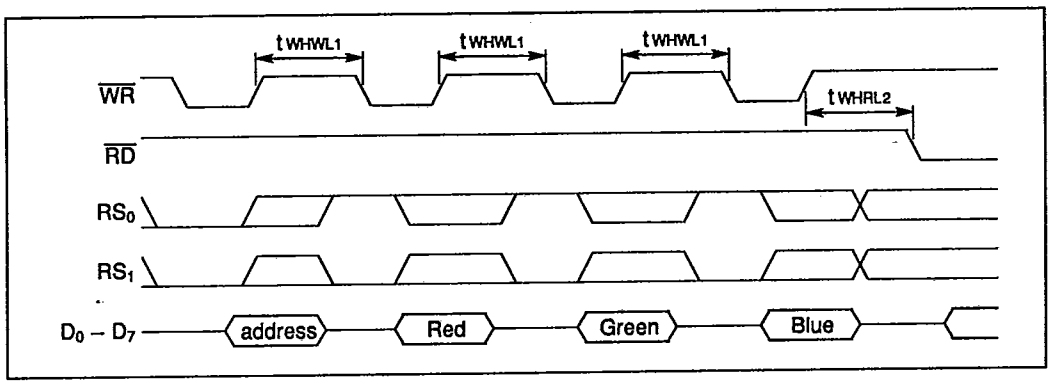

Figure 3.10 Colour value write followed by any read

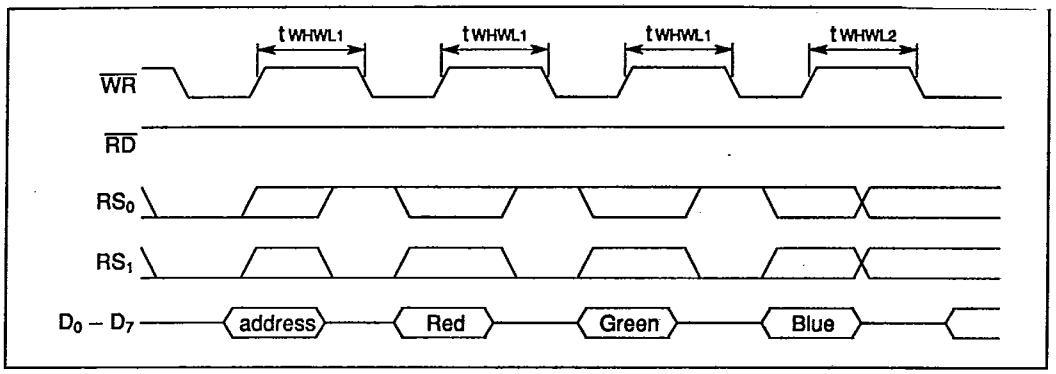

Figure 3.11 Colour value write followed by any write

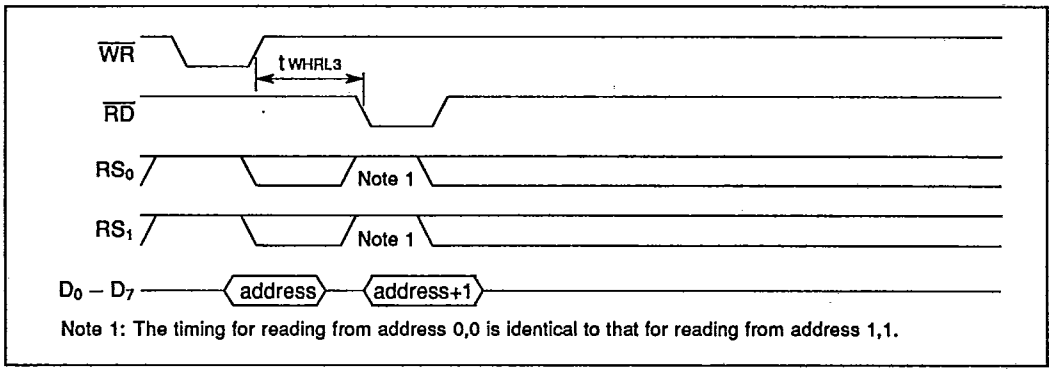

Figure 3.12 Write and read back address register (read mode)

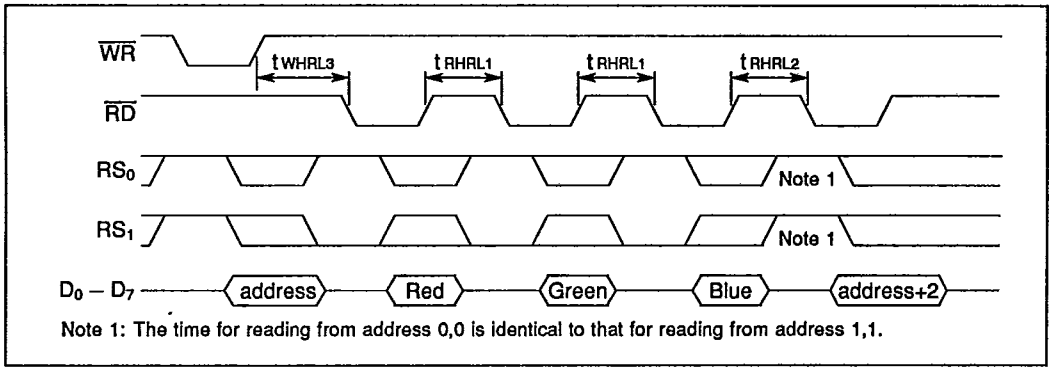

Figure 3.13 Read colour value then the address register (read mode)

3.4 Designing with the IMS G171

3.4.1 Board layout — general

The IMS G171 is a high speed CMOS device. As such it has relatively low DC power requirements. However, CMOS devices may draw large transient currents from the power supply. To supply the transient currents present in high speed video circuitry it is essential that proper consideration is given to board layout and decoupling circuitry when using the IMS G171. A four layer board with separate power and ground planes is strongly recommended, since this will minimise differential noise and impedance in the supply.

3.4.2 Power supply decoupling

To supply the transient currents required by the IMS G171 the impedance in the decoupling path between VCC and VSS should be a 0.1 μF high frequency capacitor in parallel with a larger tantalum capacitor with a value between 22 μF and 47 μF. An inductance may be added in series with the positive supply to form a low pass filter and so further improve the power supply local to the IMS G171.

The combination of series impedance in the ground supply to the IMS G171 and transients in the current drawn by the IMS G171 will appear as differences in the VSS voltages to the IMS G171 and to the digital devices driving it. To minimise this differential ground noise the impedance in the ground supply between the IMS G171 and the digital devices driving it should be minimised.

3.4.3 Analogue output — line driving

The DACs in the IMS G171 are made from summed, switched current sources. IREF sets the current sourced by each current source, the digital input to each DAC determines how many current sources are active. The load resistance between the DAC output and VSS determines the voltage produced by each DAC.

The connection between the DAC outputs of the IMS G171 and the RGB inputs of the monitor it is driving should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor. To ensure good signal fidelity, RF techniques should be observed. The PCB trace connecting the IMS G171 to the offboard connector should be sized so as to form a transmission line of the correct impedance. Correctly matched RF connectors should be used to connect from the PCB to the coaxial cable, and from the cable to the monitor being driven.

Two methods of DAC termination and their relative merits are described here.

Double termination

A load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line.

Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched, and thus should result in an ideal reflection free system.

This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

Also the rise time of the DAC outputs is dependent on the RC time constant of the load it is driving. Thus, a double terminated DAC output will rise faster than any singly terminated output.

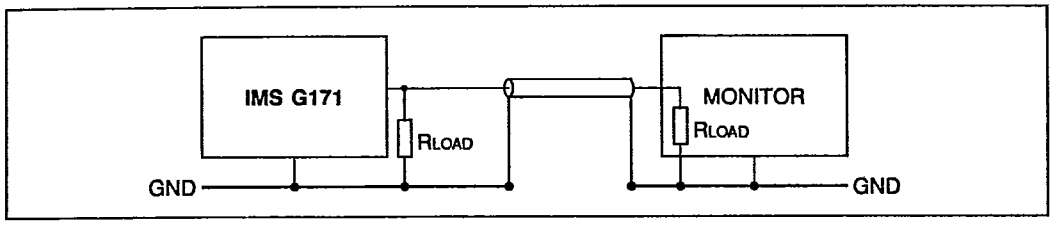

Figure 3.14 Double termination

Buffered signal

If the IMS G171 is required to drive large capacitative loads (for instance long lossy cable runs) it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should be considered as a transmission line. The buffer output will have a relatively low impedance so should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

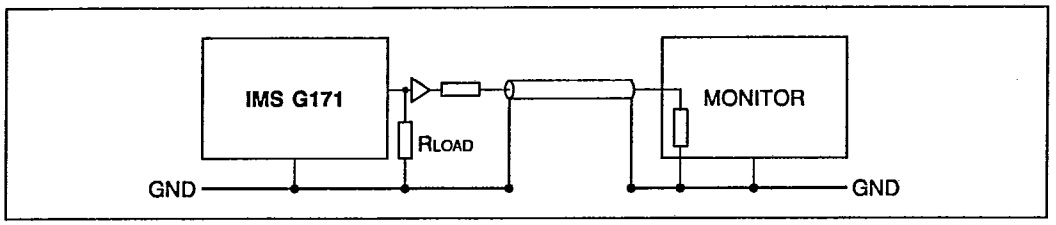

Figure 3.15 Buffered signal

3.4.4 Analogue output — protection

CMOS devices are susceptible to damage from from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G171 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G171 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection devices (e.g. IN4148 or any low cost silicon diode) should be considered at this exposed interface (see figure 3.17).

3.4.5 Digital input termination

The PCB trace lines between the outputs of the TTL devices driving the IMS G171 behave like low impedance transmission lines driven from a low impedance source and terminated with a high impedance. In accordance with transmission line principles signal transitions will be reflected from the high impedance input to the IMS G171. Similarly signal transitions will be inverted and reflected from the low impedance TTL output. To reduce or eliminate the ringing and in particular the undershoot that reflections cause, line termination is recommended. The termination may either be series or parallel.

The recommended technique is to use series termination. Series termination has the advantage of drawing no DC current and using fewer components. Series termination is accomplished by placing a resistor in series with the signal line at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and so ensures that any signal incident on the TTL output is not reflected.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a value around 100Ω will be required. Because each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be found empirically.

3.4.6 Current reference — design

To ensure that the output current of the DACs is predictable and stable with temperature variations an active current reference is recommended. Figure 3.16 shows four designs of current reference.

Figure 3.16d shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of VCC.

Figures 3.16a–c are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuit 3.16b and 3.16c the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 3.16c).

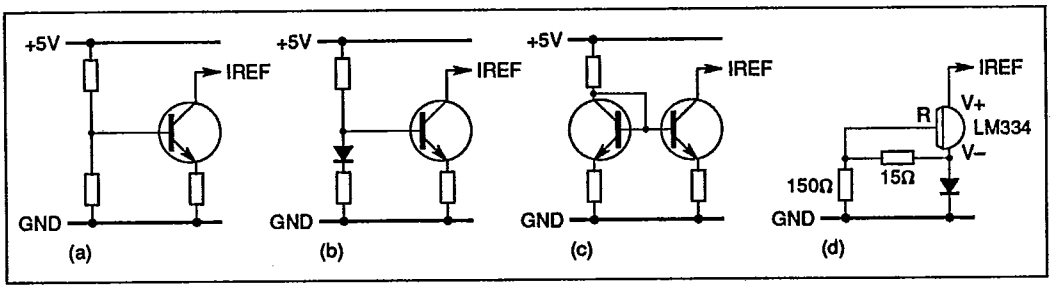

Figure 3.16

3.4.7 Current reference — decoupling

The DACs in the IMS G171 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capacitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the IREF input to VCC. This will enable the current reference to track both low and high frequency variations in the supply.

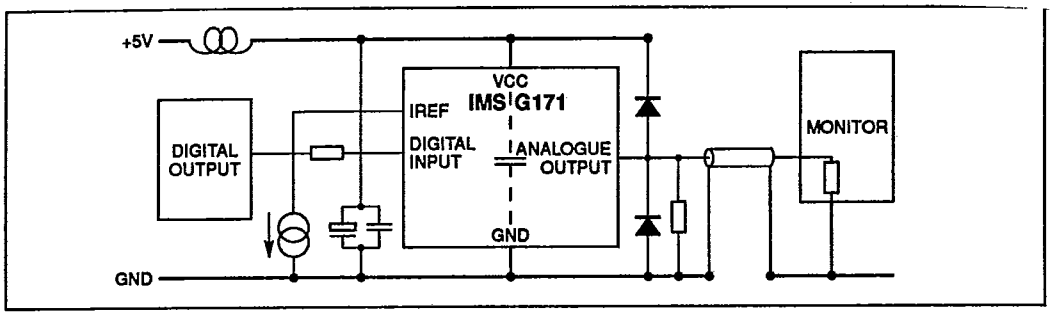

Figure 3.17 Circuit incorporating suggested design features

3.4.8 Pixel Mask register synchronisation

Each pixel address used as an address into the colour look-up table is masked by the Pixel Mask register.If the contents of the Pixel Mask register are modified asynchronously to PCLK there is a possibilty that the data held within the Pixel Mask register will change at such an instant as to corrupt the address applied to the look-up table as it is being latched.

If the Pixel Mask register is only initialised once on power up the synchronisation precautions described below need not be taken, it is sufficient simply to ensure that the colour look-up table is initialised after the Pixel Mask register. The synchronous properties of the Pixel Mask register in no way affect the ability to update the look-up table asynchronously,

If the Pixel Mask register is to be updated on a regular basis, asynchronously to PCLK, corruption of the look-up table contents will inevitably occur. To prevent such corruption the update of the mask register should occur at a time which ensures that the internal pixel mask value is not changing between values as it is being sampled. This requires that certain timing constraints synchronising $\overline{WR}$ to PCLK are met (see table 3.1).

The circuit given in figure 3.18 should be suitable for systems with pixel rates up to 35 MHz. The synchronisation circuitry required for systems working above 35 MHz may be more complex.

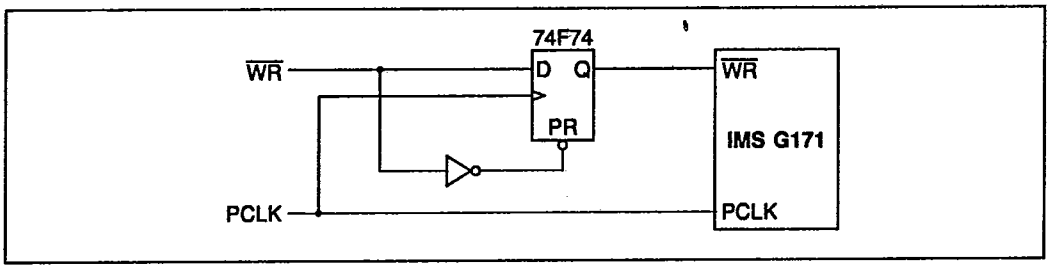

Figure 3.18

Symbol	Parameter	All	35 MHz	50 MHz	Units	Notes
		Max	Min	Min		
t_{WLCH}	$\overline{WR}$ illegal transition window	12	1	1	ns	1,2
t_{DVWL}	Data setup time		15	15	ns	2
t_{WHDX}	Data hold time		15	10	ns	

Table 3.1 Pixel mask register synchronisation.

Notes

1 $\overline{WR}$ should not change from high to low within the window delimited by the minimum and maximum times specified.

2 This parameter need only be observed if modifications of the value held in the Pixel Mask register are required to occur synchronously to the pixel stream.

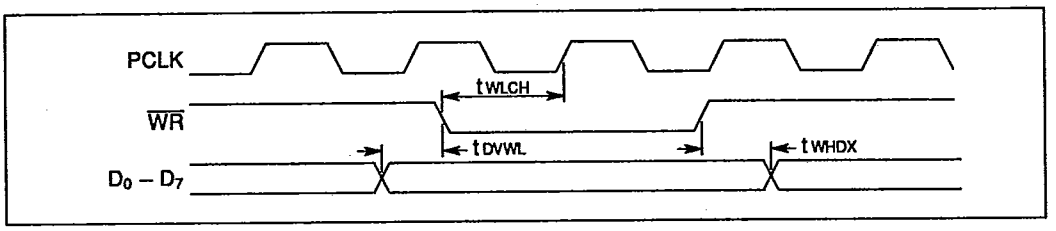

Figure 3.19 Pixel mask register synchronisation.

3.5 Package specifications

3.5.1 28 pin dual-in-line package

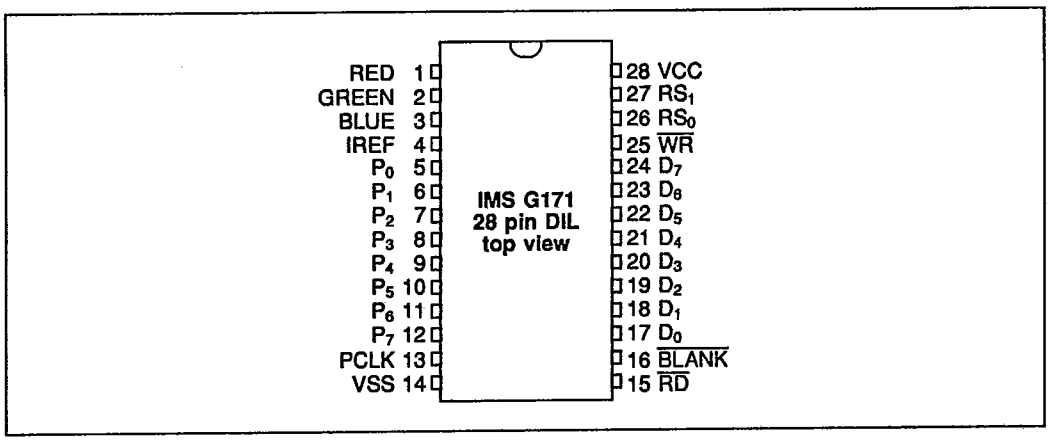

Figure 3.20 IMS G171 28 pin dual-in-line package pinout

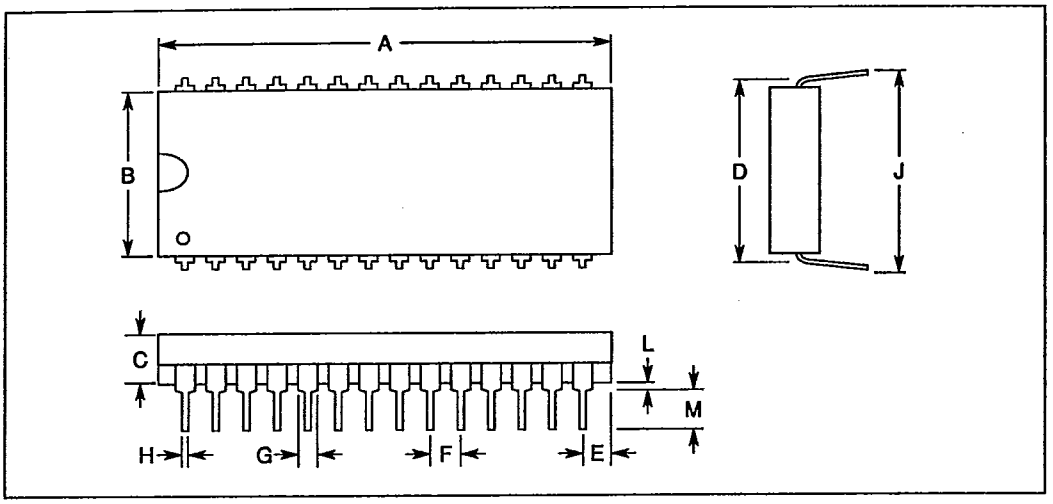

Figure 3.21 28 pin plastic dual-in-line package dimensions

DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	36.830	±0.254	1.450	±0.010	
B	13.970	±0.254	0.550	±0.010	
C	4.445	±0.635	0.175	±0.025	
D	15.240	±0.076	0.600	±0.003	
E	1.905		0.075		
F	2.540		0.100		
G	1.397	±0.254	0.055	±0.010	
H	0.457		0.018		
J	16.256	±0.508	0.640	±0.020	
L	0.508		0.020		Minimum
M	3.429		0.135		Maximum

Table 3.2 28 pin plastic dual-in-line package dimensions

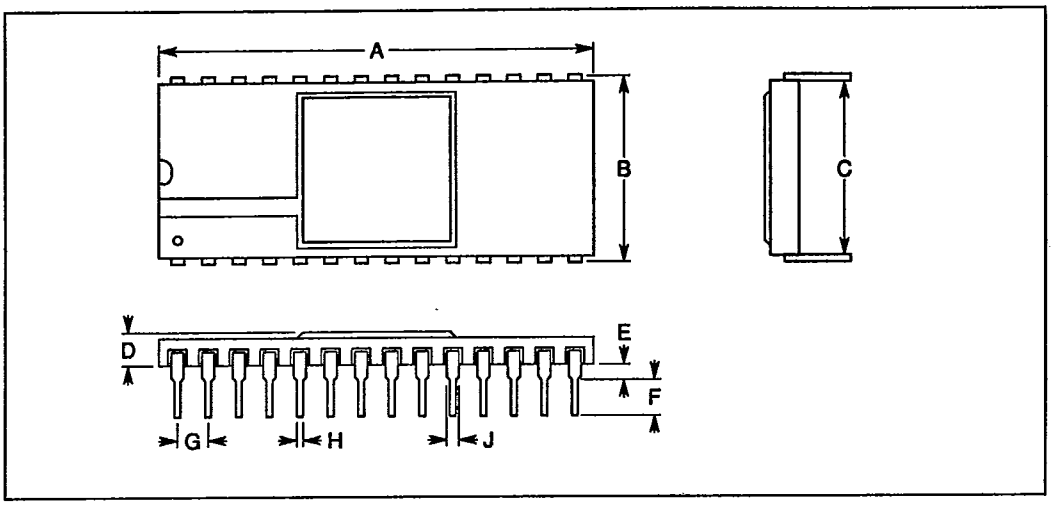

Figure 3.22 28 pin ceramic dual-in-line package dimensions

DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	35.560	±0.356	1.400	±0.014	
B	15.494	±0.254	0.610	±0.010	
C	14.681	+0.813	0.578	+0.032	
D	2.466	±0.229	0.097	±0.009	
E	1.270	±0.254	0.051	±0.010	
F	3.048		0.120		Minimum
G	2.540		0.100		
H	0.457	±0.051	0.018	±0.002	
J	1.016	+0.508	0.040	+0.020	

Table 3.3 28 pin ceramic dual-in-line package dimensions

3.5.2 Ordering information

Device	Clock rate	Package	Part number
IMS G171	35 MHz	Plastic DIP	IMSG171P-35
IMS G171	35 MHz	Ceramic DIP	IMSG171S-35
IMS G171	50 MHz	Plastic DIP	IMSG171P-50
IMS G171	50 MHz	Ceramic DIP	IMSG171S-50