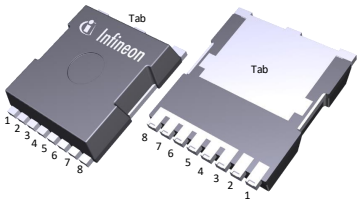
# SiC MOSFET

## CoolSiC™ MOSFET 650 V G2

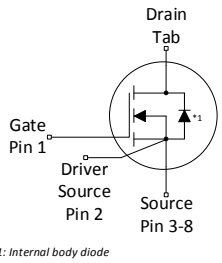
TOLL




Built on Infineon's robust 2nd generation Silicon Carbide trench technology, the 650 V CoolSiC™ MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.

## Features

- Ultra-low switching losses
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.5 V
- Robust against parasitic turn-on even with 0 V turn-off gate voltage
- Flexible driving voltage and compatible with bipolar driving scheme
- Robust body diode operation under hard commutation events
- .XT interconnection technology for best-in-class thermal performance




*1: Internal body diode

## Benefits

- Enables high efficiency and high power density designs
- Facilitates great ease of use and integration
- Provides the best price performance ratio compared to Industry's most ambitious roadmaps
- Reduces the size, weight and bill of materials of the systems
- Enhances system robustness and reliability

## Potential applications

- SMPS
- Solar PV inverters
- Energy storage and battery formation
- UPS
- EV charging infrastructure
- Motor drives

## Product validation

Fully qualified according to JEDEC for Industrial Applications

*Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.*

**Table 1 Key performance parameters**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DSS}$ over full $T_{j,range}$ | 650 | V |
| $R_{DS(on),typ}$ | 14.5 | mΩ |
| $R_{DS(on),max}$ | 18 | mΩ |
| $Q_{G,typ}$ | 79 | nC |
| $I_{D,pulse}$ | 400 | A |
| $Q_{oss}$ @ 400 V | 148 | nC |
| $E_{oss}$ @ 400 V | 20.1 | µJ |

| Part number | Package | Marking | Related links |
|---|---|---|---|
| IMT65R015M2H | PG-HSOF-8 | 65R015M2 | see Appendix A |

# Table of contents

# 1 Maximum ratings

at $T_j$ = 25°C, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

**Table 2 Maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous DC drain current [1] | $I_{DDC}$ | - | - | 131<br>95 | A | $T_c$ = 25°C<br>$T_c$ = 100°C |
| Peak drain current [2] | $I_{DM}$ | - | - | 400 | A | $T_c$ = 25°C, $V_{GS}$ = 18 V |
| Avalanche energy, single pulse | $E_{AS}$ | - | - | 372 | mJ | $I_D$ = 13.9 A, $V_{DD}$ = 50 V; see table 11 |
| Avalanche energy, repetitive | $E_{AR}$ | - | - | 1.86 | mJ | |
| Avalanche current, single pulse | $I_{AS}$ | - | - | 13.9 | A | - |
| MOSFET *dv/dt* ruggedness | *dv/dt* | - | - | 200 | V/ns | $V_{DS}$= 0...400 V |
| Gate source voltage (static) [3] | $V_{GS}$ | -7 | - | 23 | V | - |
| Gate source voltage (transient) | $V_{GS}$ | -10 | - | 25 | V | $t_p$ ≤ 500 ns, duty cycle ≤ 1% |
| Power dissipation | $P_{tot}$ | - | - | 535 | W | $T_c$ = 25°C |
| Storage temperature | $T_{stg}$ | -55 | - | 150 | °C | - |
| Operating junction temperature | $T_j$ | -55 | - | 175 | °C | |
| Mounting torque | - | - | - | n.a. | Ncm | |
| Continuous reverse drain current [1] | $I_{SDC}$ | - | - | 131<br>92 | A | $V_{GS}$ = 18 V, $T_c$ = 25°C<br>$V_{GS}$ = 0 V, $T_c$ = 25°C |
| Peak reverse drain current [2] | $I_{SM}$ | - | - | 400<br>121 | A | $T_c$ = 25°C, $t_p$ ≤ 250 ns<br>$T_c$ = 25°C |
| Insulation withstand voltage | $V_{ISO}$ | - | - | n.a. | V | $V_{rms}$, $T_c$ = 25°C, $t$ = 1 min |

1) Limited by $T_{j,max}$.

2) Pulse width $t_{pulse}$ limited by $T_{j,max}$.

3) The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

# 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{th(j-c)}$ | - | - | 0.28 | °C/W | Not subject to production test. Parameter verified by design/characterization according to JESD51-14. |
| Soldering temperature, reflow soldering allowed | $T_{sold}$ | - | - | 260 | °C | reflow MSL3 |

# 3 Operating range

**Table 4 Operating range**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Recommended turn-on voltage | $V_{GS(on)}$ | - | 18 | - | V | - |
| Recommended turn-off voltage | $V_{GS(off)}$ | - | 0 | - | V | |

# 4 Electrical characteristics

at $T_j$ = 25°C, unless otherwise specified

**Table 5 Static characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source voltage | $V_{DSS}$ | 650 | - | - | V | $V_{GS}$ = 0 V, $I_D$ = 1.3 mA |
| Gate threshold voltage [4] | $V_{GS(th)}$ | 3.5 | 4.5 | 5.6 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 13 mA |
| Zero gate voltage drain current | $I_{DSS}$ | - | 1<br>3 | 75<br>- | µA | $V_{DS}$ = 650 V, $V_{GS}$ = 0 V, $T_j$ = 25°C<br>$V_{DS}$ = 650 V, $V_{GS}$ = 0 V, $T_j$ = 175°C |
| Gate-source leakage current | $I_{GSS}$ | - | - | 100 | nA | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 19<br>14.5<br>13.2<br>24 | -<br>18<br>-<br>- | mΩ | $V_{GS}$ = 15 V, $I_D$ = 64.2 A, $T_j$ = 25°C<br>$V_{GS}$ = 18 V, $I_D$ = 64.2 A, $T_j$ = 25°C<br>$V_{GS}$ = 20 V, $I_D$ = 64.2 A, $T_j$ = 25°C<br>$V_{GS}$ = 18 V, $I_D$ = 64.2 A, $T_j$ =175°C |
| Internal gate resistance | $R_{G,int}$ | - | 2.1 | - | Ω | $f$ = 1 MHz |

[4] Tested after 1 ms pulse at $V_{GS}$ = +20 V. “Linear mode” operation is not recommended. For assessment of potential “linear mode” operation, please contact Infineon sales office.

**Table 6 Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 2792 | - | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 400 V, $f$ = 250 kHz |
| Reverse transfer capacitance | $C_{rss}$ | - | 16 | - | pF | |
| Output capacitance [5] | $C_{oss}$ | - | 207 | 269 | pF | |
| Output charge [5] | $Q_{oss}$ | - | 148 | 192 | nC | calculation based on $C_{oss}$ |
| Effective output capacitance, energy related [6] | $C_{o(er)}$ | - | 251 | - | pF | $V_{GS}$ = 0 V,<br>$V_{DS}$ = 0...400 V |
| Effective output capacitance, time related [7] | $C_{o(tr)}$ | - | 371 | - | pF | $I_D$ = constant, $V_{GS}$ = 0 V, $V_{DS}$ = 0... 400 V |
| Turn-on delay time | $t_{d(on)}$ | - | 11.6 | - | ns | $V_{DD}$ = 400 V, $V_{GS}$ = 0/18 V, $I_D$ = 64.2 A, $R_{G,ext}$ = 1.8 Ω; see table 10 |
| Rise time | $t_r$ | - | 14.7 | - | ns | |
| Turn-off delay time | $t_{d(off)}$ | - | 22 | - | ns | |
| Fall time | $t_f$ | - | 6.4 | - | ns | |

### Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Turn-ON switching losses [8] | $E_{on}$ | - | 84 | - | µJ | $V_{DD}$ = 400 V, $V_{GS}$ = 0/18 V, $I_D$ = 64.2 A, $R_{G,ext}$ = 1.8 Ω |
| Turn-OFF switching losses [8] | $E_{off}$ | - | 138 | - | µJ | |
| Total switching losses [8] | $E_{tot}$ | - | 222 | - | µJ | |

[5] Maximum specification is defined by calculated six sigma upper confidence bound.

[6] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 400 V.

[7] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 400 V.

[8] Values for 4-pin configuration based on TO-263-7 measurements; MOSFET used in half-bridge configuration without external diode.

### Table 7 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Plateau gate to source charge | $Q_{GS(pl)}$ | - | 20 | - | nC | $V_{DD}$ = 400 V, $I_D$ = 64.2 A, $V_{GS}$ = 0 to 18 V |
| Gate to drain charge | $Q_{GD}$ | - | 15 | - | nC | |
| Total gate charge | $Q_G$ | - | 79 | - | nC | |

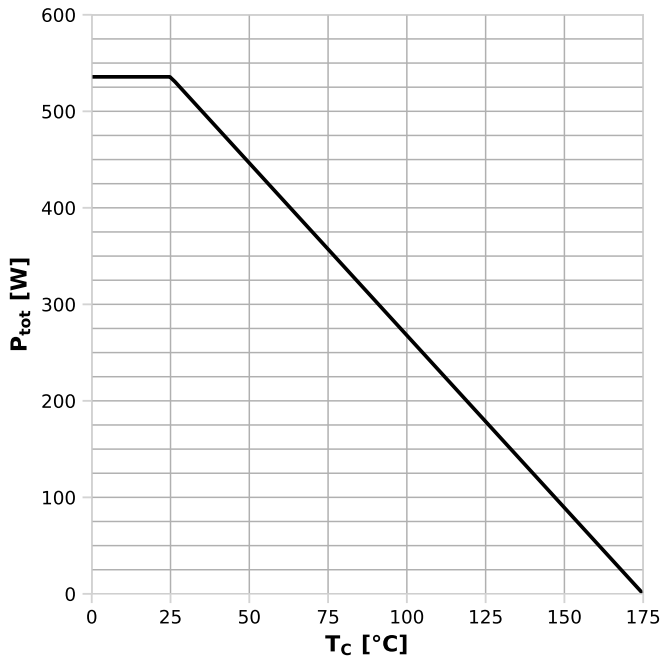
### Table 8 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source reverse voltage | $V_{SD}$ | - | 4.3 | - | V | $V_{GS}$ = 0 V, $I_S$ = 64.2 A, $T_j$ = 25°C |
| MOSFET forward recovery time | $t_{fr}$ | - | 22<br>16 | - | ns | $V_{DD}$ = 400 V, $I_S$ = 64.2 A, $di_S/dt$ = 1000 A/µs; see table 9<br>$V_{DD}$ = 400 V, $I_S$ = 64.2 A, $di_S/dt$ = 4000 A/µs; see table 9 |
| MOSFET forward recovery charge [9] | $Q_{fr}$ | - | 154<br>258 | - | nC | $V_{DD}$ = 400 V, $I_S$ = 64.2 A, $di_S/dt$ = 1000 A/µs; see table 9<br>$V_{DD}$ = 400 V, $I_S$ = 64.2 A, $di_S/dt$ = 4000 A/µs; see table 9 |
| MOSFET peak forward recovery current | $I_{frm}$ | - | 14.3<br>32 | - | A | $V_{DD}$ = 400 V, $I_S$ = 64.2 A, $di_S/dt$ = 1000 A/µs; see table 9<br>$V_{DD}$ = 400 V, $I_S$ = 64.2 A, $di_S/dt$ = 4000 A/µs; see table 9 |

[9] $Q_{fr}$ includes $Q_{oss}$.

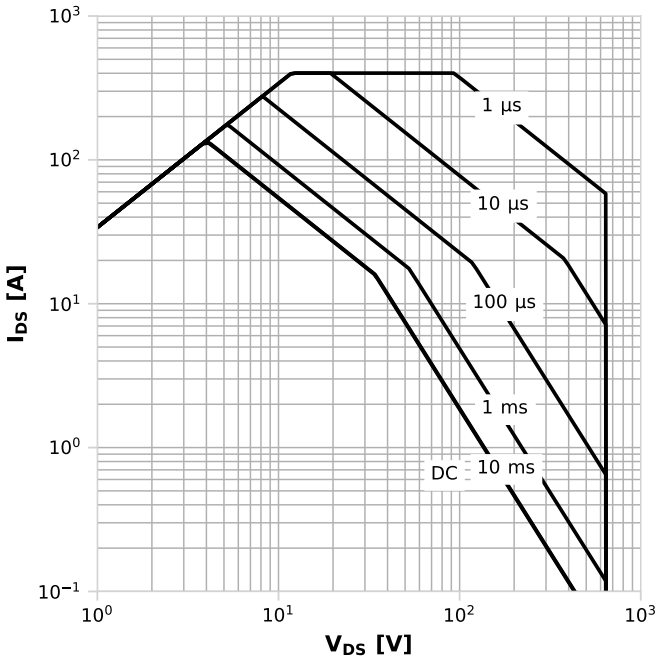
# 5 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



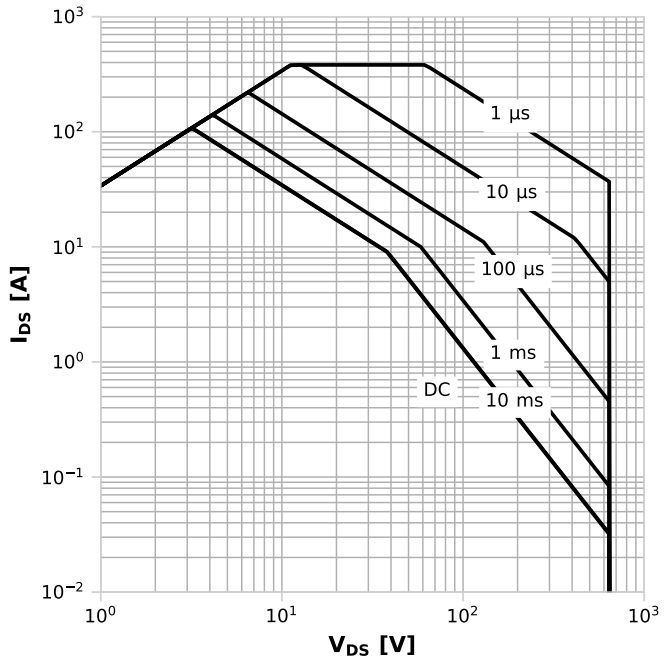

$P_{tot}=f(T_C)$

**Diagram 2: Safe operating area**



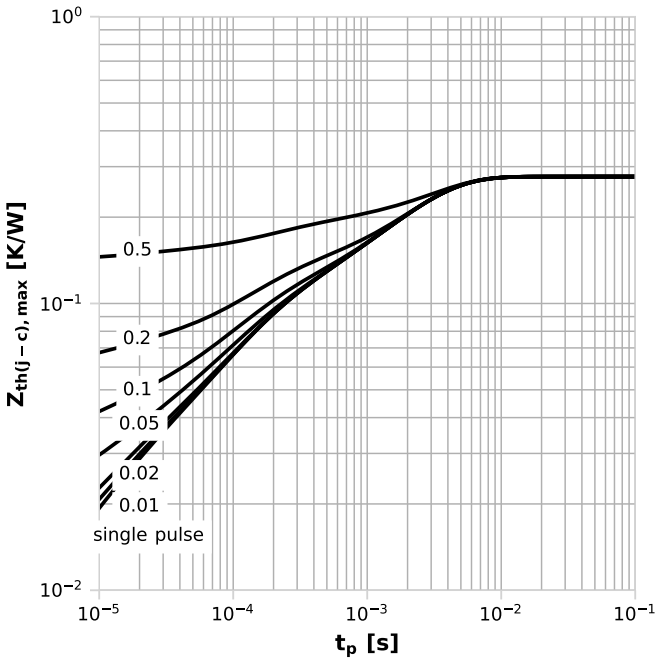

$I_{DS}=f(V_{DS})$; $T_C$=25 °C; D=0; parameter: $t_p$

**Diagram 3: Safe operating area**

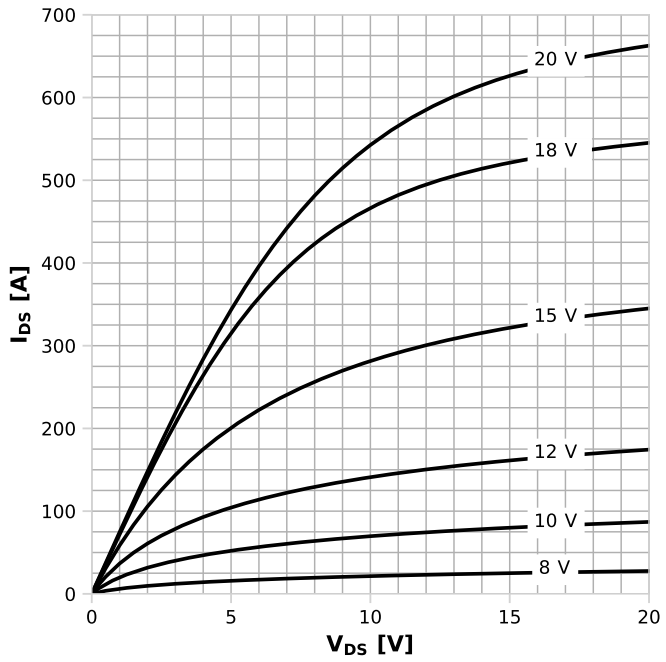
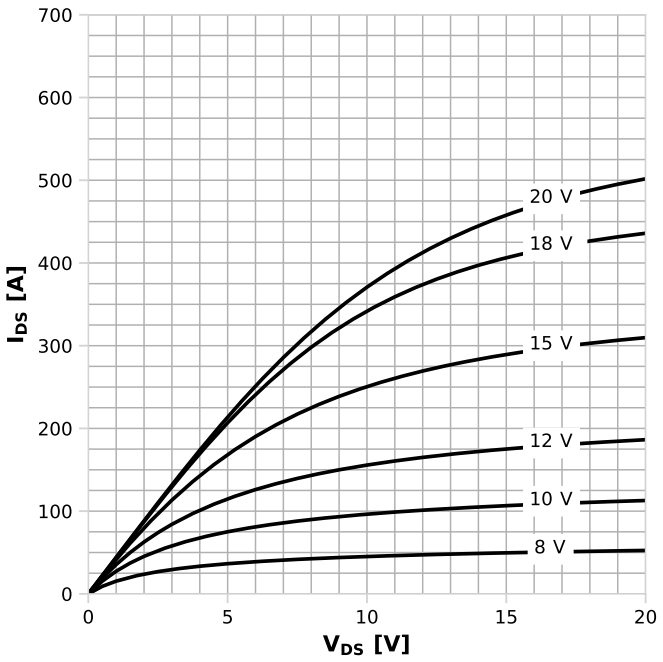


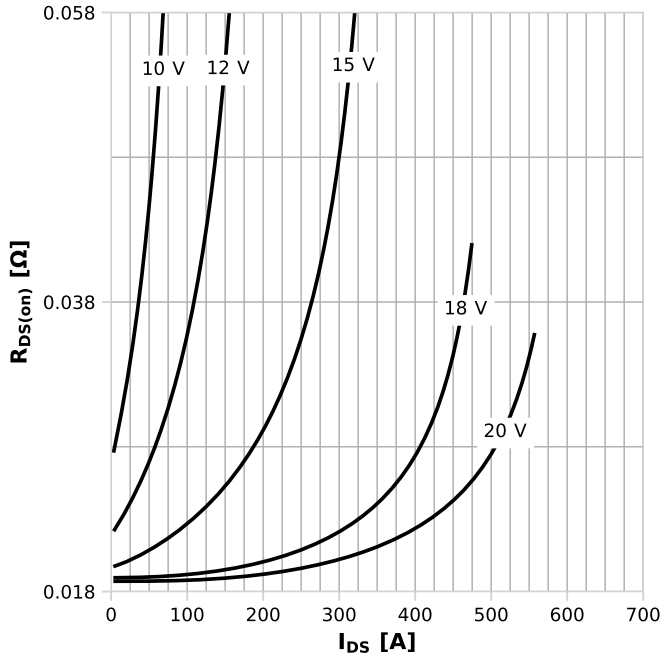
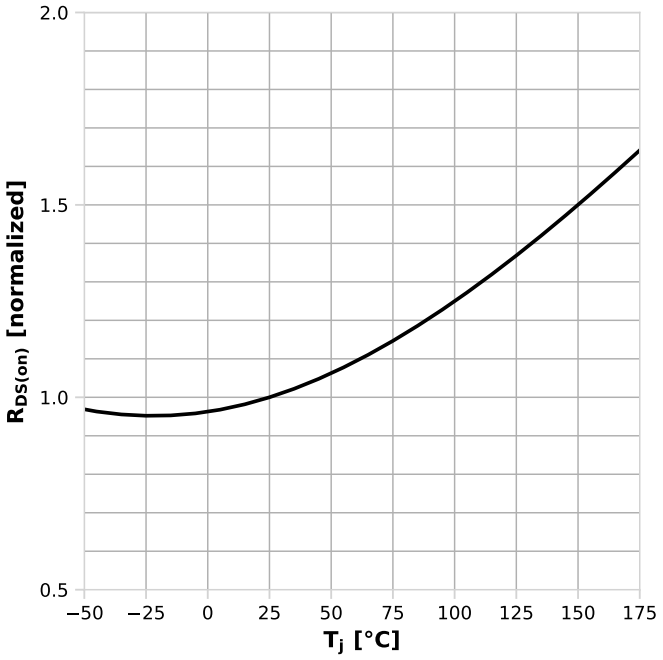

$I_{DS}=f(V_{DS})$; $T_C$=80 °C; D=0; parameter: $t_p$

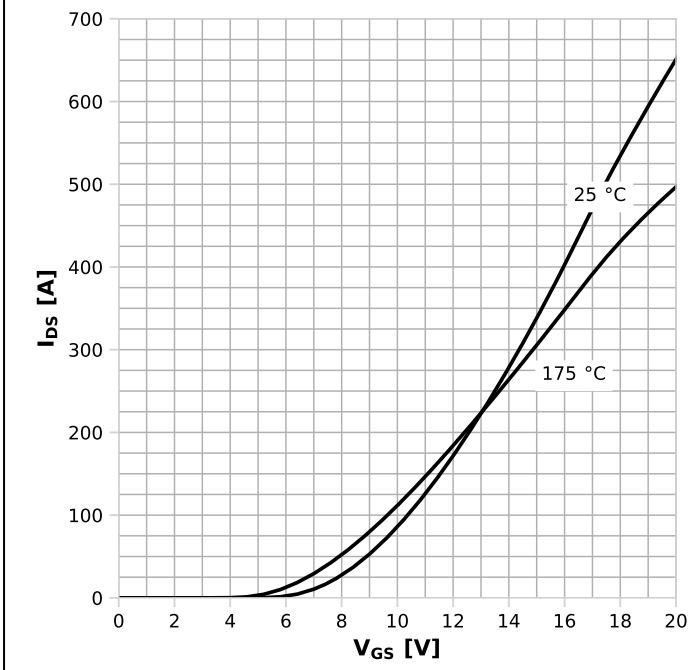
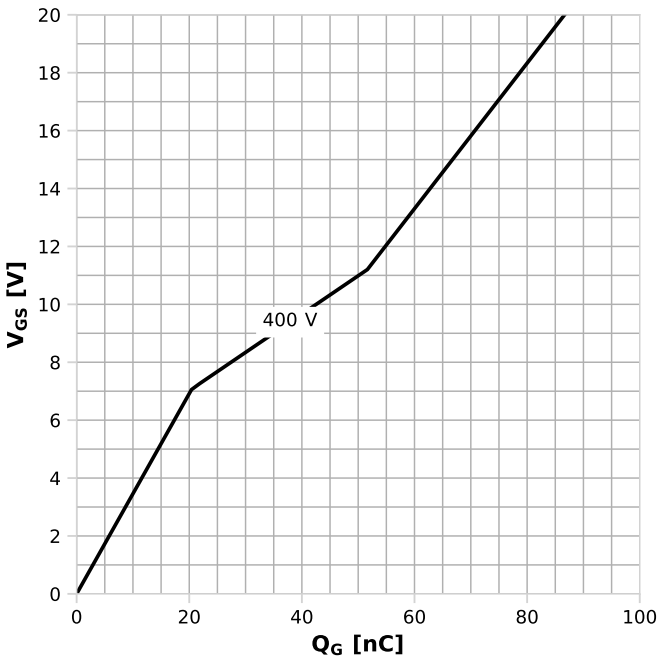
**Diagram 4: Max. transient thermal impedance**

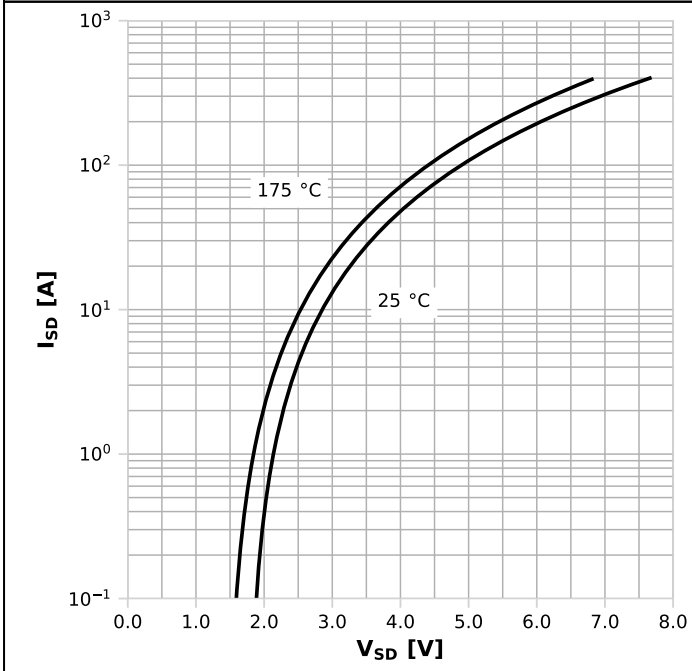
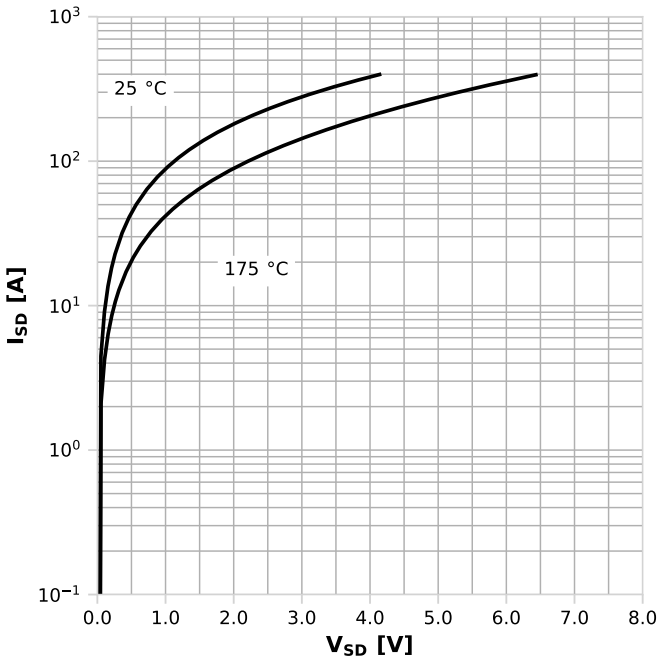


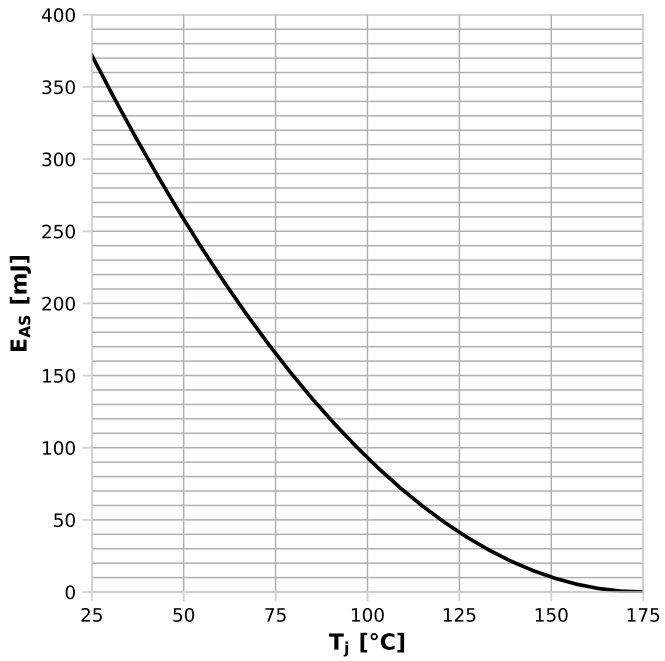
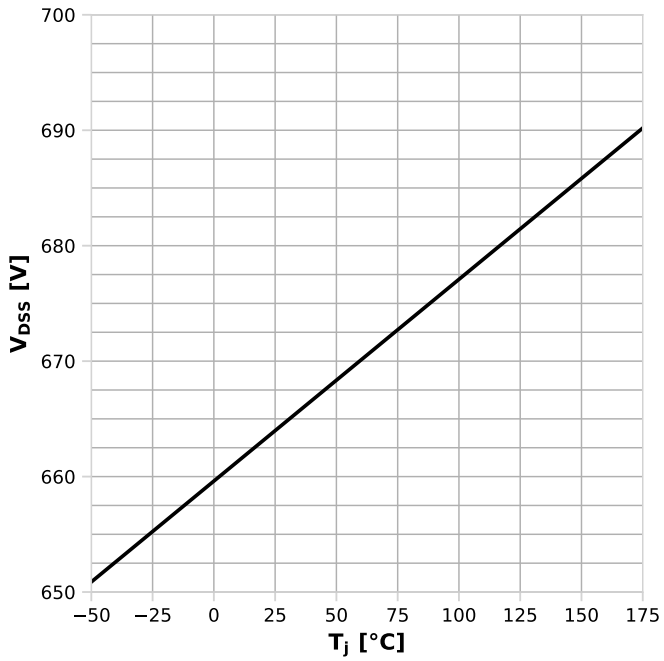

$Z_{th(j-c),max}=f(t_P)$; parameter: $D=t_p/T$

| Diagram 5: Typ. output characteristics | Diagram 6: Typ. output characteristics |
|---|---|
|  |  |
| $I_{DS}=f(V_{DS})$; $T_j=25$ °C; parameter: $V_{GS}$ | $I_{DS}=f(V_{DS})$; $T_j=175$ °C; parameter: $V_{GS}$ |

| Diagram 7: Typ. drain-source on-state resistance | Diagram 8: Drain-source on-state resistance |
|---|---|
|  |  |
| $R_{DS(on)}=f(I_{DS})$; $T_j=125$ °C; parameter: $V_{GS}$ | $R_{DS(on)}=f(T_j)$; $I_D=64.2$ A; $V_{GS}=18$ V |

| Diagram 9: Typ. transfer characteristics | Diagram 10: Typ. gate charge |
|---|---|
|  |  |
| $I_{DS}=f(V_{GS})$; $V_{DS}=20$ V; parameter: $T_j$ | $V_{GS}=f(Q_G)$; $I_D=64.2$ A pulsed; parameter: $V_{DD}$ |

| Diagram 11: Typ. reverse drain current characteristics | Diagram 12: Typ. reverse drain current characteristics |
|---|---|
|  |  |
| $I_{SD}=f(V_{SD})$; $V_{GS}=0$ V; parameter: $T_j$ | $I_{SD}=f(V_{SD})$; $V_{GS}=18$ V; parameter: $T_j$ |

| Diagram 13: Avalanche energy | Diagram 14: Drain-source breakdown voltage |
|---|---|
|  |  |
| $E_{AS}=f(T_j)$; $I_D$=13.9 A; $V_{DD}$=50 V | $V_{DSS}=f(T_j)$; $I_D$=1.3 mA |

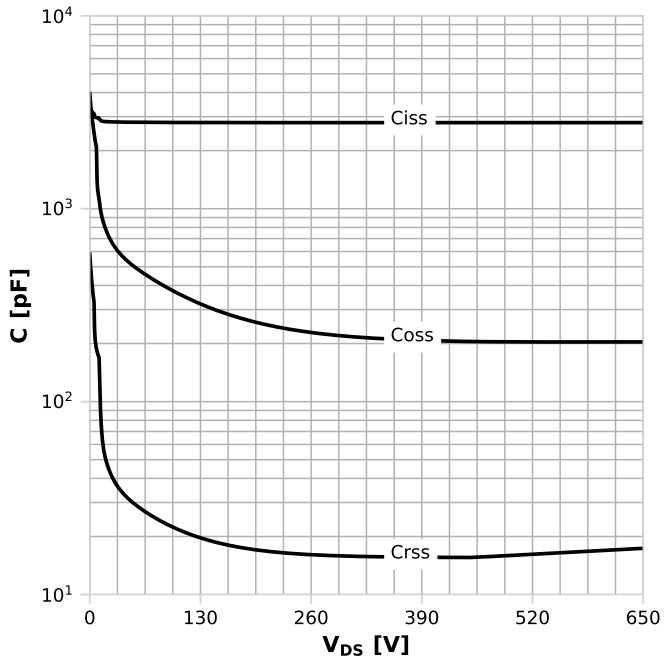
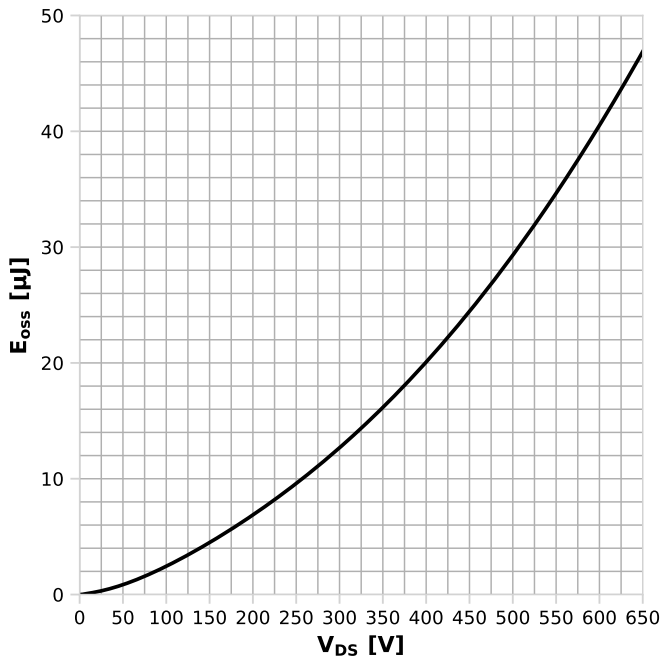
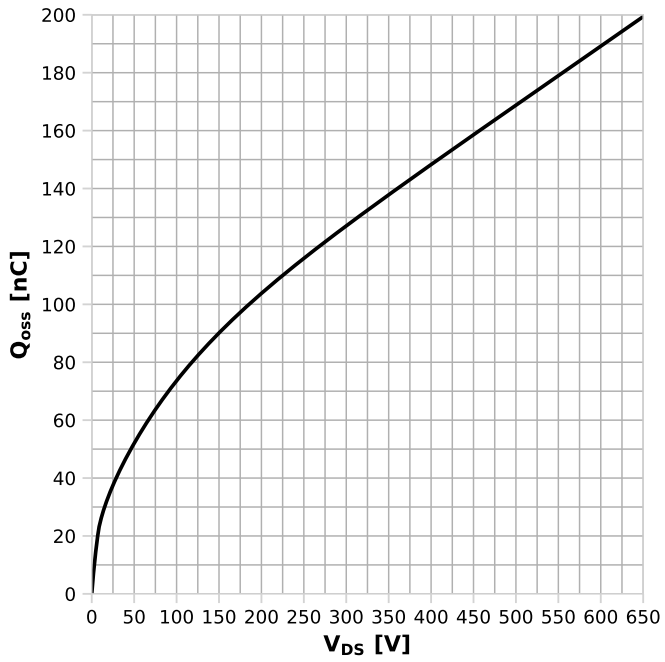
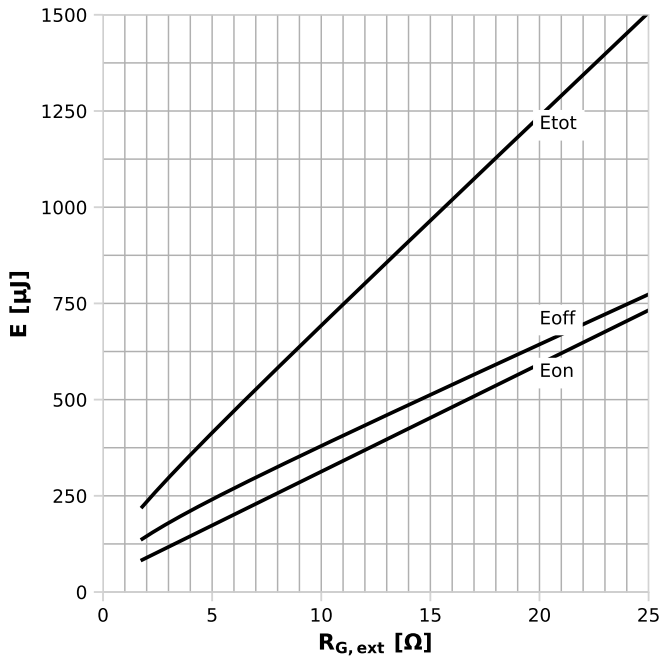
| Diagram 15: Typ. capacitances | Diagram 16: Typ. Coss stored energy |
|---|---|
|  |  |
| $C=f(V_{DS})$; $V_{GS}$=0 V; f=250 kHz | $E_{oss}=f(V_{DS})$ |

**Diagram 17: Typ. Qoss output charge**



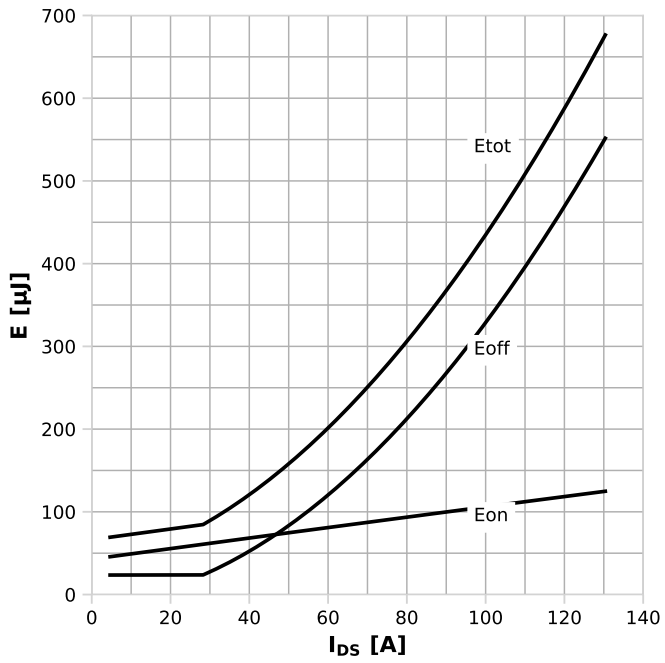

$Q_{oss}=f(V_{DS})$

**Diagram 18: Typ. Switching Losses vs $R_{G,ext}$**




$E=f(R_{G,ext})$; $V_{DD}$=400 V; $V_{GS}$=0/18 V; $I_D$=64.2 A

**Diagram 19: Typ. Switching Losses vs switching current**




$E=f(I_{DS})$; $V_{DD}$=400 V; $V_{GS}$=0/18 V; $R_{G,ext}$=1.8 Ω

# 6 Test circuits

**Table 9 Body diode characteristics**

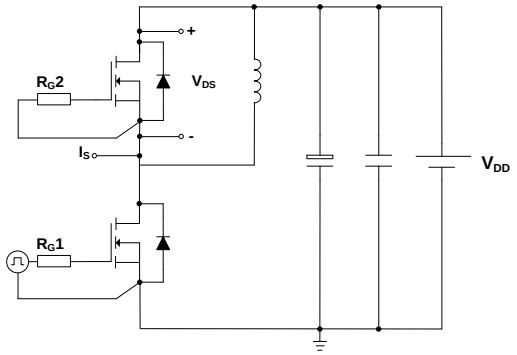
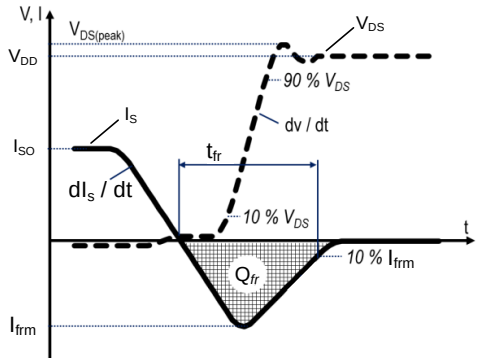
| Test circuit for body diode characteristics | Body diode recovery waveform |
|---|---|
|  |  |



**Table 10 Switching times**

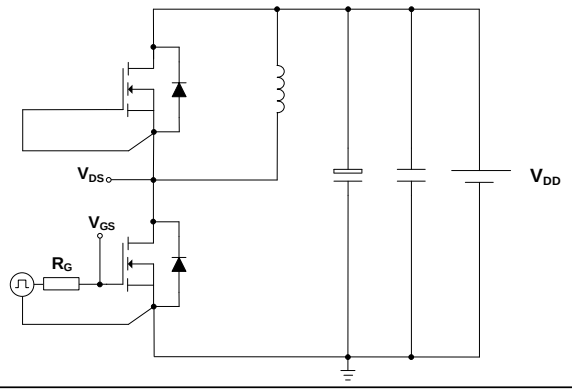
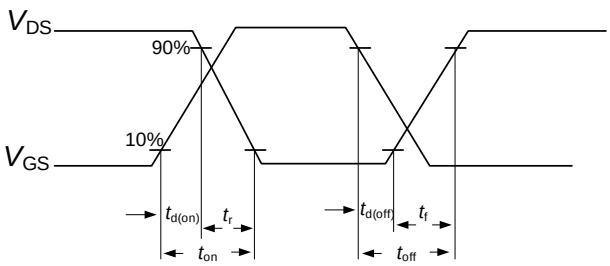
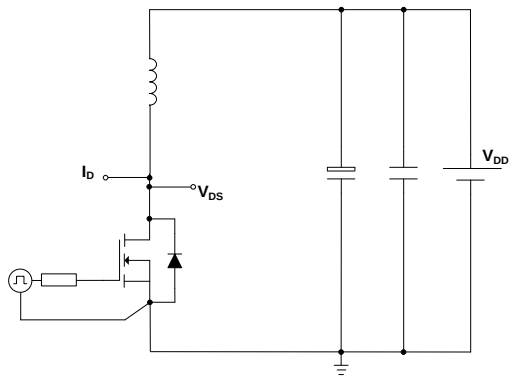
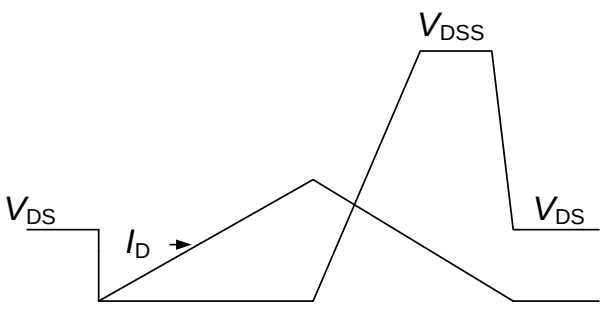
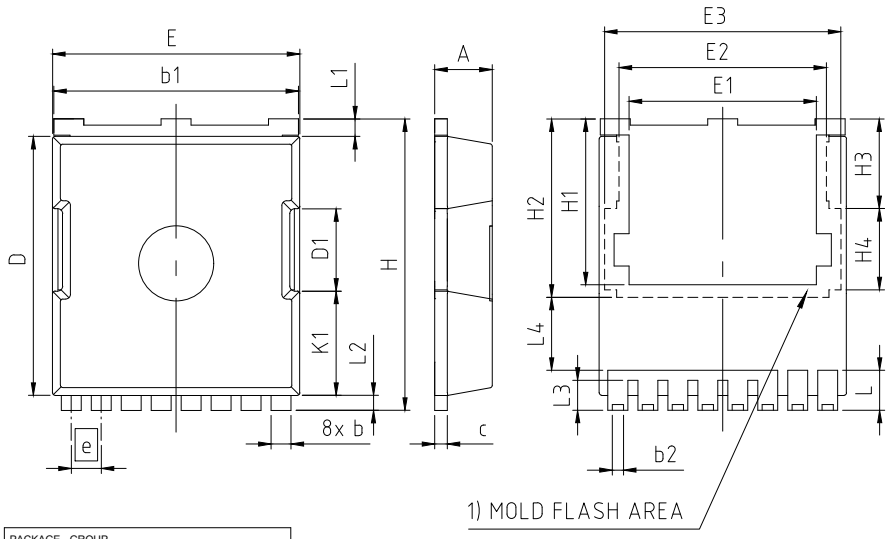
| Switching times test circuit for inductive load | Switching times waveform |
|---|---|
|  |  |



**Table 11 Unclamped inductive load**

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---|---|
|  |  |

# 7 Package outlines




| PACKAGE - GROUP NUMBER: | PG-HSOF-8-U02 | |
|---|---|---|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 2.20 | 2.40 |
| b | 0.70 | 0.90 |
| b1 | 9.70 | 9.90 |
| b2 | 0.42 | 0.50 |
| c | 0.40 | 0.60 |
| D | 10.28 | 10.58 |
| D1 | 3.30 | |
| E | 9.70 | 10.10 |
| E1 | 7.50 | |
| E2 | 8.50 | |
| E3 | 9.46 | |
| e | 1.20 (BSC) | |
| H | 11.48 | 11.88 |
| H1 | 6.55 | 6.95 |
| H2 | 7.15 | |
| H3 | 3.59 | |
| H4 | 3.26 | |
| N | 8 | |
| K1 | 4.18 | |
| L | 1.40 | 1.80 |
| L1 | 0.50 | 0.90 |
| L2 | 0.50 | 0.70 |
| L3 | 1.00 | 1.30 |
| L4 | 2.62 | 2.81 |

1) PARTIALLY COVERED WITH MOLD FLASH

**Figure 1 Outline PG-HSOF-8, dimensions in mm**

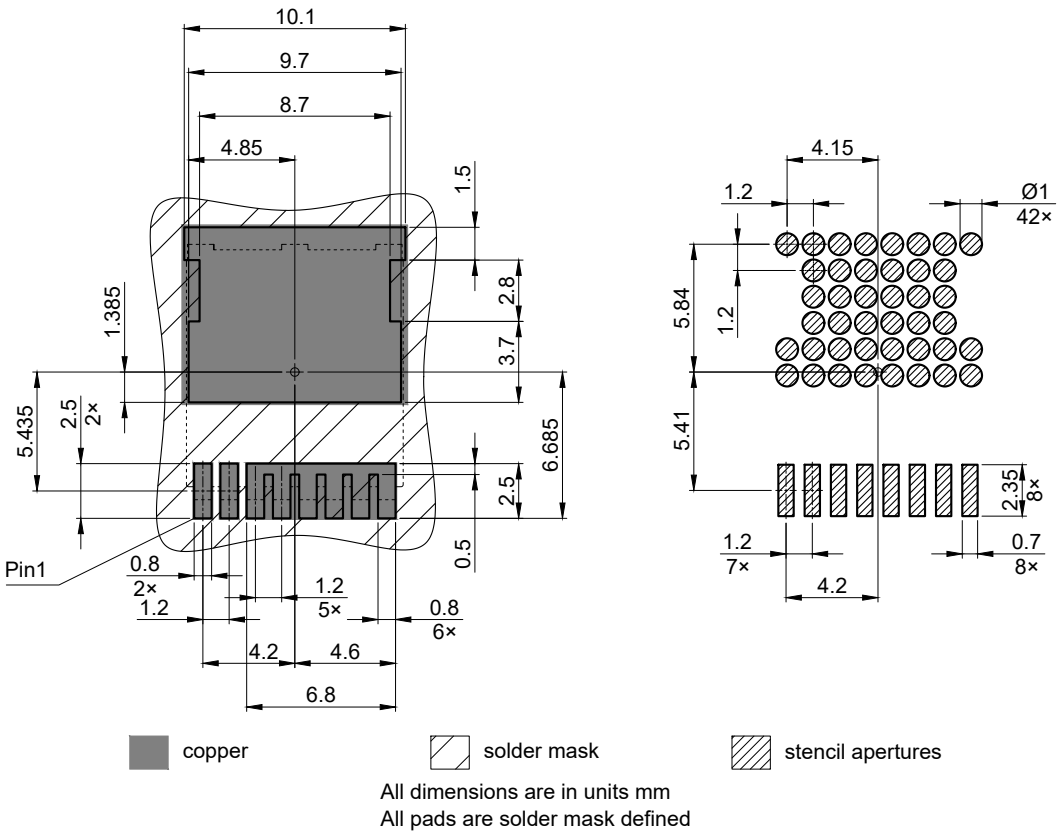



**Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm**

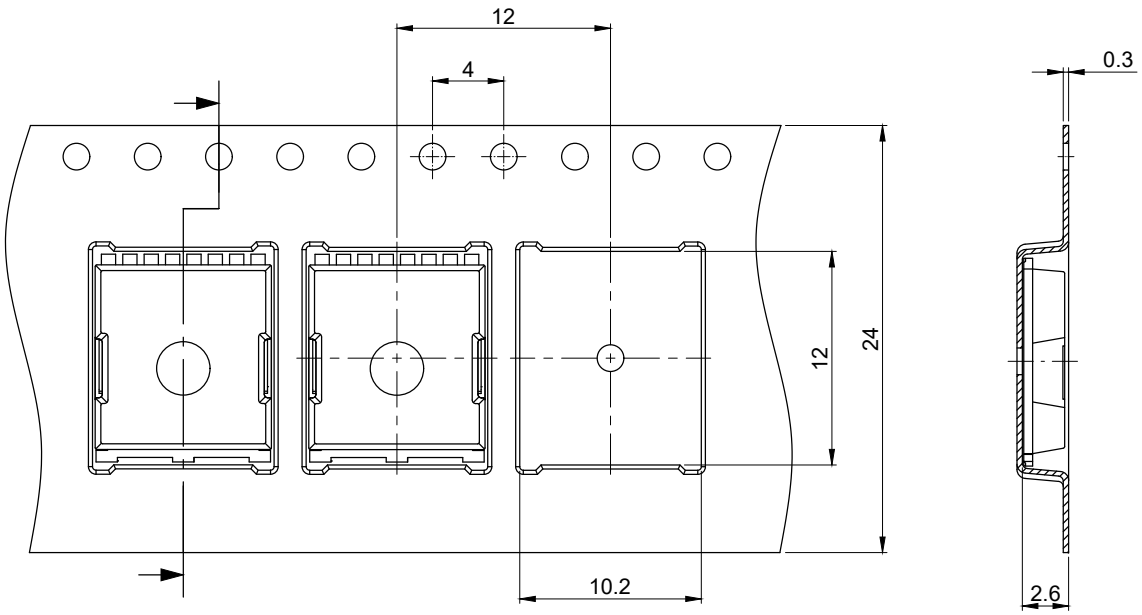



**Figure 3 Packaging variant PG-HSOF-8, dimensions in mm**

# 8 Appendix A

**Table 12 Related links**

- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Webpage
- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Application Note
- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Simulation Model
- IFX Design tools

## Revision history

IMT65R015M2H

### Revision 2025-01-16, Rev. 2.1

Previous revisions

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 2.0 | 2024-11-06 | Release of final |
| 2.1 | 2025-01-16 | updated continuous reverse drain current |



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