IN25AA080N, IN25AA080D, IN25AA160N, IN25AA160D

NONVOLATILE ELECTRICALLY ERASABLE PROM WITH SERIAL PERIPHERAL INTERFACE (SPI).

functionally compartible to 25AA080, 25AA160 (Microchip)

DESCRIPTION

The IN25AA080N/D are a 8K(1Kx8) serial Electrically Erasable PROM with SPI interface.
·The IN25AA160N/D are a 16K (2Kx8) serial Electrically Erasable PROM with SPI interface (SPI).
The ICs is purposed for reading, writing & nonvolatile data storage in electronic units with SPI interface. ICs are realized in SO-8 (MS-012AA) and DIP-8 (MS-001BA)

FEATURES

- Data capacity, Q_{INF}:
for IN25AA080N, IN25AA080D .... 8192 bit,
for IN25AA160N, IN25AA160D .... 16384 bit;
- Maximum clock frequency, f_C:
for $4,5\ V \le U_{CC} \le 5,5\ V$ .... 3 MHz;
for $2,5\ V \le U_{CC} \le 5,5\ V$ .... 2 MHz;
for $1,8\ V \le U_{CC} \le 5,5\ V$ .... 1 MHz;
- Maximum stand-by current, I_{CC}:
  for $U_{CC} = 5,5\ V$, $U_{IL} = 0\ V$, $U_{IH} = U_{CC}$ .... 5,0 uA
for $U_{CC} = 2,5\ V$, $U_{IL} = 0\ V$, $U_{IH} = U_{CC}$ .... 1,0 uA;
- Maximum read current, I_{OCCR} :

for $U_{CC} = 5,5\ B$, $f_C = 3,0$ МГц, SO pin is not loaded ....1,0 mA,
for $U_{CC} = 2,5\ B$, $f_C = 2,0$ МГц, SO pin is not loaded .....0,5 mA;
- Maximum write current, I_{OCCW} :
for $U_{CC} = 5,5\ V$ .... 5,0 mA;
for $U_{CC} = 2,5\ V$ .... 3,0 mA;
- Byte & page (16 bytes) data write modes are available;
- Endurance $N_{E/W}$, …...1000000 cycles;
- Build-in write protection block
- Write protection for 1/4, 1/2, or all of storage array;
- Power on/off data protection circuitry;
- Supply voltage U_{CC} 1,8 … 5,5 V;
- Operating temperature range -40 … +85°C.
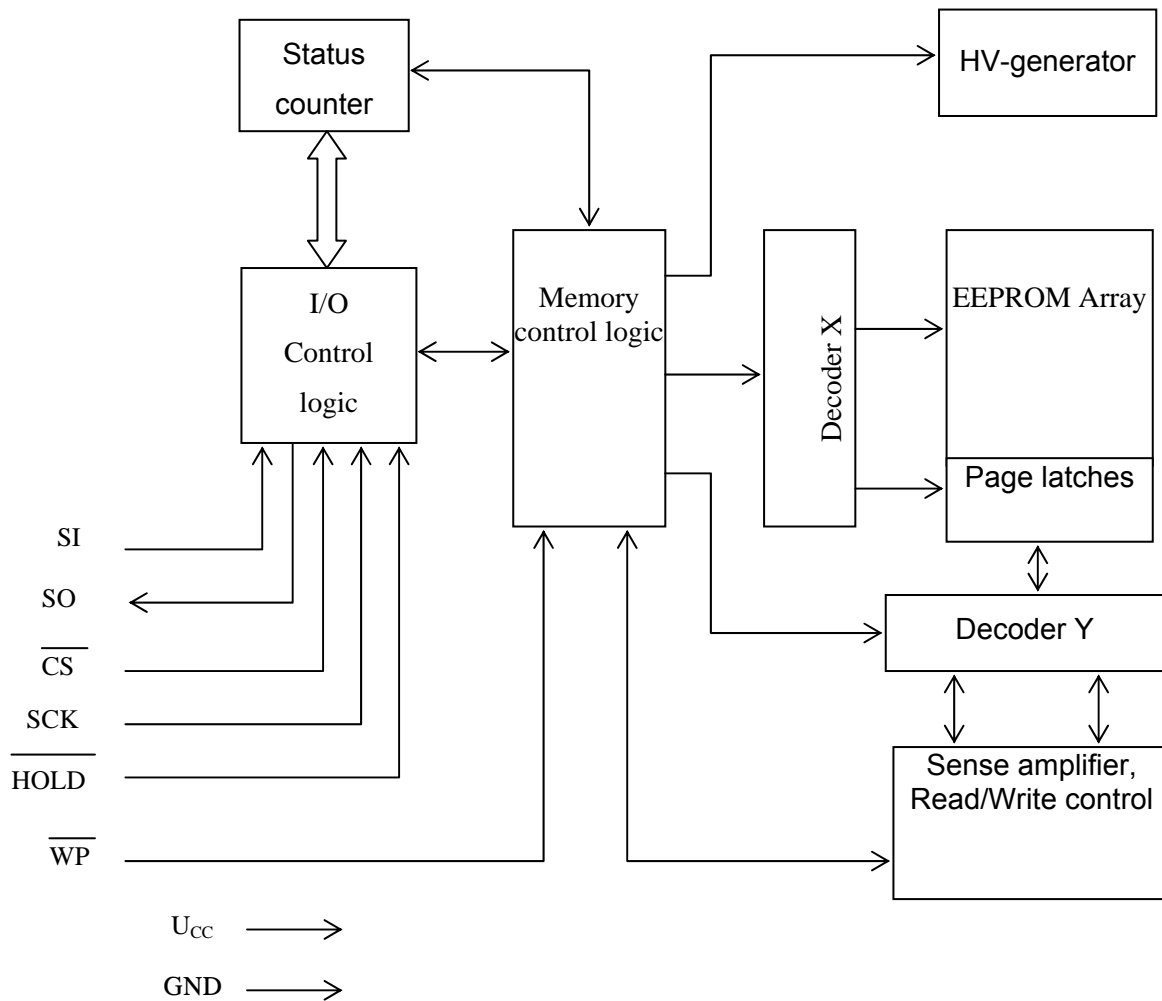- 100 years non-volatile data retention time
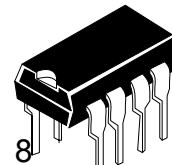
N SUFFIX
DIP
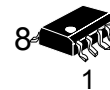
D SUFFIX
SOIC

PIN FUNCTIONS

Pin Name	Function
$\overline{CS}$	Chip Select
SO	Serial Data Output
$\overline{WP}$	Write protection
GND	Ground
SI	Serial Data Input
SCK	Clock Input
$\overline{HOLD}$	Hold input *
V_{CC}	Power Supply

$\overline{CS}$	01	08 Vcc
SO	02	07 $\overline{HOLD}$
$\overline{WP}$	03	06 SCK
GND	04	05 SI

INTEGRAL

Block Diagram

Recommended Operation Conditions & Maximum Ratings*

Parameter, unit		Symbol	Recommended Operation Conditions		Maximum Ratings	
			Min	Max	Min	Max
Supply voltage,V		U_{cc}	1,8	5,5	-0,6	7,0
High level input voltage, V	$2,7\ V \leq U_{cc} \leq 5,5\ V$	U_{IH}	2,0	$U_{cc} + 1,0$	–	$U_{cc} + 1,0$
	$1,8\ V \leq U_{cc} < 2,7\ V$		$0,7U_{cc}$	$U_{cc} + 1,0$		
Low level input voltage, V	$2,7\ V \leq U_{cc} \leq 5,5\ V$	U_{IL}	-0,3	0,8	- 0,6	-
	$1,8\ V \leq U_{cc} < 2,7\ V$		-0,3	$0,3U_{CC}$		
Ambient temperature		T_A	-40	85	-60	150

ESD protection 2000 V.

Input capacity C_I, output capacity C_O have to be not more than 7pF for U_{CC} = 5,0 V & T_A= (25±10) °C.

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Electric Parameters ($-40^oC \le T_A \le 85^oC$

Parameter, unit	Symbol	Mode	Min	Max	T_A, °C
Low level output voltage, V	U_{OL}	$2,5\ V \le U_{CC} \le 5,5\ V$ $I_{OL} = 2,1\ mA$	–	0,4	25 ± 10; -45; 85
		$1,8\ V \le U_{CC} \le 2,5\ V$ $I_{OL} = 1,0\ mA$	-	0,2	
High level output voltage, V	U_{OH}	$U_{CC} = 1,8\ V$ $I_{OH} = -400\ uA$	1,3	–	
		$U_{CC} = 5,5\ V$ $I_{OH} = -400\ uA$	5,0	–	
Low level input leakage current, uA	I_{ILL}	$U_I = 0\ V$	–	-10,0	
High level input leakage current, uA	I_{ILH}	$U_I = 5,5V$	-	10,0	
Low level output leakage current, uA	I_{OLL}	$U_I = 0\ V$	-	-10,0	
High level output leakage current, uA	I_{OLH}	$U_I = 5,5V$	–	10,0	
Consumption current, uA	I_{CC}	$Ucc = 5,5\ V, U_{IL} = 0\ V$ $U_{IH} = Ucc$	–	5,0	
		$Ucc = 2,5\ V, U_{IL} = 0\ V$ $U_{IH} = Ucc$	–	1,0	
Consumption current (Operating Read), uA	$I_{OCC\ R}$	$Ucc = 5,5\ V, f_C = 3\ MHz$ SO pin is not loaded	–	1,0	
		$Ucc = 2,5\ V, f_C = 2\ MHz$ SO pin is not loaded		0,5	
Consumption current (Operating Write), uA	$I_{OCC\ W}$	$Ucc = 5,5\ V, f_C = 3\ MHz$	–	5,0	
		$Ucc = 2,5\ V, f_C = 2\ MHz$		3,0	
Data access time on SCK transition to low level, ns	t_V	$4,5\ V \le U_{CC} \le 5,5\ V,$ $f_C \le 3\ MHz$	-	150	25±10 –40 85
		$2,5\ V \le U_{CC} < 4,5\ V,$ $f_C \le 2\ MHz$	-	230	
		$1,8\ V \le U_{CC} < 2,5\ V,$ $f_C \le 1\ MHz$	-	475	
Output disable time on $\overline{CS}$ high, ns	t_{DIS}	$4,5\ V \le U_{CC} \le 5,5\ V,$ $f_C \le 3\ MHz$	-	200	
		$2,5\ V \le U_{CC} < 4,5\ V,$ $f_C \le 2\ MHz$	-	250	
		$1,8\ V \le U_{CC} < 2,5\ V,$ $f_C \le 1\ MHz$	-	500	
Output disable time on $\overline{HOLD}$ low, ns	t_{HZ}	$4,5\ V \le U_{CC} \le 5,5\ V,$ $f_C \le 3\ MHz$	100	-	
		$2,5\ V \le U_{CC} < 4,5\ V,$ $f_C \le 2\ MHz$	150	-	
		$1,8\ V \le U_{CC} < 2,5\ V,$ $f_C \le 1\ MHz$	200	-	
Output enable time on $\overline{HOLD}$ high, ns	t_{HV}	$4,5\ V \le U_{CC} \le 5,5\ V,$ $f_C \le 3\ MHz$	100	-	
		$2,5\ V \le U_{CC} < 4,5\ V,$ $f_C \le 2\ MHz$	150	-	
		$1,8\ V \le U_{CC} < 2,5\ V,$ $f_C \le 1\ MHz$	200	-	
Write/Erase cycle, ms	t_{CY}	$U_{CC} = 4,5\ V, f_C = 3\ MHz$	–	5	
Program/erase cycles	$N_{E/W}$	$Ucc = 5,0\ V$	1000000	–	

Instruction Set

Instruction	Instruction Format	Description
READ	0000 X011	Read data from memory array beginning at selected address
WRITE	0000 X010	Write data to memory array beginning at selected address
WRDI	0000 X100	Reset the write enable latch (disable write operations)
WREN	0000 X110	Set the write enable latch (enable write operations)
RDSR	0000 X101	Read status register
WRSR	0000 X001	Write status register
Notes 1 X – Any level (low or high).		

SPI parameters (-40 °C ≤ Ta ≤ 85 °C)

Symbol	Parameter, unit	Mode	$1{,}8\,V \le U_{CC} < 2{,}5\,V$		$2{,}5\,V \le U_{CC} < 4{,}5\,V$		$4{,}5\,V \le U_{CC} \le 5{,}5\,V$	
			Min	Max	Min	Max	Min	Max
f_C	Clock frequency, MHz	$C_L = 100\,pF$	-	1	-	2	-	3
t_{CSS}	CS setup time, ns		500	-	250	-	100	-
t_{CSH}	CS hold time, ns		475	-	250	-	150	-
t_{SU}	SI setup time, ns		50	-	50	-	30	-
t_{HD}	SI hold time, ns		100	-	100	-	50	-
t_{CSD}	Disable time on $\overline{CS}$, ns		Not less 500					
t_R	SCK rise time, us		Not more 2					
t_F	SCK fall time, us		Not more 2					
t_{HI}	SCK high time, ns		475	-	230	-	150	-
t_{LO}	SCK low time, ns		475	-	230	-	150	-
t_{CLD}	Clock delay, ns		Not less 50					
t_{CLE}	Clock setup time, ns		Not less 50					
t_{HO}	Data hold time, ns		Not less 0					
t_{HS}	$\overline{HOLD}$ setup time, ns		200	-	100	-	100	-
t_{HH}	$\overline{HOLD}$ hold time, ns		200	-	100	-	100	-

INTEGRAL

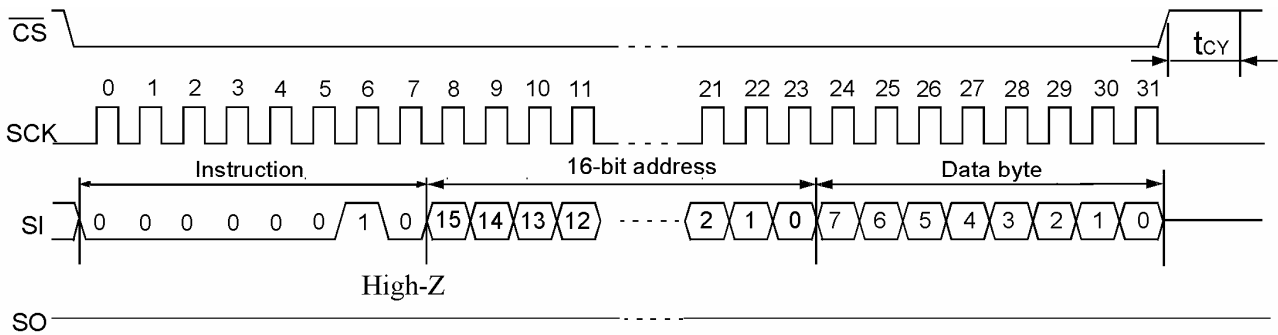**Data read sequence**
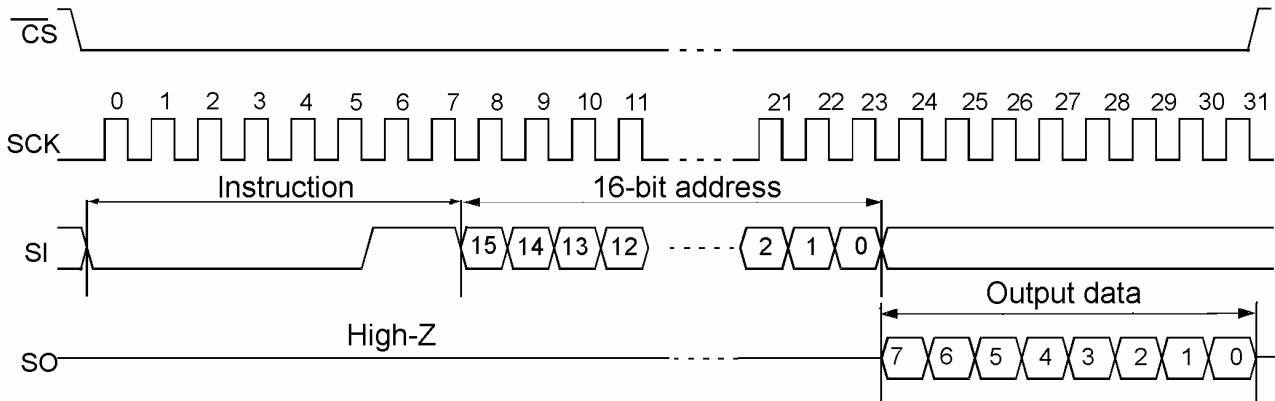
        There are six 8-bit instructions available for executing of read/write operation. The feature of IN25AA080N, IN25AA080D (IN25AA160N, IN25AA160D) is that 6 (5) higher address bits are insignificant (have to be ignored).

**Enable/disable instructions a) "Write enable" - WREN & b) "Write disable" - WRDI**

a)   b)
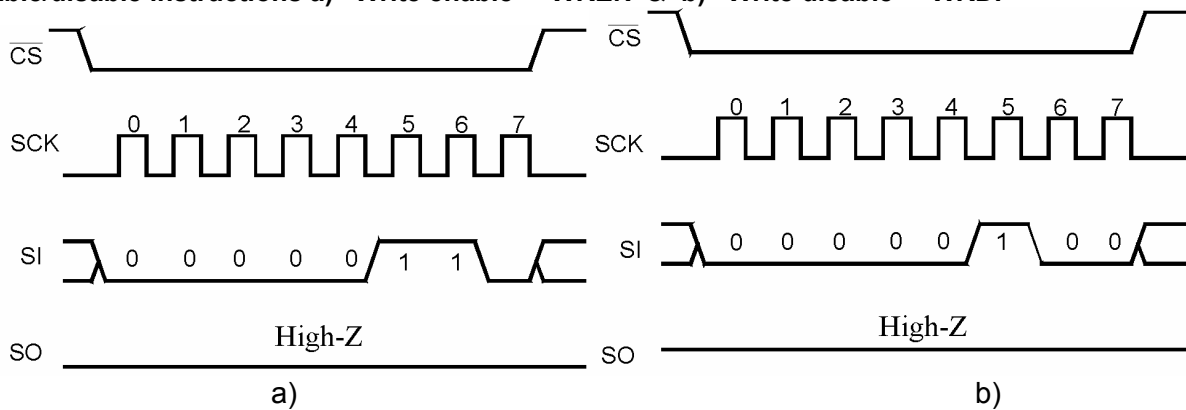
The powers up set ICs in the write disable state. For writing operation after power-up or after an WRDI (write disable) instruction, WREN (write enable) instruction must be issued. Any read/write operation can be executed on condition $\overline{CS}$ =0 (enable signal) , high level on $\overline{CS}$ pin switch IC to standby mode. Already intiated programming cycle will be comleted independently from $\overline{CS}$ signal. A low to high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle.

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Byte write sequence

Read status register sequence
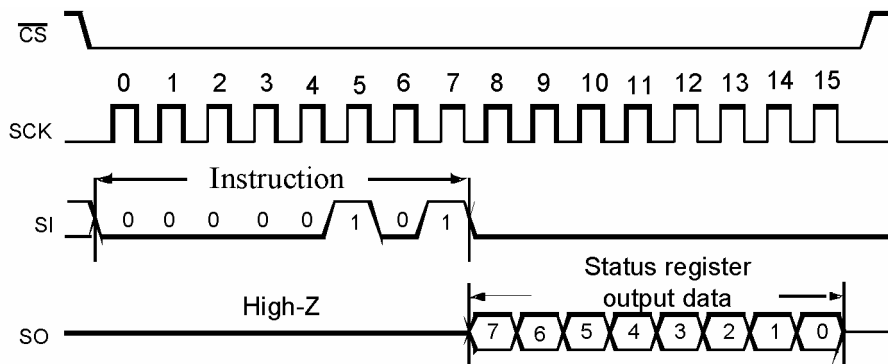
The RDSR (read status register) instruction provides access to the status register. The status register may be read at any time, even during a write cycle.

The 0th bit - WIP bit (Write-In-Process) of the status register indicates whether the IC is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress. This bit is read only.

The 1st bit - WEL bit (Write Enable Latch) of the status register indicates the status of the write enable latch. When set to a '1' the latch allows writes to the array, when set to a '0' the latch prohibits writes to the array. This bit is read only.

The 2nd & 3rd bits - BP0 and BP1 bits (Block Protection) indicate which blocks are currently write protected. These bits are set by the user issuing the WRSR instruction.

The SCK is used to synchronize the communication between a master and the IC. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

INTEGRAL

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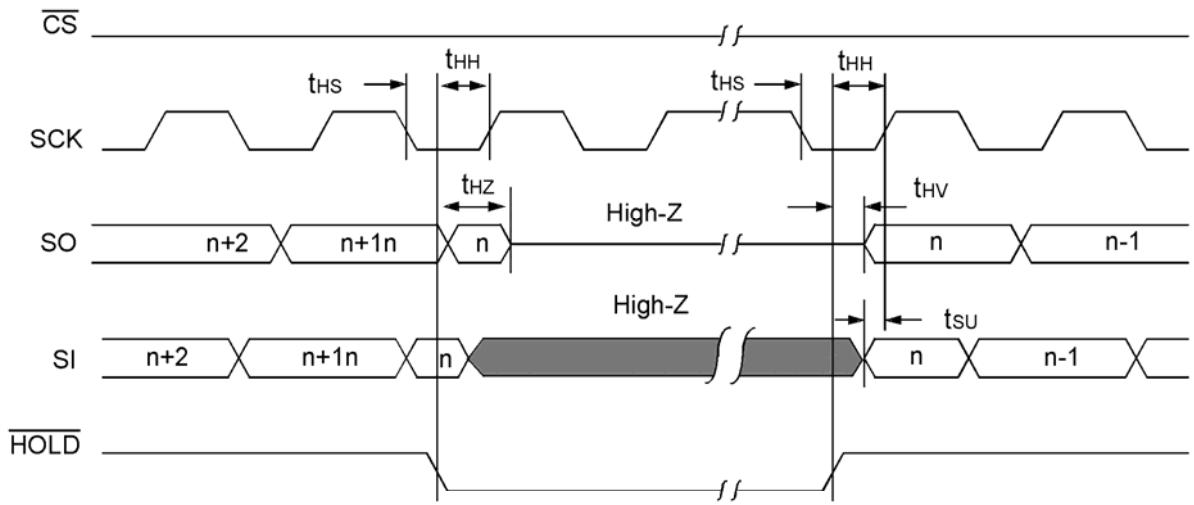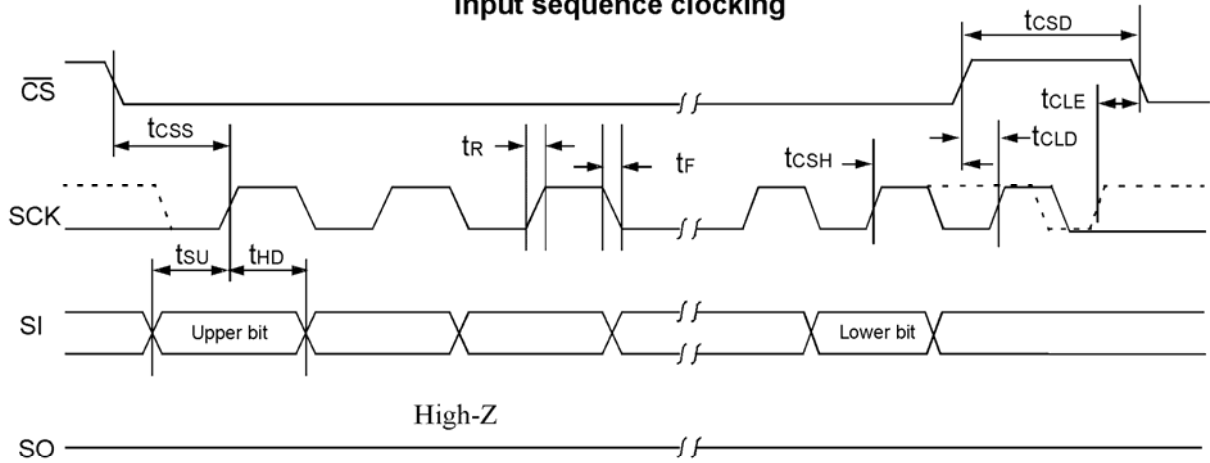**Write status register sequence**
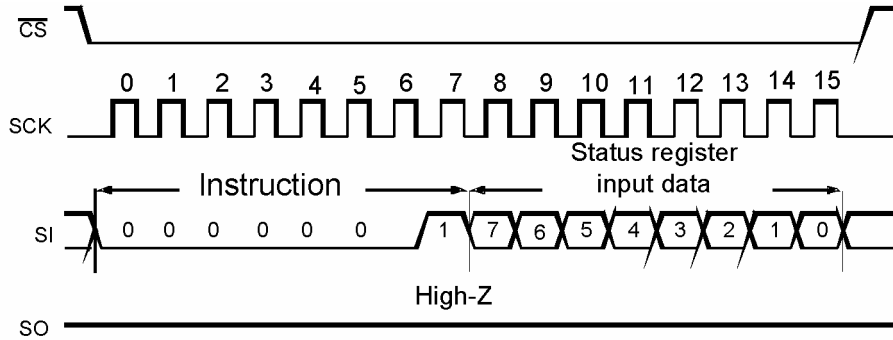
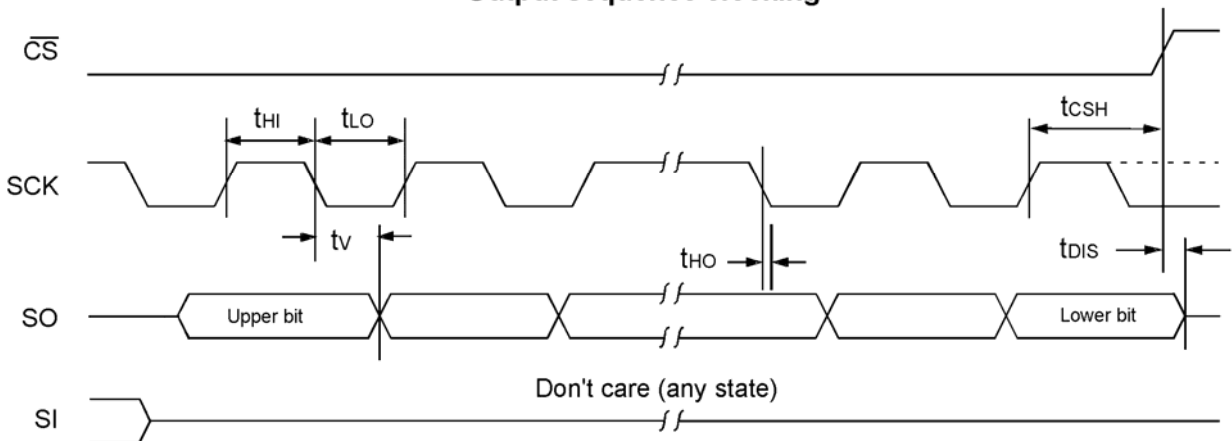**Page write sequence**

INTEGRAL
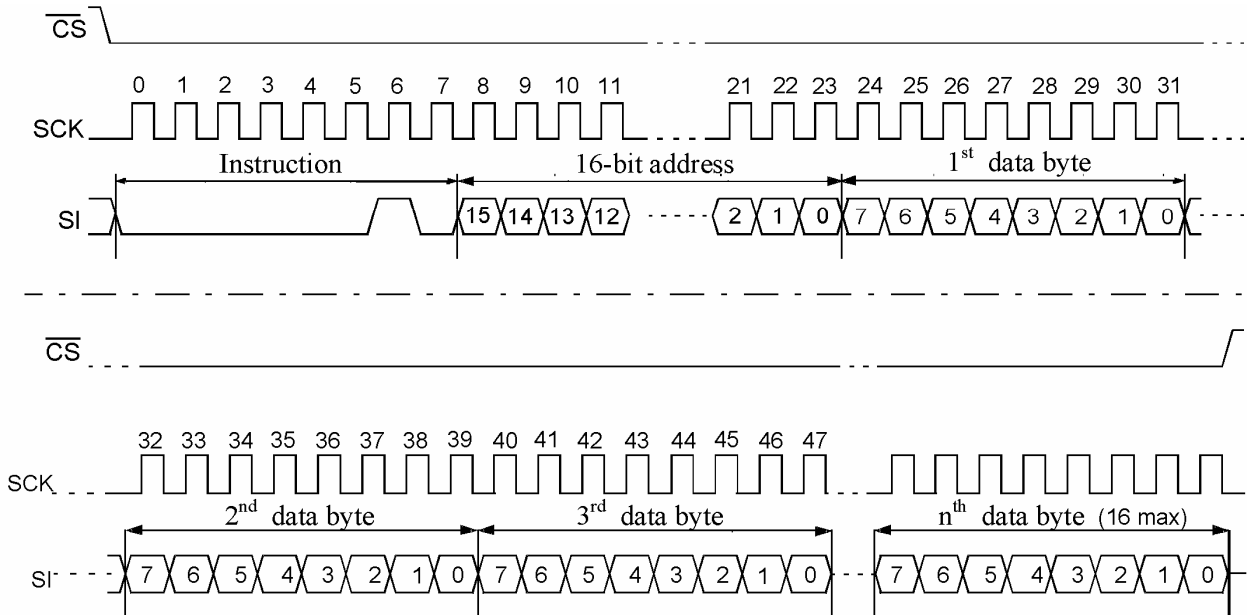
Data clocking diagramm
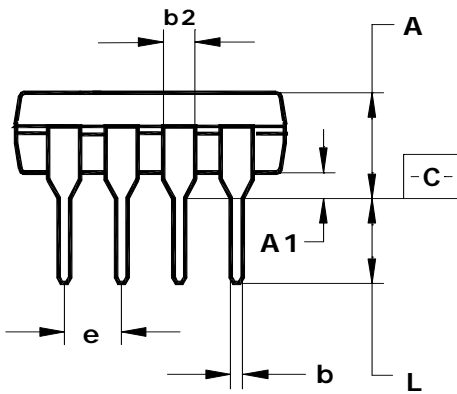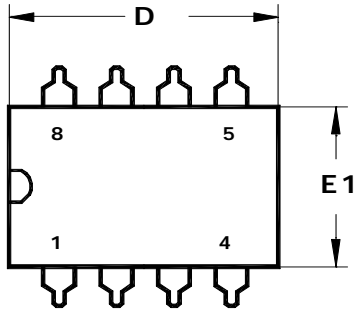
HOLD signal clocking

Input sequence clocking

Output sequence clocking

INTEGRAL

N SUFFIX PLASTIC DIP
(MS-001BA)
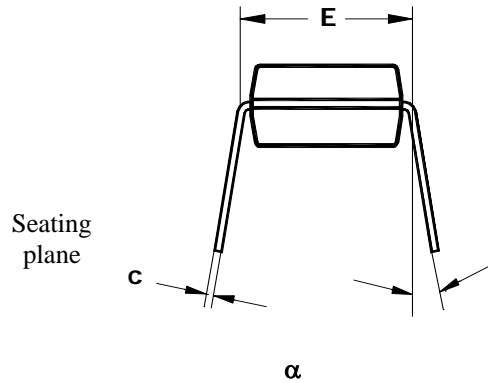
	D	E1	A	b	b2	e	α	L	E	c	A1
	mm										
min	9.02	6.07	—	0.36	1.14		0°	2.93	7.62	0.20	0.38
max	10.16	7.11	5.33	0.56	1.78	2.54	15°	3.81	8.26	0.36	—
	inches										
min	0.355	0.240	—	0.014	0.045		0°	0.115	0.300	0.008	0.015
max	0.400	0.280	0.210	0.022	0.070	0.1	15°	0.150	0.325	0.014	—

D SUFFIX PLASTIC SOP
(MS-012AA)

Seating
plane

⊕ | 0,25 (0,010) | Ⓜ | C

hx45°

α
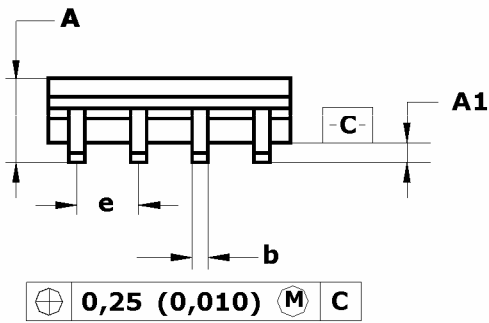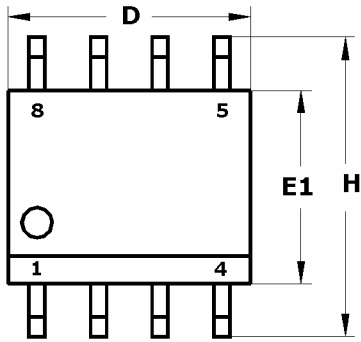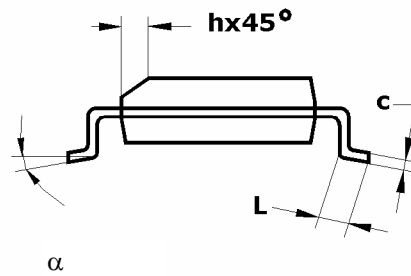
	D	E1	H	b	e	α	A	A1	c	L	h
	mm										
min	4.80	3.80	5.80	0.33		0°	1.35	0.10	0.19	0.41	0.25
max	5.00	4.00	6.20	0.51	1.27	8°	1.75	0.25	0.25	1.27	0.50
	inches										
min	0.1890	0.1497	0.2284	0.013		0°	0.0532	0.0040	0.0075	0.016	0.0099
max	0.1968	0.1574	0.2440	0.020	0.100	8°	0.0688	0.0090	0.0098	0.050	0.0196