

IN74HC112A

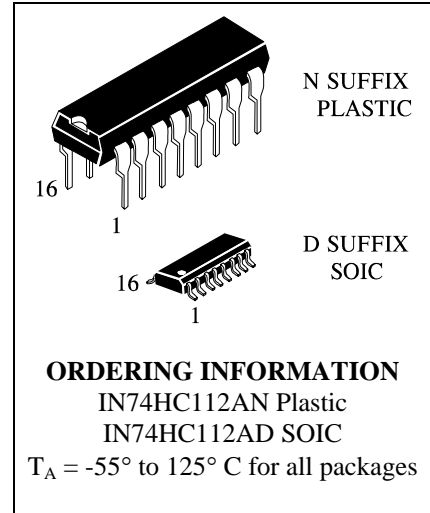
Dual J-K Flip-Flop with Set and Reset

High-Performance Silicon-Gate CMOS

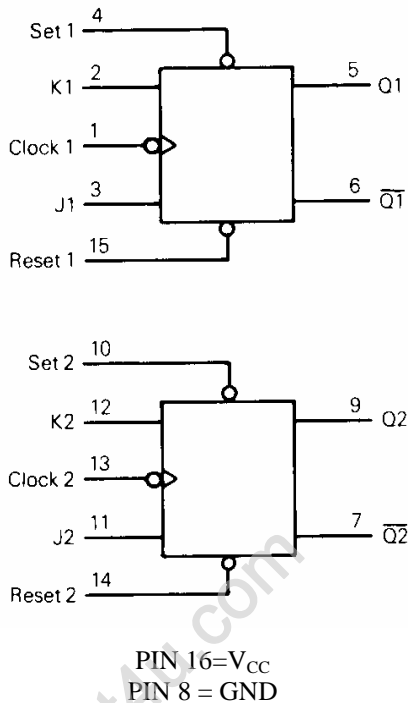
The IN74HC112A is identical in pinout to the LS/ALS112. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices



LOGIC DIAGRAM



PIN ASSIGNMENT

CLOCK 1	1	16	V _{CC}
K1	2	15	RESET 1
J1	3	14	RESET 2
SET 1	4	13	CLOCK 2
Q1	5	12	K2
$\overline{Q1}$	6	11	J2
$\overline{Q2}$	7	10	SET 2
GND	8	9	Q2

FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	\overline{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H		L	L	No Change	
H	H		L	H	L	H
H	H		H	L	H	L
H	H		H	H	Toggle	
H	H	L	X	X	No Change	
H	H	H	X	X	No Change	
H	H		X	X	No Change	

* Both output will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously
 X = Don't Care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC} = 2.0$ V	0	1000	
	$V_{CC} = 4.5$ V	0	500	
	$V_{CC} = 6.0$ V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	4.0	40	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \overline{Q} (Figures 1 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{PLH} , t _{PHL}	Maximum Propagation Delay , Reset to Q or \overline{Q} (Figures 2 and 4)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay ,Set to Q or \overline{Q} (Figures 2 and 4)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{IN}	Maximum Input Capacitance	-	10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop)	Typical @25°C, V _{CC} =5.0 V			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	35			

TIMING REQUIREMENTS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to-55°C	≤85°C	≤125°C	
t _{SU}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _H	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t _{REC}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

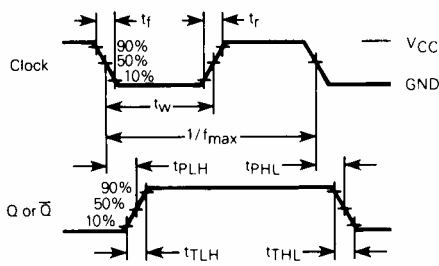


Figure 1. Switching Waveforms

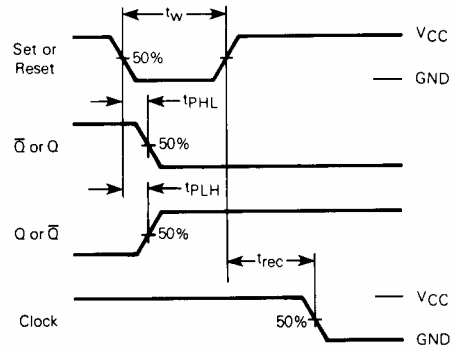


Figure 2. Switching Waveforms

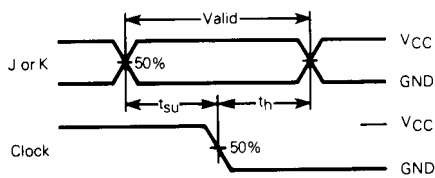


Figure 3. Switching Waveforms

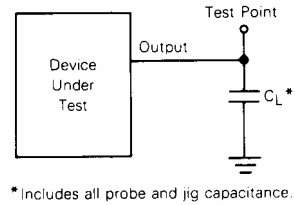
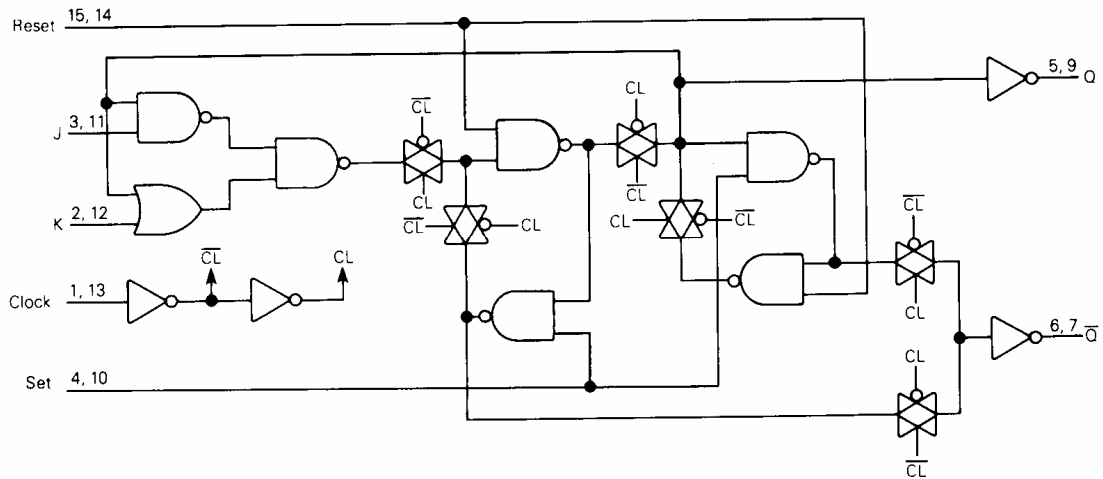
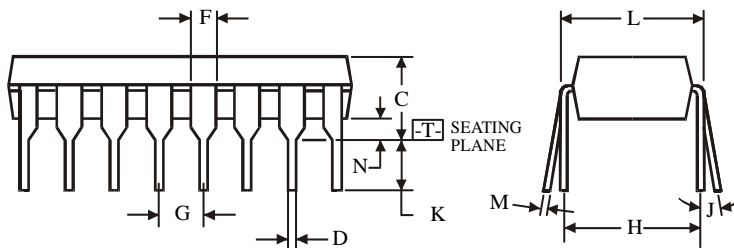
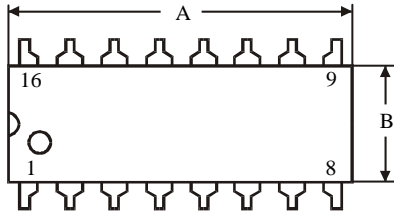
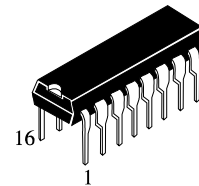


Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



**N SUFFIX PLASTIC DIP
(MS - 001BB)**



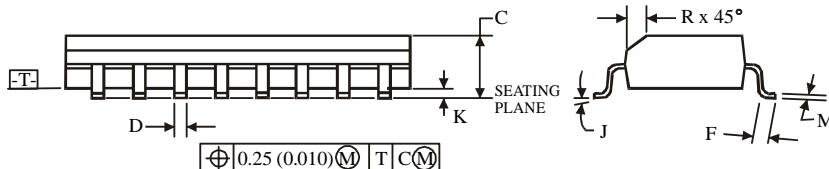
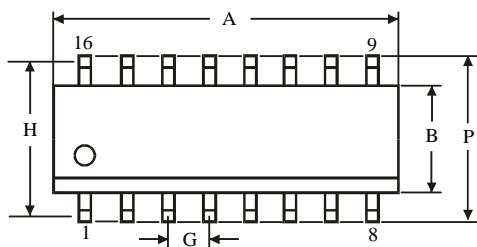
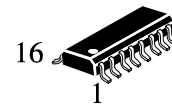
$\oplus 0.25 (0.010) \text{ (M) T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**D SUFFIX SOIC
(MS - 012AC)**



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	9.8	10
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5