IN74HC373A

Octal 3-State Noninverting Transparent Latch

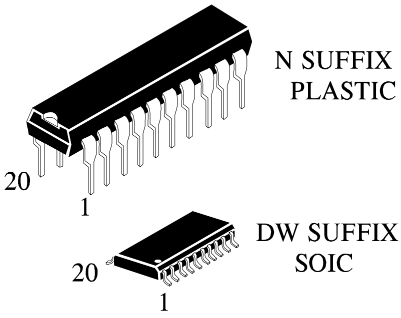
High-Performance Silicon-Gate CMOS

The IN74HC373A is identical in pinout to the LS/ALS373. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

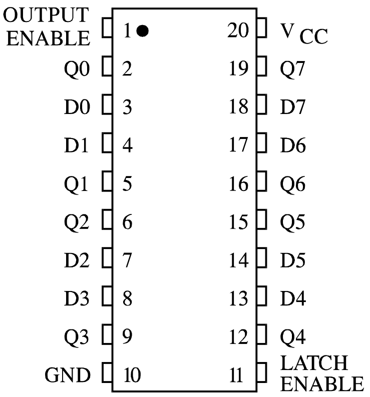
The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 µA
- High Noise Immunity Characteristic of CMOS Devices

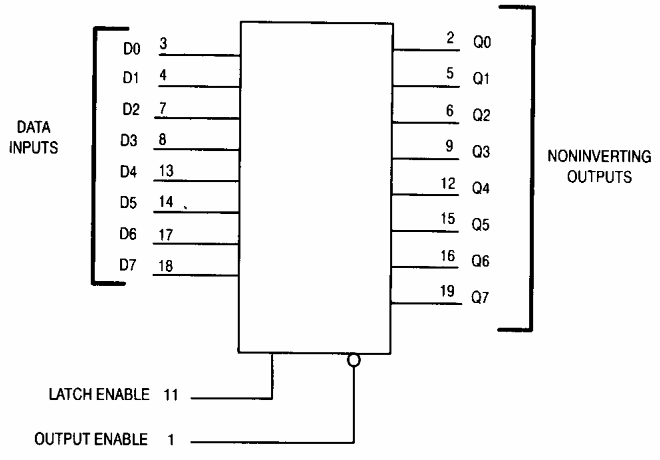


ORDERING INFORMATION
IN74HC373AN Plastic
IN74HC373ADW SOIC
T_A = -55° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don’t Care
Z = High Impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V	0	1000	ns
		V_{CC} =4.5 V	0	500	
		V_{CC} =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20$ µA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20$ µA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20$ µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA $\|I_{OUT}\| \le 7.8$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{IL} or V_{IH} $\|I_{OUT}\| \le 20$ µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}= V_{IL} or V_{IH} $\|I_{OUT}\| \le 6.0$ mA $\|I_{OUT}\| \le 7.8$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V_{IN}= V_{IL} or V_{IH} V_{OUT}=V_{CC} or GND	6.0	±0.5	±5.0	±10	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0µA	6.0	4.0	40	160	µA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay , Latch Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay ,Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay , Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF
C_{OUT}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 36	pF

TIMING REQUIREMENTS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{SU}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0 4.5 6.0	25 5.0 5.0	30 6.0 6.0	40 8.0 7.0	ns
t_h	Minimum Hold Time,Latch Enable to Input D (Figure 4)	2.0 4.5 6.0	5.0 5.0 5.0	5.0 5.0 5.0	5.0 5.0 5.0	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

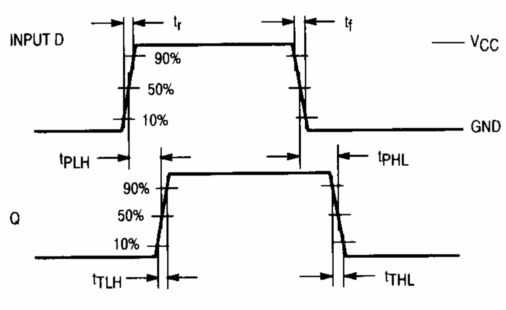


Figure 1. Switching Waveforms

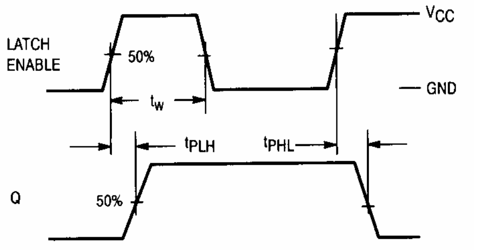


Figure 2. Switching Waveforms

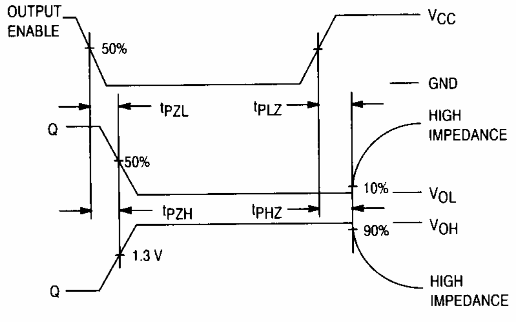


Figure 3. Switching Waveforms

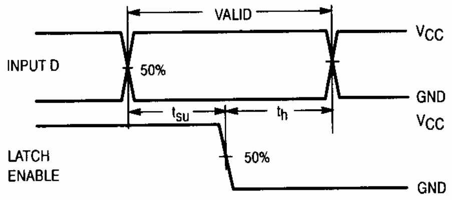
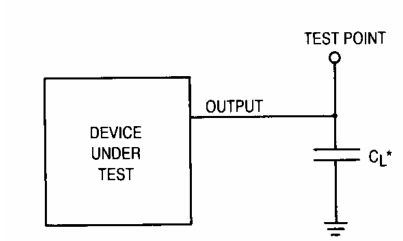
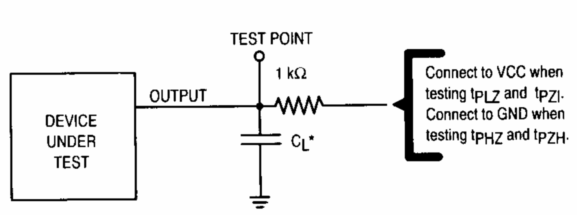


Figure 4. Switching Waveforms



* Includes all probe and jig capacitance

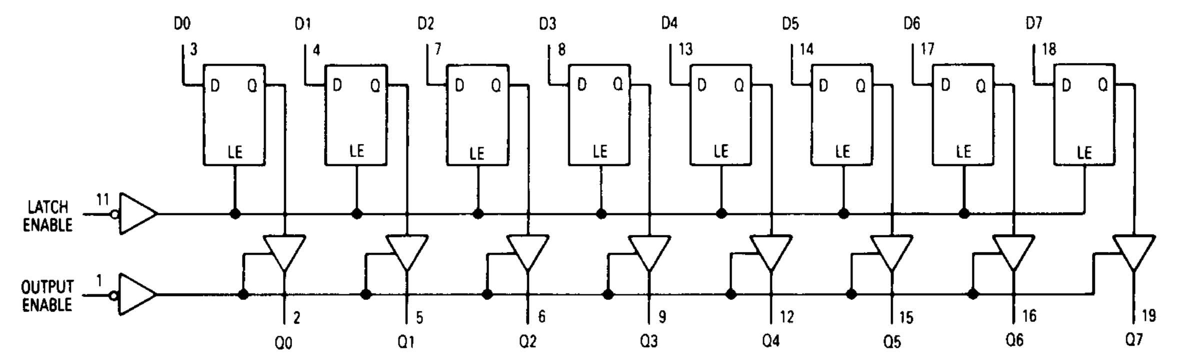
Figure 5. Test Circuit



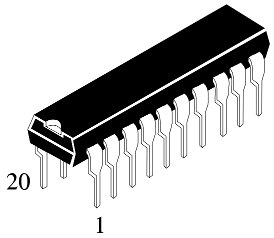
* Includes all probe and jig capacitance

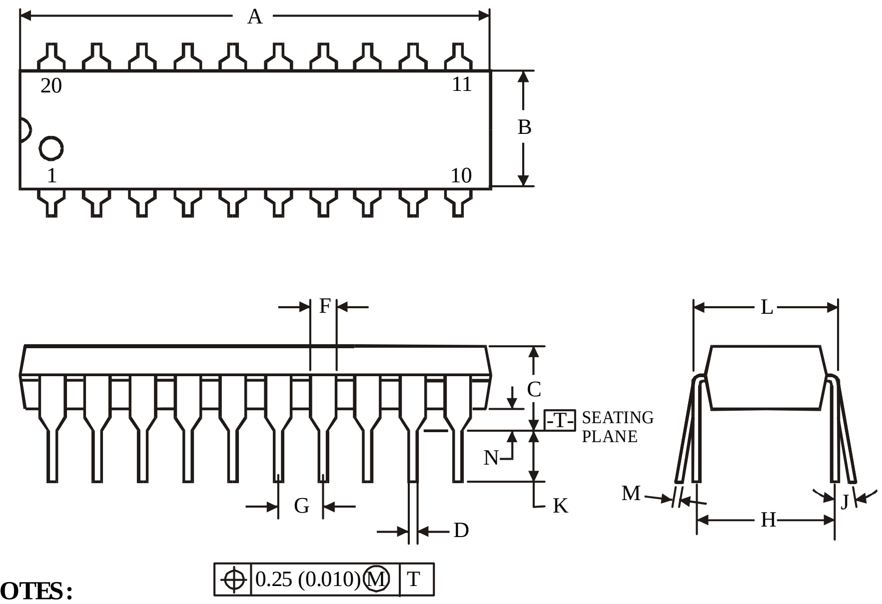
Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



N SUFFIX PLASTIC DIP
(MS - 001AD)





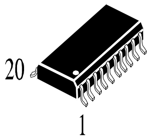
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	24.89	26.92
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

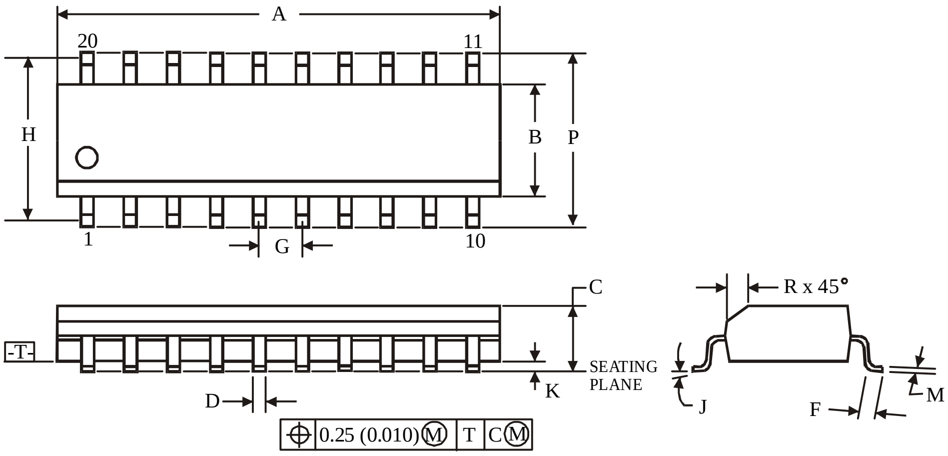
NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.

   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 013AC)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	12.6	13
B	7.4	7.6
C	2.35	2.65
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.1	0.3
M	0.23	0.32
P	10	10.65
R	0.25	0.75

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B ‐ 0.25 mm (0.010) per side.