

**IN74HC652A**

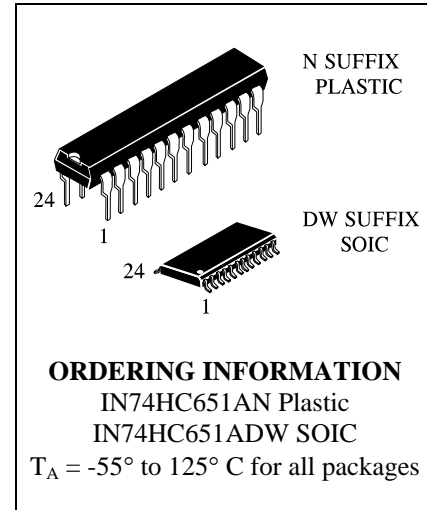
**Octal 3-State Bus Transceivers and D Flip-Flops**  
**High-Performance Silicon-Gate CMOS**

The IN74HC652A is identical in pinout to the LS/ALS652. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

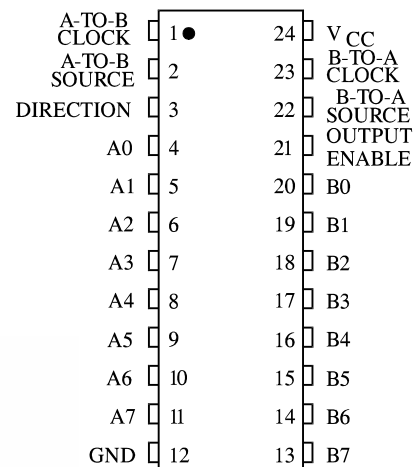
These devices consist of bus transceiver circuits, D-type flip-flop, and control circuitry arranged for multiplex transmission of data directly from the data bus or from the internal storage registers. Direction and Output Enable are provided to select the read-time or stored data function. Data on the A or B Data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (A-to-B Clock or B-to-A Clock) regardless of the select or enable or enable control pins. When A-to-B Source and B-to-A Source are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simulta-neously enabling Direction and Output Enable. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The IN74HC652A has noninverted outputs.

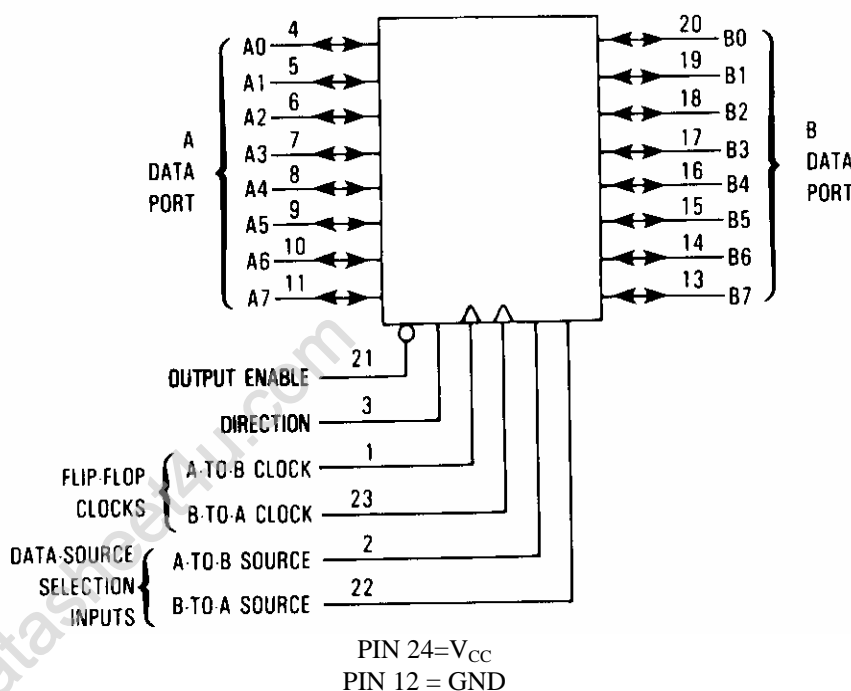
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices



**PIN ASSIGNMENT**



**LOGIC DIAGRAM**



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figures 2,3)			
	V <sub>CC</sub> =2.0 V	0	1000	ns
	V <sub>CC</sub> =4.5 V	0	500	
	V <sub>CC</sub> =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 6.0 mA   I <sub>OUT</sub>   ≤ 7.8 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 6.0 mA   I <sub>OUT</sub>   ≤ 7.8 mA)	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND (Pins 1,2,3,21,22,and 23)	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND, I/O Pins	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	8.0	80	160	μA

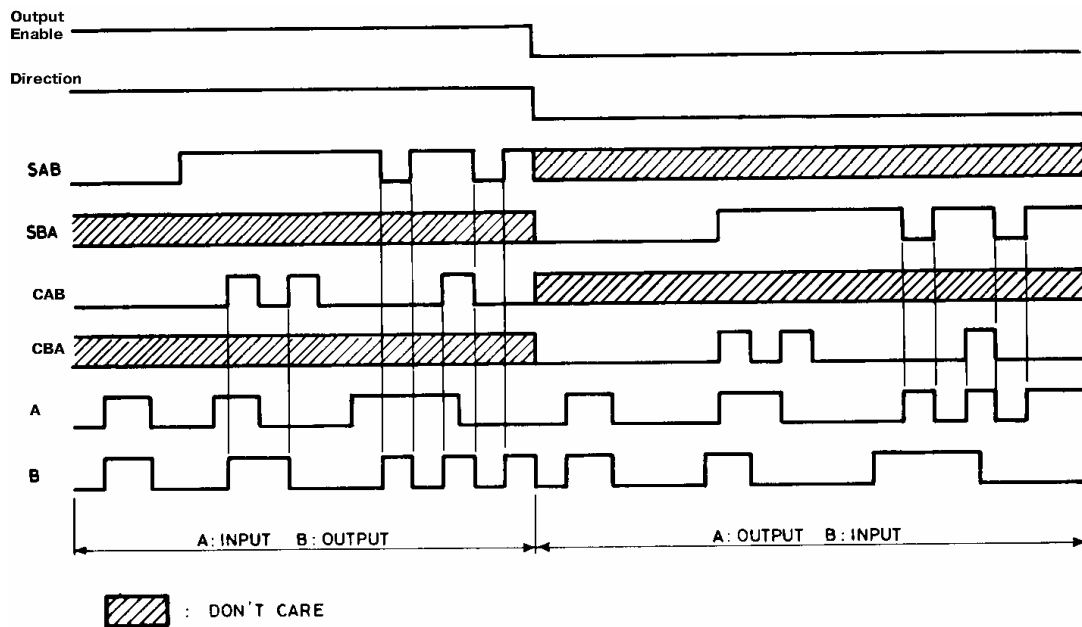
**AC ELECTRICAL CHARACTERISTICS** ( $C_L=50\text{pF}$ , Input  $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output B (or Input B to Output A) (Figures 2,3 and 9)	2.0	180	225	270	ns
		4.5	36	45	54	
		6.0	31	38	46	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A-to-B Clock to Output B (or B-to-A Clock to Output A) (Figures 1 and 9)	2.0	240	300	360	ns
		4.5	48	60	72	
		6.0	41	51	61	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A-to-B Source to Output B (or B-to-A Source to Output A) (Figures 4 and 9)	2.0	220	275	330	ns
		4.5	44	55	66	
		6.0	37	47	56	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay , Direction or Output Enable to Output A or B (Figures 5,6 and 10)	2.0	170	215	255	ns
		4.5	34	43	51	
		6.0	29	37	43	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay , Direction or Output Enable to Output A or B (Figures 5,6 and 10)	2.0	180	225	270	ns
		4.5	36	45	54	
		6.0	31	38	46	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figure 2)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>IN</sub>	Maximum Input Capacitance	-	10	10	10	pF
C <sub>OUT</sub>	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	-	15	15	15	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Channel)	Typical @25°C, V <sub>CC</sub> =5.0 V				pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	60				

**TIMING REQUIREMENTS** (Input  $t_r=t_f=6.0$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to-55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, Input A to A-to-B Clock (or Input B to B-to-A Clock) (Figure 7)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t <sub>h</sub>	Minimum Hold Time, A-to-B Clock to Input A (or B-to-A Clock to Input B) (Figure 7)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	5	7	
t <sub>w</sub>	Minimum Pulse Width, A-to-B Clock (or B-to-A Clock) (Figure 7)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figures 2 and 3)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

**TIMING DIAGRAM**



**FUNCTION TABLE**

Dir.	OE	CAB	CBA	SAB	SBA	A	B	FUNCTION
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
				X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*		X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops, are displayed at the A bus.
		X*		X	H	H L	H L	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
			X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
			X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
				H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respec.

X : DON'T CARE

Z : HIGH IMPEDANCE

Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS

\* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO TRANSITION OF THE CLOCK INPUTS

SWITCHING DIAGRAMS

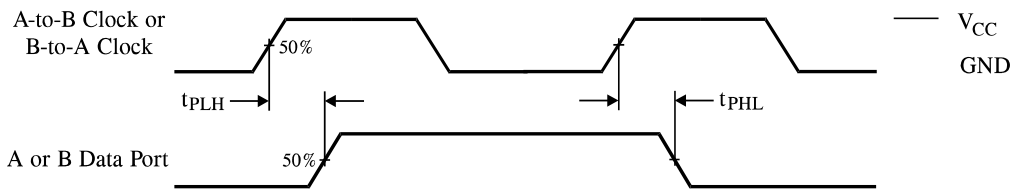


Figure 1. Switching Waveforms

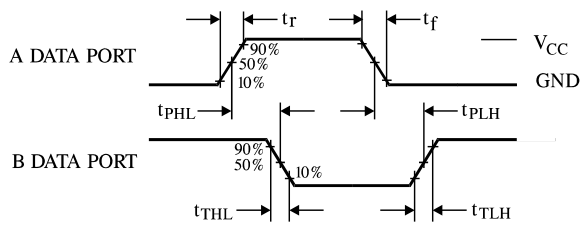


Figure 2. A Data Port = Input, B Data Port = Output

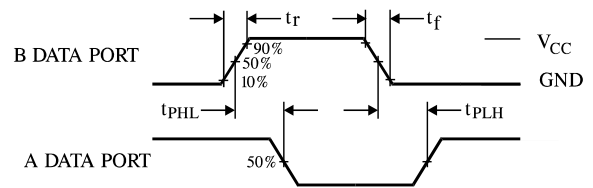


Figure 3. A Data Port = Output, B Data Port = Input

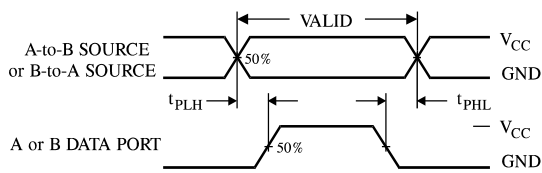


Figure 4. Switching Waveforms

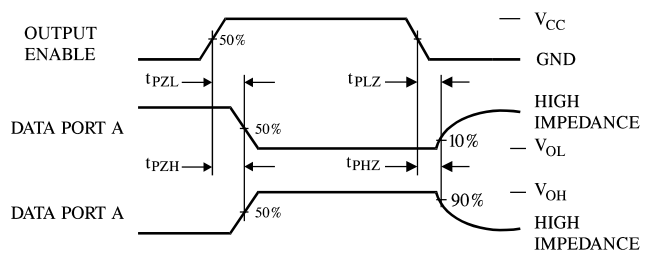


Figure 5. Switching Waveforms

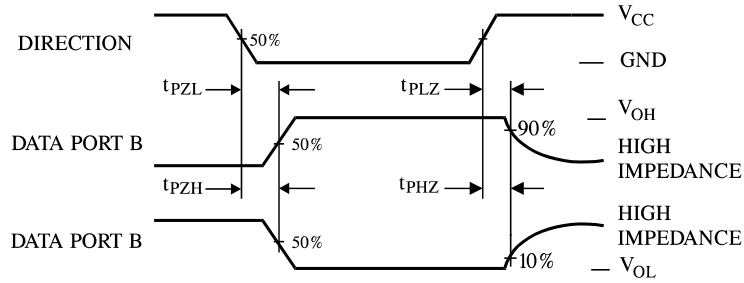


Figure 6. Switching Waveforms

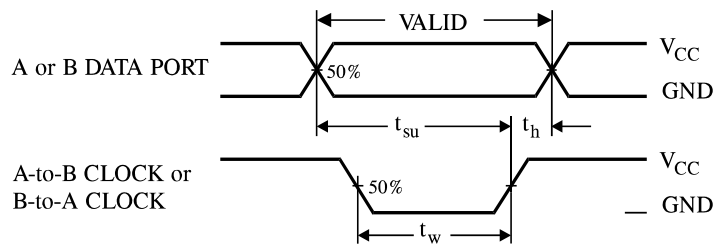
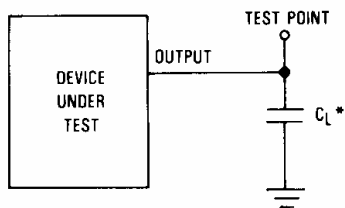
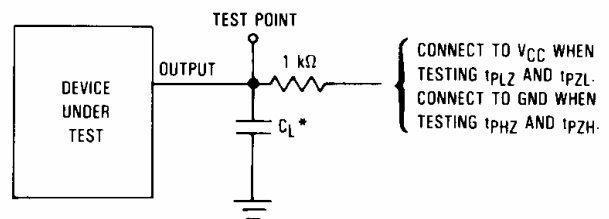


Figure 7. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 9. Test Circuit

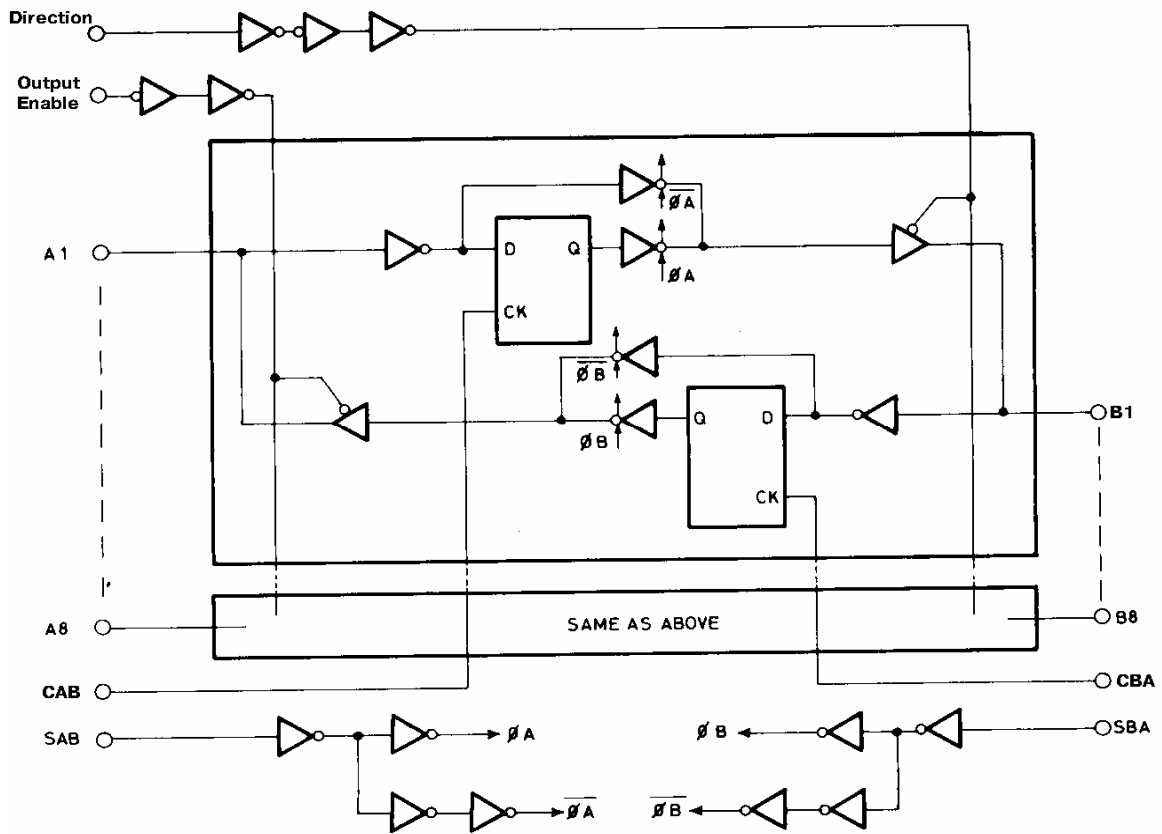


\*Includes all probe and jig capacitance.

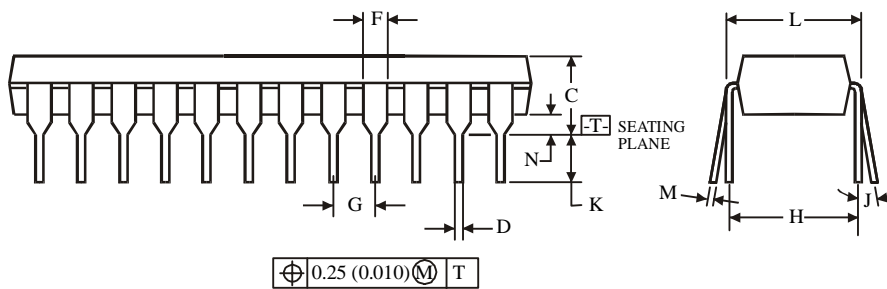
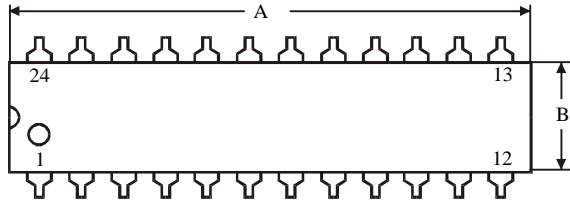
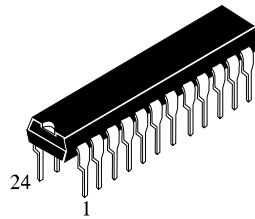
Figure 10. Test Circuit



EXPANDED LOGIC DIAGRAM



**N SUFFIX PLASTIC DIP  
(MS - 001AF)**

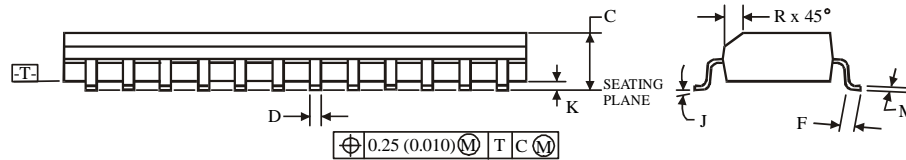
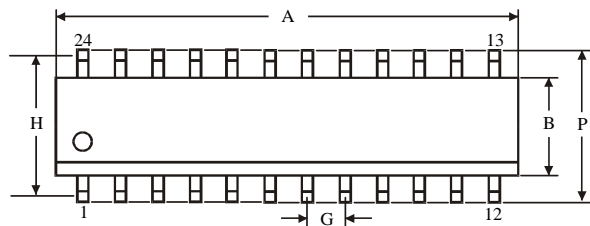
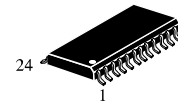


Dimension, mm		
Symbol	MIN	MAX
A	31.24	32.51
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**NOTES:**

- Dimensions "A", "B" do not include mold flash or protrusions.  
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

**D SUFFIX SOIC  
(MS - 013AD)**



Dimension, mm		
Symbol	MIN	MAX
A	15.2	15.6
B	7.4	7.6
C	2.35	2.65
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.1	0.3
M	0.23	0.32
P	10	10.65
R	0.25	0.75

**NOTES:**

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.