2K-BIT SERIAL EEPROM WITH MICROWIRE INTEFACE

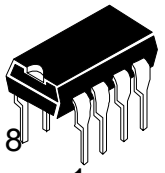
(compatible to CAT93C56 Catalyst)

DESCRIPTION

The IN93LC56 is a Electric erasable programmable ROM (EEPROM) memory data capacity 2K (256x8 or 128x16) with 3-wire interface.
There are 3 modification of ICs
A: ICs IN93AA56AD/AN are 8 bits registers (256x8) - ORG pin not used
B: ICs IN93AA56BD/BN are 16 bits registers (128x16) - ORG pin not used
C: ICs IN93AA56CN/CD are configured as either registers of 8 bits (ORG pin at GND) or 16 bits (ORG pin at V_{CC}, or not connected). Each register can be written (or read) serially by using the DI (or DO) pin.
The ICs is purposed for reading, writing & nonvolatile data storage in electronic units with 3-wire interface. ICs can be used in TV-sets, telecom equipment & consumer electronic devices.

FEATURES

- 100 year 2K data retention for Ta=25°C;
- Single power supply source (V_{CC} = 1,8 V – 6,0 V);
- Build-in voltage multiplier;
- Serial I/O bus;
- Autoincrement of word address;
- Self-timed write cycle with auto-clear;
- 1,000,000 Program/erase cycles;
- Power-up internal logic setup;
- Read cycles quantity are not limited;
- Low power consumption;
- Operating temperature range -40 … +85 °C.



N SUFFIX
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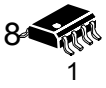
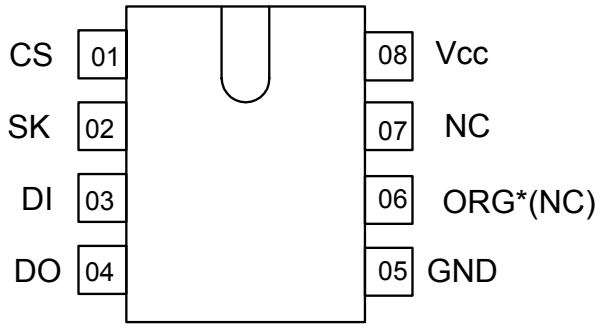


D SUFFIX
SOIC

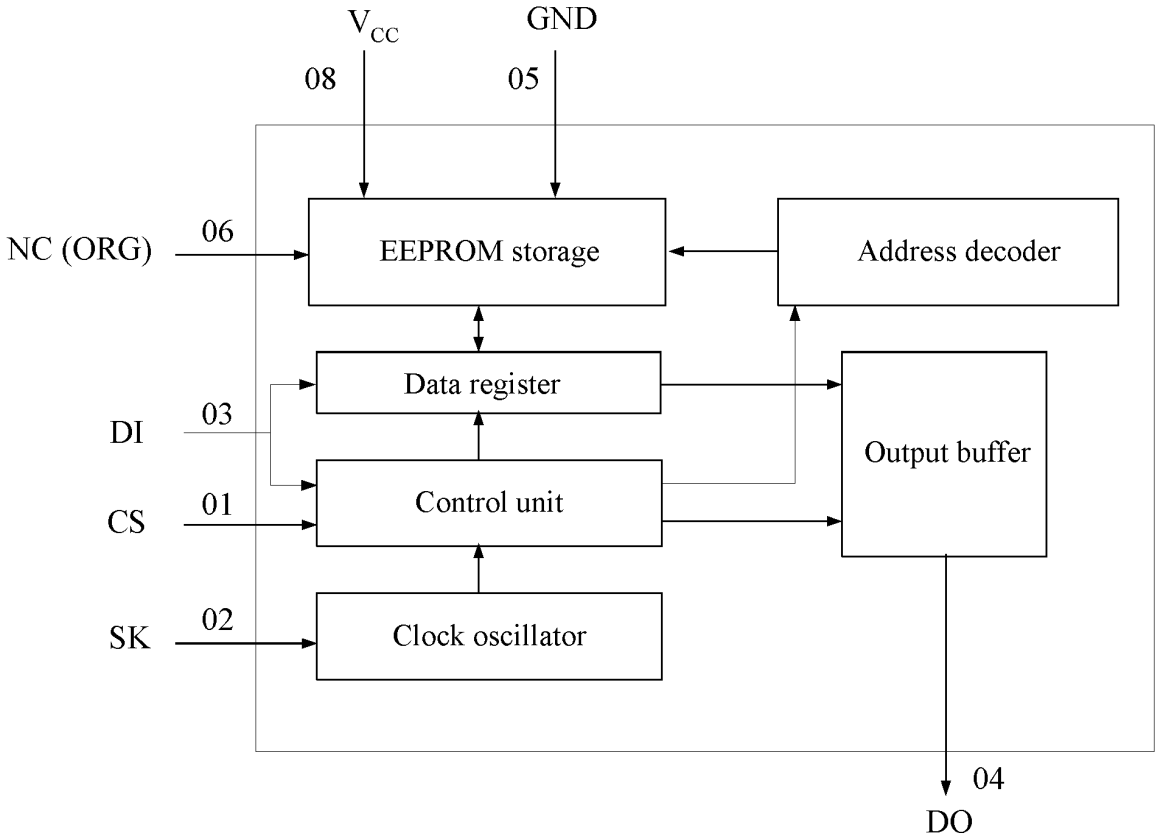
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+1.8 to 6.0V Power Supply
GND	Ground
ORG*	Memory Organization pin *
NC	No Connection



Note
* this pin is present only in IN93AA56CN, IN93AA56CD:
When the ORG pin is connected to V_{CC}, the x16 organization is selected.
When it is connected to ground, the x8 pin is selected.
If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.

IN93AA56AN/AD, IN93AA56BN/BD, IN93AA56CN/CD Block Diagram



Recommended Operation Conditions & Maximum Ratings*

Parameter, unit		Symbol	Recommended Operation Conditions		Maximum Ratings	
			Min	Max	Min	Max
Supply voltage,V		U_{CC}	1,8	6,0	- 0,5	7,0
High level input voltage, V	4,5 V ≤ Ucc ≤ 5,5 V	U_{IH}	2,0	Ucc + 0,5	–	Ucc + 0,5
	1,8 V ≤ Ucc < 4,5 V		0,7Ucc	Ucc + 0,5		
Low level input voltage, V	4,0 V ≤ Ucc ≤ 5,5 V	U_{IL}	-0,1	0,8	- 0,5	–
	1,8 V ≤ Ucc < 4,0 V		0	0,2Ucc		
Low level output current мA		I_{OL}	–	2,1	–	–
Output short-circuit current, mA		I_{OS} [1)]	–	–	–	100

[1)] Time not more than 1 sec

Electric Parameters

Parameter, unit	Symbol	Mode	Min	Max	T_A, °C
Low level output voltage, V	U_{OL1}	4,5 V ≤ U_{CC} ≤ 5,5 V I_{OL} = 2,1 mA	–	0,4	25 ± 10; -45; 85
High level output voltage, V	U_{OH1}	4,5 V ≤ U_{CC} ≤ 5,5 V I_{OH} = -400 uA	2,4	–	
Low level output voltage, V	U_{OL2}	1,8 V ≤ U_{CC} < 4,5 V I_{OL} = 1 mA	–	0,2	
High level output voltage, V	U_{OH2}	1,8 V ≤ U_{CC} < 4,5 V I_{OH} = -100 uA	U_{CC}-0,2	–	
Low level input leakage current, uA	I_{ILL}	0 ≤ U_I ≤ Ucc 1,8 V ≤ U_{CC} ≤ 6,0 V	–	-1,0	
High level input leakage current, uA	I_{ILH}	0 ≤ U_I ≤ Ucc 1,8 V ≤ U_{CC} ≤ 6,0 V	–	1,0	
Low level output leakage current, uA	I_{OLL}	0 ≤ U_O ≤ Ucc U_{IL} = 0 V 1,8 V ≤ U_{CC} ≤ 6,0 V	–	-1,0	
High level output leakage current, uA	I_{OLH}	0 ≤ U_O ≤ Ucc U_{IL} = 0 V 1,8 V ≤ U_{CC} ≤ 6,0 V	–	1,0	
Consumption current (8-bit mode), uA	I_{CC1}	Ucc = 5,5 V U_{IL} = 0 V	–	10	
Consumption current (16-bit mode), nA	I_{CC2}	Ucc = 5,5 V U_{IL} = 0 V U_{IH} = Ucc U_{ORG} = Ucc	–	900	
Consumption current (Operating Read), uA	$I_{OCC\ R}$	Ucc = 5,0 V f_C = 1 MHz	–	500	
Consumption current (Operating Write/Erase), uA	$I_{OCC\ E/W}$	Ucc = 5,0 V f_C = 1 MHz	–	3,0	
Output Delay to Low, ns	t_{PD0}	U_{CC} = 4,5 V f_C = 1 MHz	–	250	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	500	
		U_{CC} = 1,8 V f_C = 250 kHz	–	1000	
Output Delay to High, ns	t_{PD1}	U_{CC} = 4,5 V f_C = 1 MHz	–	250	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	500	
		U_{CC} = 1,8 V f_C = 250 kHz	–	1000	

Parameter, unit	Symbol	Mode	Min	Max	T_A, °C
Output Delay to High-Z, ns	t_{HZ}	U_{CC} = 4,5 V f_C = 1 MHz	–	100	25 ± 10; -40; 85
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	200	
		U_{CC} = 1,8 V f_C = 250 kHz	–	400	
Write/Erase cycle, ms	t_{CY}	U_{CC} = 4,5 V f_C = 1 MHz	–	10	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	10	
		U_{CC} = 1,8 V f_C = 250 kHz	–	10	
Output Delay to Status Check, ns	t_{SV}	U_{CC} = 4,5 V f_C = 1 MHz	–	250	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	500	
		U_{CC} = 1,8 V f_C = 250 kHz	–	1000	
Power-up to Read Operation Time, ms	t_{PUR}	U_{CC} = 4,5 V f_C = 1 MHz	–	1,0	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	1,0	
		U_{CC} = 1,8 V f_C = 250 kHz	–	1,0	
Power-up to Wtite Operation Time, ms	t_{PUW}	U_{CC} = 4,5 V f_C = 1 MHz	–	1,0	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	1,0	
		U_{CC} = 1,8 V f_C = 250 kHz	–	1,0	
Program/erase cycles	$N_{E/W}$	Ucc = 5,0 V	1000000	–	25 ± 10
Note t_{PUR} & t_{PUW} times are delays from of power up to operation started					

3-wire Interface Parameters (-40 °C ≤ T_A ≤ 85 °C)

Symbol	Parameter, unit	1,8V≤U_{CC}≤6,0V		2,5V≤U_{CC}≤6,0 V		4,5V≤U_{CC}≤6,0 V	
		Min	Max	Min	Max	Min	Max
f_C	Clock frequency, MHz	-	0,25	-	0,5	-	2
t_{CSS}	CS Setup Time, ns	200	-	100	-	50	-
t_{CSH}	CS Hold Time, ns	0	-	0	-	0	-
t_{DIS}	DI Setup Time, ns	400	-	200	-	100	-
t_{DIH}	DI Hold Time, ns	400	-	200	-	100	-
$t_{CS\ MIN}$	Minimum CS Low Time, ns	1000	-	500	-	250	-
t_{SKHI}	Minimum SK High Time, ns	1000	-	500	-	250	-
t_{SKLOW}	Minimum SK Low Time, ns	1000	-	500	-	250	-

Instruction Set

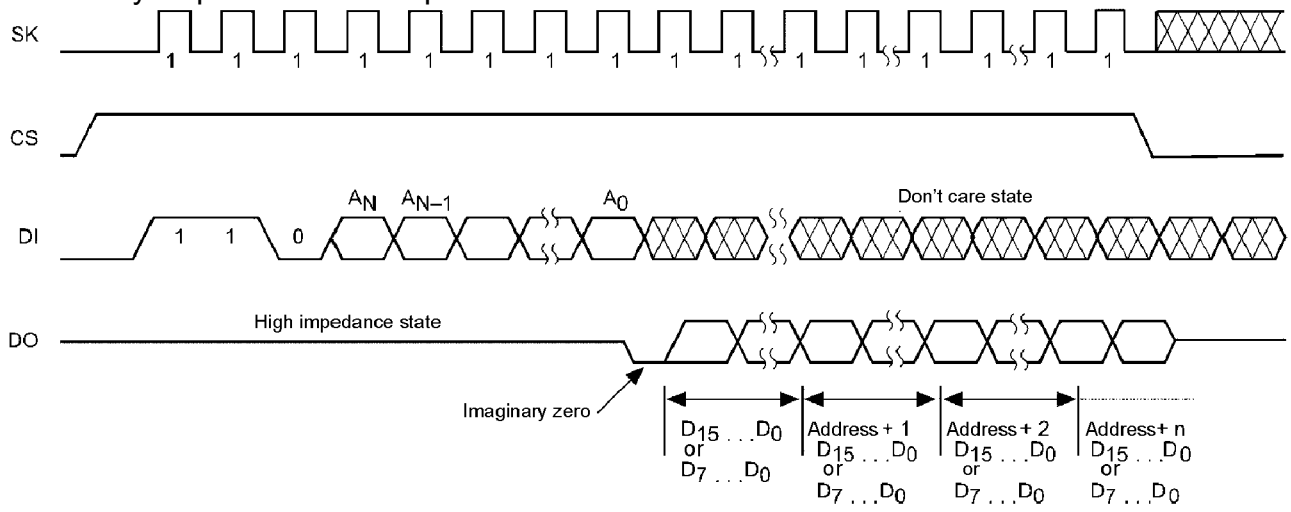
Instruction	Start Bit	Op-code	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A8-A0	A7-A0			Read Address AN- AO
ERASE	1	11	A8-A0	A7-A0			Clear Address AN- AO
WRITE	1	01	A8-A0	A7-A0	D7-D0	D15-D0	Write Address AN- AO
EWEN	1	00	11XXXXXXX	11XXXXXX			Write Enable
EWDS	1	00	00XXXXXXX	00XXXXXX			Write Disable
ERAL	1	00	10XXXXXXX	10XXXXXX			Clear All Addresses
WRAL	1	00	01XXXXXXX	01XXXXXX	D7-D0	D15-D0	Write All Addresses
Note – Address bits A8 is not used, but must be "1" or "0" for READ, ERASE, WRITE instructions							

There are 7 instructions 11bit for 128x16 or 12bit for 256x8 memory organization to execute WRITE, ERASE or READ operation

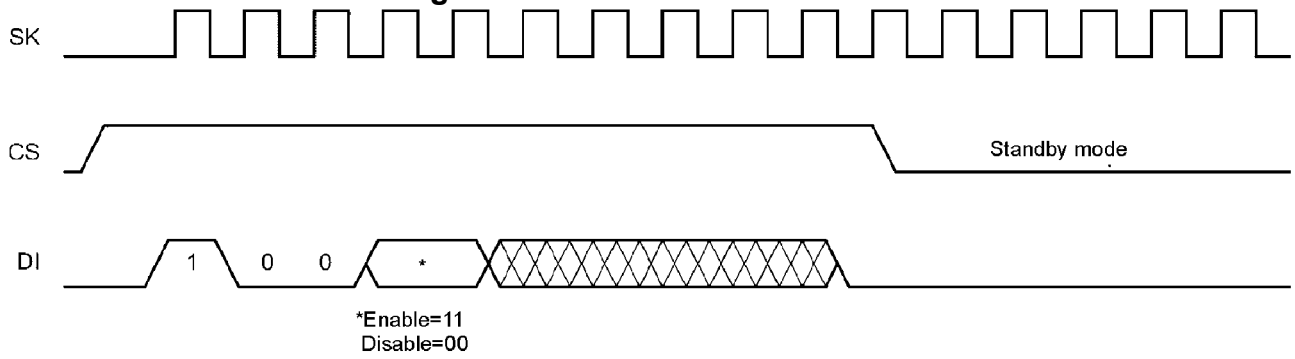
The format for all instructions sent to the device is a logical "1" start bit, a 2-bits (or 4-bits) operation code, 8-bit address (128x16)/ 9-bit address (256x8).

High address bit is inessential for decoding and can be any (“1” or “0”)

A 16-bit data field (organization 128x16) or 8-bit data field (organization 256x8) is additionally required for write operations.

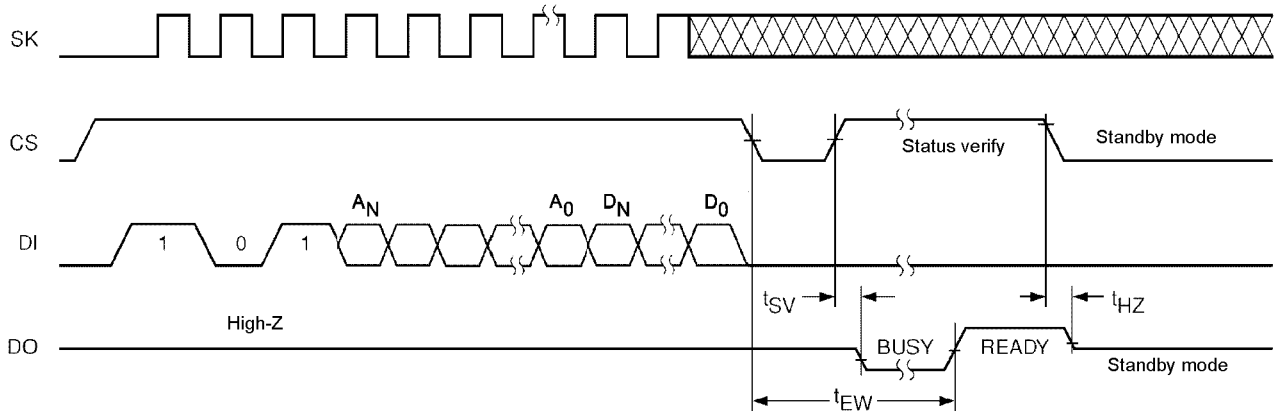


Read Instruction Timing



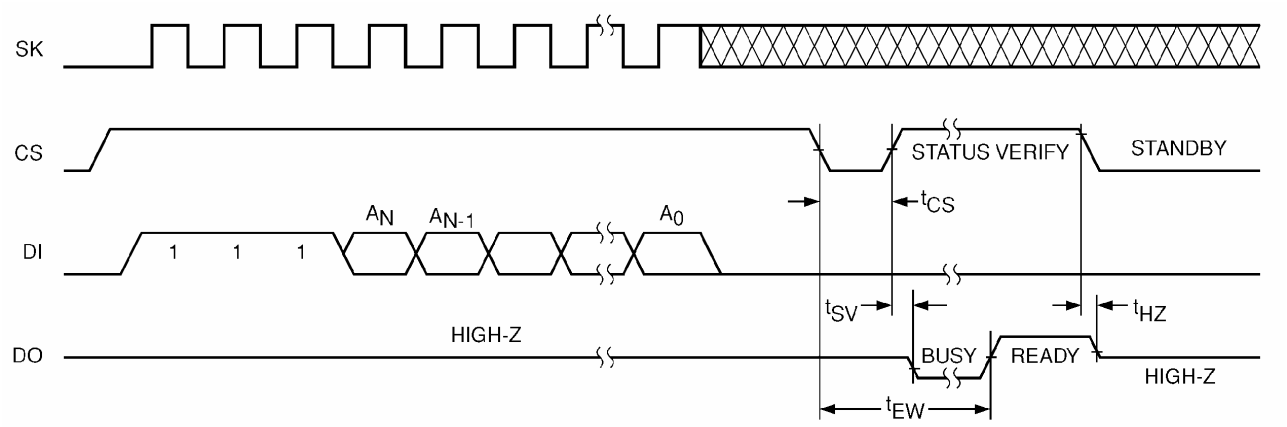
EWEN/EWDS Instruction Timing

The IN93AA56 powers up switch IC to the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction.



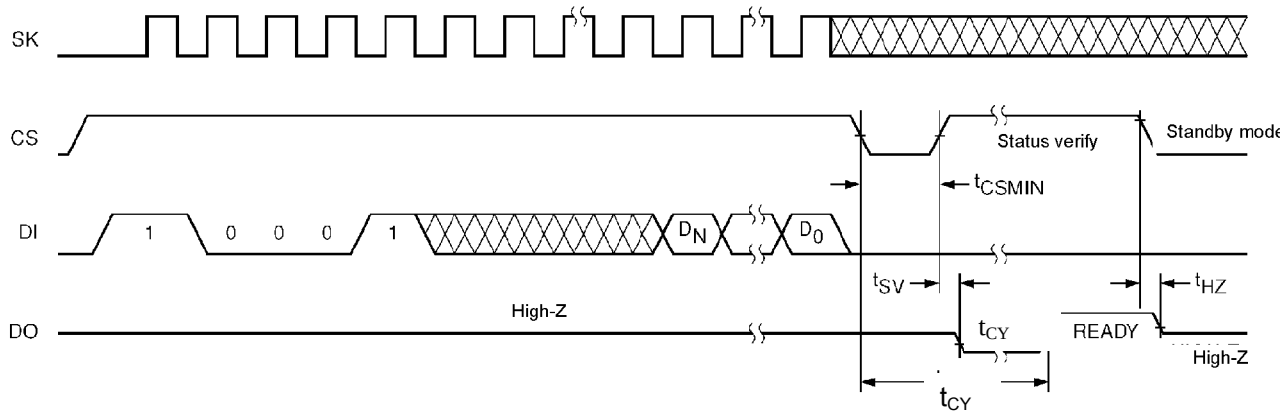
ERAL Instruction Timing

The IN93AA56 ignore all external signals applied to SK and DI pins during cycle of active programming. Erase/write cycle duration (t_{CY}) can be measured (controlled) by scanning of IC output. Low level (logical “0”) means that programming still in progress, high level (logical “1”) means that programming is already completed. Transition of output to High-Z state after programming cycle was completed is executed by applying low level (logic “0”) to CS pin or applying high level (logical “1”) to DI pin (for case CS = 1).

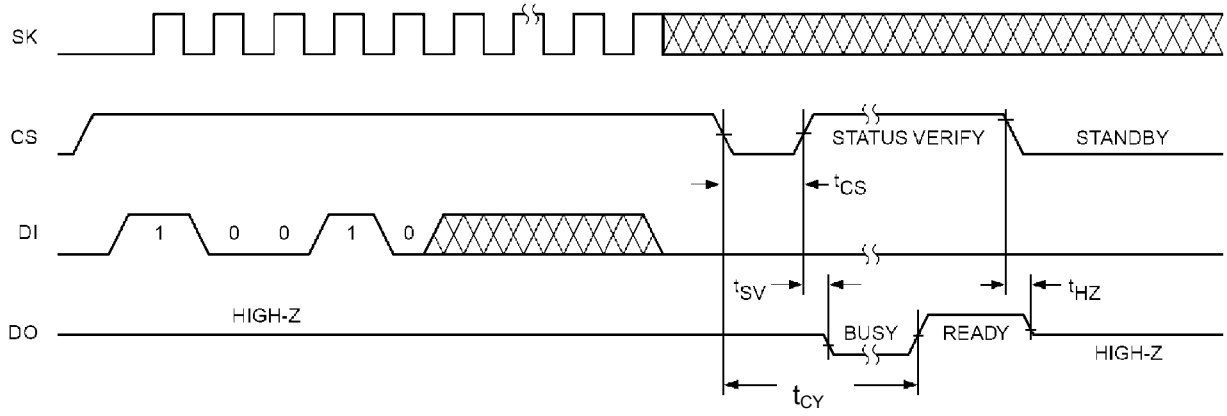


ERASE Instruction Timing

Once cleared, the content of a cleared location returns to a logical “1” state.

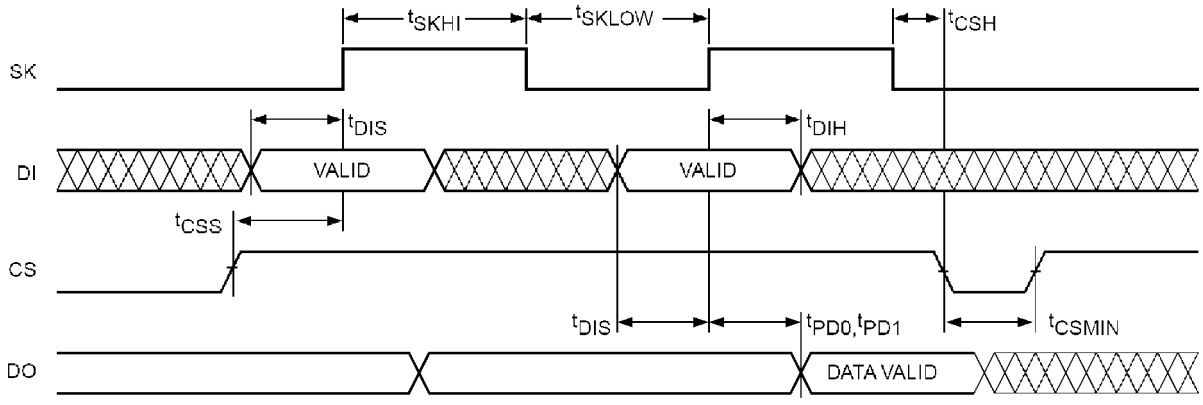


WRAL Instruction Timing



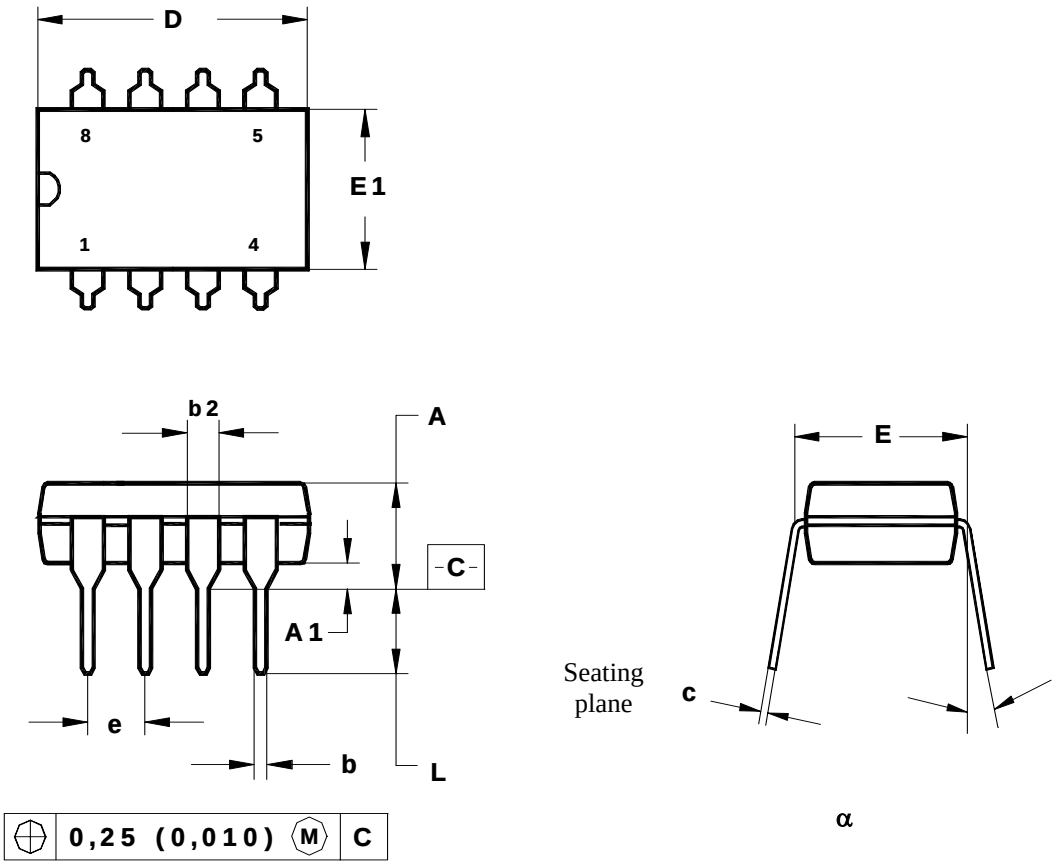
Once cleared, the contents of all memory bits return to a logical “1” state.

ERAL Instruction Timing



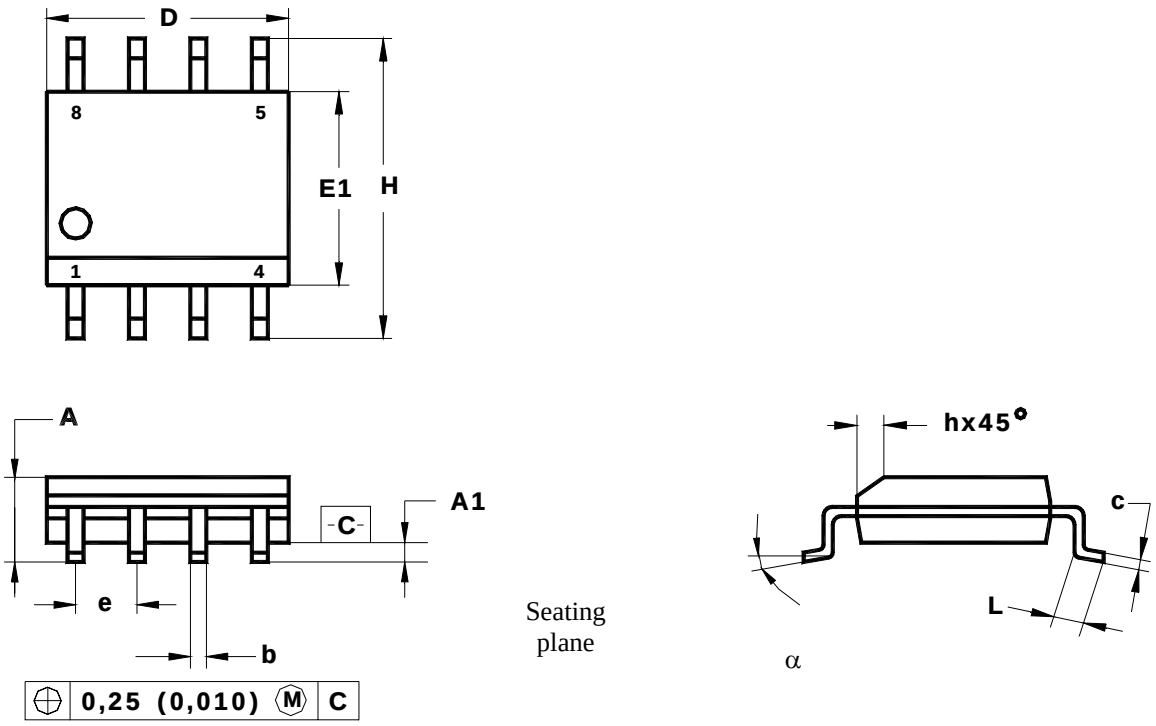
Sychronous Data Timing

N SUFFIX PLASTIC DIP
(MS-001BA)



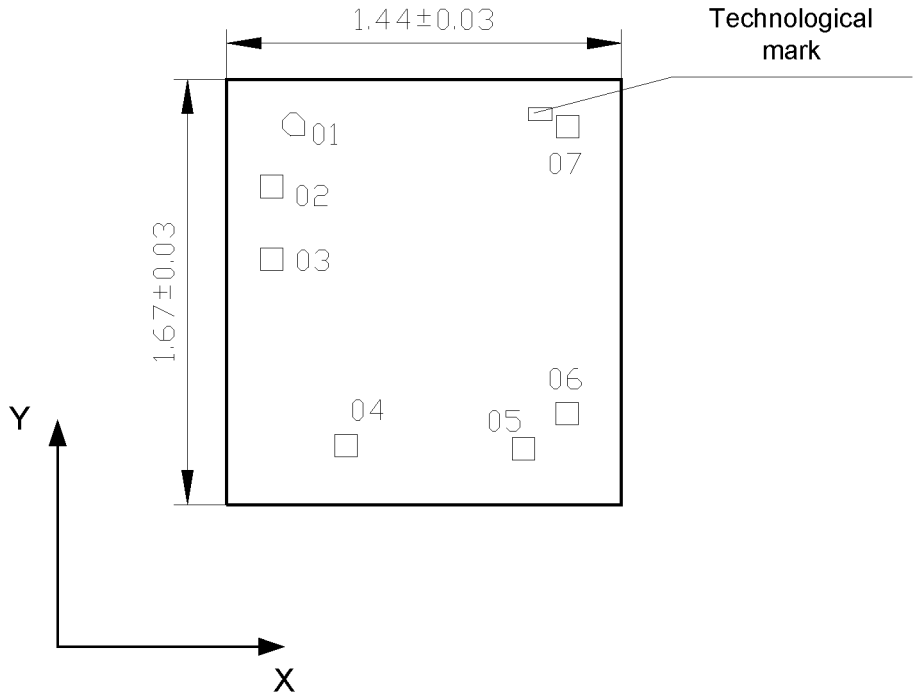
	D	E1	A	b	b2	e	α	L	E	c	A1
mm											
min	9.02	6.07	—	0.36	1.14		0°	2.93	7.62	0.20	0.38
max	10.16	7.11	5.33	0.56	1.78	2.54	15°	3.81	8.26	0.36	—
inches											
min	0.355	0.240	—	0.014	0.045		0°	0.115	0.300	0.008	0.015
max	0.400	0.280	0.210	0.022	0.070	0.1	15°	0.150	0.325	0.014	—

D SUFFIX PLASTIC SOP
(MS-012AA)



	D	E1	H	b	e	α	A	A1	c	L	h
mm											
min	4.80	3.80	5.80	0.33		0°	1.35	0.10	0.19	0.41	0.25
max	5.00	4.00	6.20	0.51	1.27	8°	1.75	0.25	0.25	1.27	0.50
inches											
min	0.1890	0.1497	0.2284	0.013		0°	0.0532	0.0040	0.0075	0.016	0.0099
max	0.1968	0.1574	0.2440	0.020	0.100	8°	0.0688	0.0090	0.0098	0.050	0.0196

Die dimension & contact pad location



Technology mark coordinates, mm: left bottom corner x = 1,075; y =1,41.

Die thickness 0,46±0,02 mm.

Pad location table

Pad number	Coordinates (left bottom corner), mm		Contact pad description
	X	Y	
01	0.223	1.450	CS
02	0.145	1.230	SK
03	0.145	0.964	DI
04	0.414	0.162	DO
05	1.064	0.149	GND
06	1.221	0.278	NC (ORG*)
07	1.225	1.450	V_{CC}

Note: Contact pad coordinates and dimensions 0.085 x 0.085 mm are indicated according passivation layer

* For ICs IN93AA56CN/CD