

16K-BIT SERIAL EEPROM WITH MICROWIRE INTEFACE

(compatible to CAT93C86 Catalyst)

DESCRIPTION

The IN93LC86 is a Electric erasable programmable ROM (EEPROM) memory data capacity 4K (2048x8 or 1024x16) with 3-wire interface.

There are 3 modification of ICs

A: ICs IN93AA86AD/AN are 8 bits registers (2048x8) - ORG pin not used

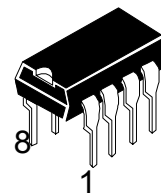
B: ICs IN93AA86BD/BN are 16 bits registers (1024x16) - ORG pin not used

C: ICs IN93AA86CN/CD are configured as either registers of 8 bits (ORG pin at GND) or 16 bits (ORG pin at V_{CC}, or not connected). Each register can be written (or read) serially by using the DI (or DO) pin.

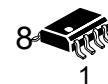
The ICs is purposed for reading, writing & nonvolatile data storage. ICs can be used in TV-sets, telecom equipment & consumer electronic devices.

FEATURES

- 100 year data (16K) retention for Ta=25°C;
- Single power supply source (V_{CC} = 1,8 V – 6,0 V);
- Build-in voltage multiplier;
- Serial I/O bus;
- Autoincrement of address word;
- Self-timed write cycle;
- 1,000,000 Program/erase cycles;
- Power-up internal logic setup;
- Read cycles quantity are not limited;
- Low power consumption;
- Operating temperature range -40 ... +85 °C.



N SUFFIX
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PIN FUNCTIONS

Pin Name	Function		
CS	Chip Select	CS	01
SK	Clock Input	SK	02
DI	Serial Data Input	DI	03
DO	Serial Data Output	DO	04
V _{CC}	+1.8 to 6.0V Power Supply	08	V _{CC}
GND	Ground	07	NC (ORG)
ORG	Memory Organization pin *	06	ORG
NC	No Connection	05	GND

Note

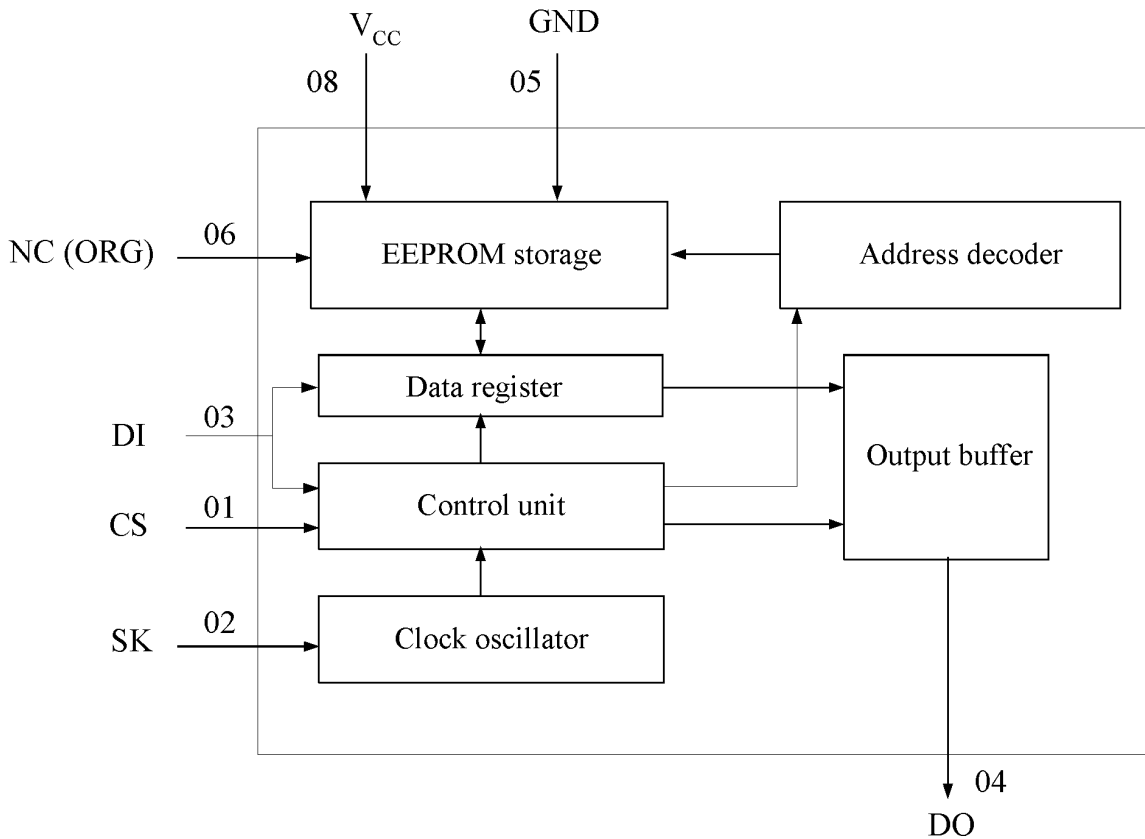
* this pin is present only in IN93AA86CN, IN93AA86CD:

When the ORG pin is connected to V_{CC}, the x16 organization is selected.

When it is connected to ground, the x8 pin is selected.

If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.

IN93AA86AN/AD, IN93AA86BN/BD, IN93AA86CN/CD Block Diagram



Recommended Operation Conditions & Maximum Ratings*

Parameter, unit	Symbol	Recommended Operation Conditions		Maximum Ratings		
		Min	Max	Min	Max	
Supply voltage, V	U_{CC}	1,8	6,0	- 0,5	7,0	
High level input voltage, V	U_{IH}	$4,5 V \leq U_{CC} \leq 5,5 V$	2,0	$U_{CC} + 1,0$	-0,5	$U_{CC} + 1,0$
		$1,8 V \leq U_{CC} < 4,5 V$	$0,7U_{CC}$	$U_{CC} + 1,0$		
Low level input voltage, V	U_{IL}	$4,0 V \leq U_{CC} \leq 5,5 V$	-0,1	0,8	- 0,5	-
		$1,8 V \leq U_{CC} < 4,0 V$	0	$0,2U_{CC}$		
Low level output current mA	I_{OL}	-	2,1	-	-	
Output short-circuit current, mA	$I_{OS}^{1)}$	-	-	-	100	

1) Time not more than 1 sec

Electric Parameters

Parameter, unit	Symbol	Mode	Min	Max	T _A , °C
Low level output voltage, V	U _{OL1}	4,5 V ≤ U _{CC} ≤ 5,5 V I _{OL} = 2,1 mA	–	0,4	25 ± 10; -45; 85
High level output voltage, V	U _{OH1}	4,5 V ≤ U _{CC} ≤ 5,5 V I _{OH} = -400 uA	2,4	–	
Low level output voltage, V	U _{OL2}	1,8 V ≤ U _{CC} < 4,5 V I _{OL} = 1 mA	–	0,2	
High level output voltage, V	U _{OH2}	1,8 V ≤ U _{CC} < 4,5 V I _{OH} = -100 uA	U _{CC} -0,2	–	
Low level input leakage current, uA	I _{ILL}	1,8 V ≤ U _{CC} ≤ 6,0 V	–	-1,0	
High level input leakage current, uA	I _{ILH}	U _I = U _{CC} 1,8 V ≤ U _{CC} ≤ 6,0 V	–	1,0	
Low level output leakage current, uA	I _{OLL}	U _O = U _{CC} U _{CS} = 0 V 1,8 V ≤ U _{CC} ≤ 6,0 V	–	-1,0	
High level output leakage current, uA	I _{OLH}	U _O = U _{CC} U _{CS} = 0 V 1,8 V ≤ U _{CC} ≤ 6,0 V	–	1,0	
Consumption current (8-bit mode), uA IN93AA86CN, IN93AA86CD IN93AA86AN, IN93AA86AD	I _{CC1}	U _{CC} = 5,5 V U _{CS} = 0 V U _{ORG} = 0 V ORG not connected	–	10	
Consumption current (16-bit mode), uA IN93AA86CN, IN93AA86CD IN93AA86AN, IN93AA86AD	I _{CC2}	U _{CC} = 5,5 V U _{CS} = 0 V U _{ORG} = U _{CC} or ORG not connected ORG not connected	–	10	
Consumption current (Operating Read), uA	I _{OCC R}	U _{CC} = 5,0 V f _C = 1 MHz	–	500	
Consumption current (Operating Write/Erase), mA	I _{OCC EW}	U _{CC} = 5,0 V f _C = 1 MHz	–	3,0	
Output Delay to Low, ns	t _{PD0}	4,5 V ≤ U _{CC} ≤ 6,0 V f _C = 3 MHz	–	150	
		2,5 V ≤ U _{CC} ≤ 6,0 V f _C = 1 MHz	–	500	
		1,8 V ≤ U _{CC} ≤ 6,0 V f _C = 0,5 MHz	–	1000	
Output Delay to High, ns	t _{PD1}	4,5 V ≤ U _{CC} ≤ 6,0 V f _C = 3 MHz	–	150	
		2,5 V ≤ U _{CC} ≤ 6,0 V f _C = 1 MHz	–	500	
		1,8 V ≤ U _{CC} ≤ 6,0 V f _C = 0,5 MHz	–	1000	

Parameter, unit	Symbol	Mode	Min	Max	T _A , °C
Output Delay to High-Z, ns	t _{HZ}	4,5 V ≤ U _{CC} ≤ 6,0 V f _C = 3 MHz	–	100	25 ± 10; -40; 85
		2,5 V ≤ U _{CC} ≤ 6,0 V f _C = 1 MHz	–	200	
		1,8 V ≤ U _{CC} ≤ 6,0 V f _C = 0,5 MHz	–	400	
Write/Erase cycle, ms	t _{CY}	4,5 V ≤ U _{CC} ≤ 6,0 V f _C = 3 MHz	–	10	
		2,5 V ≤ U _{CC} ≤ 6,0 V f _C = 1 MHz	–	10	
		1,8 V ≤ U _{CC} ≤ 6,0 V f _C = 0,5 MHz	–	10	
Output Delay to Status Check, ns	t _{SV}	4,5 V ≤ U _{CC} ≤ 6,0 V f _C = 3 MHz	–	100	
		2,5 V ≤ U _{CC} ≤ 6,0 V f _C = 1 MHz	–	500	
		1,8 V ≤ U _{CC} ≤ 6,0 V f _C = 0,5 MHz	–	1000	
Power-up to Read Operation Time, ms	t _{PUR}	4,5 V ≤ U _{CC} ≤ 6,0 V f _C = 3 MHz	–	1,0	
		2,5 V ≤ U _{CC} ≤ 6,0 V f _C = 1 MHz	–	1,0	
		1,8 V ≤ U _{CC} ≤ 6,0 V f _C = 0,5 MHz	–	1,0	
Power-up to Write Operation Time, ms	t _{PUW}	4,5 V ≤ U _{CC} ≤ 6,0 V f _C = 3 MHz	–	1,0	
		2,5 V ≤ U _{CC} ≤ 6,0 V f _C = 1 MHz	–	1,0	
		1,8 V ≤ U _{CC} ≤ 6,0 V f _C = 0,5 MHz	–	1,0	
Program/erase cycles	N _{E/W}	U _{CC} = 5,0 V	1000000	–	25 ± 10
Notes					
1. t _{PUR} & t _{PUW} times are delays from of power up to operation started					
2. U _{CS} , U _{ORG} – voltages applied to CS, ORG pins					

3-wire Interface Parameters (-40 °C ≤ T_A ≤ 85 °C, C_L=100 pF)

Symbol	Parameter, unit	1,8V ≤ U _{CC} ≤ 6,0V		2,5V ≤ U _{CC} ≤ 6,0 V		4,5V ≤ U _{CC} ≤ 6,0V	
		Min	Max	Min	Max	Min	Max
f _C	Clock frequency, MHz	-	0,25	-	0,5	-	2
t _{CSS}	CS Setup Time, ns	200	-	100	-	50	-
t _{CSH}	CS Hold Time, ns	0	-	0	-	0	-
t _{DIS}	DI Setup Time, ns	200	-	100	-	50	-
t _{DIH}	DI Hold Time, ns	200	-	100	-	50	-
t _{CS MIN}	Minimum CS Low Time, ns	1000	-	500	-	150	-
t _{SKHI}	Minimum SK High Time, ns	1000	-	500	-	150	-
t _{SKLOW}	Minimum SK Low Time, ns	1000	-	500	-	150	-

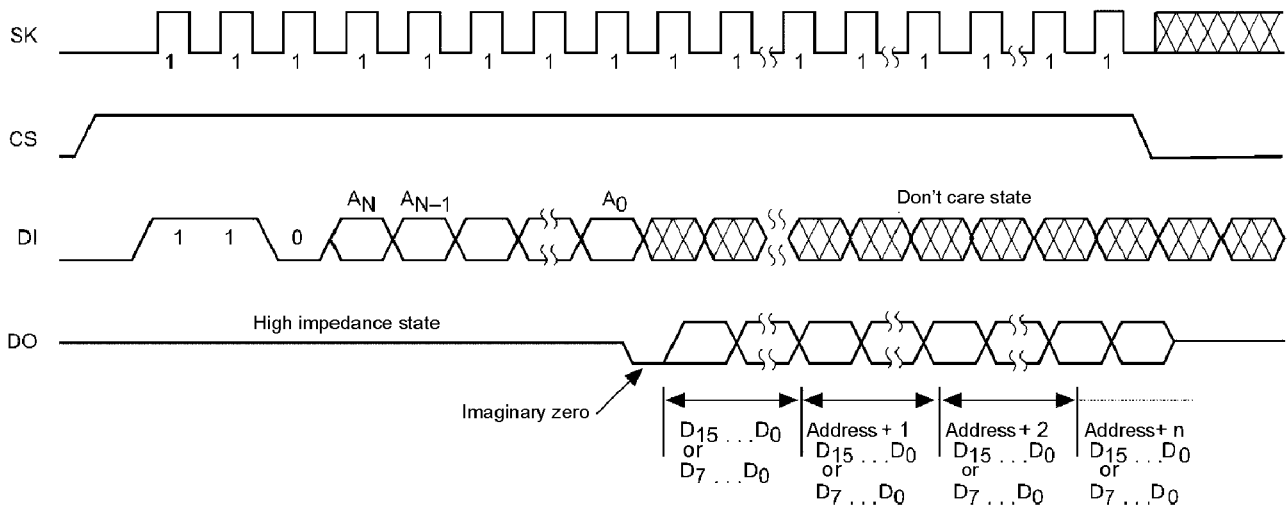
Instruction Set

Instruction	Start Bit	Op-code	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A10-A0	A9-A0			Read Address AN- AO
ERASE	1	11	A10-A0	A9-A0			Clear Address AN- AO
WRITE	1	01	A10-A0	A9-A0	D7-D0	D15-D0	Write Address AN- AO
EWEN	1	00	11XXXXXXXXXX	11XXXXXXXXXX			Write Enable
EWDS	1	00	00XXXXXXXXXX	00XXXXXXXXXX			Write Disable
ERAL	1	00	10XXXXXXXXXX	10XXXXXXXXXX			Clear All Addresses
WRAL	1	00	01XXXXXXXXXX	01XXXXXXXXXX	D7-D0	D15-D0	Write All Addresses

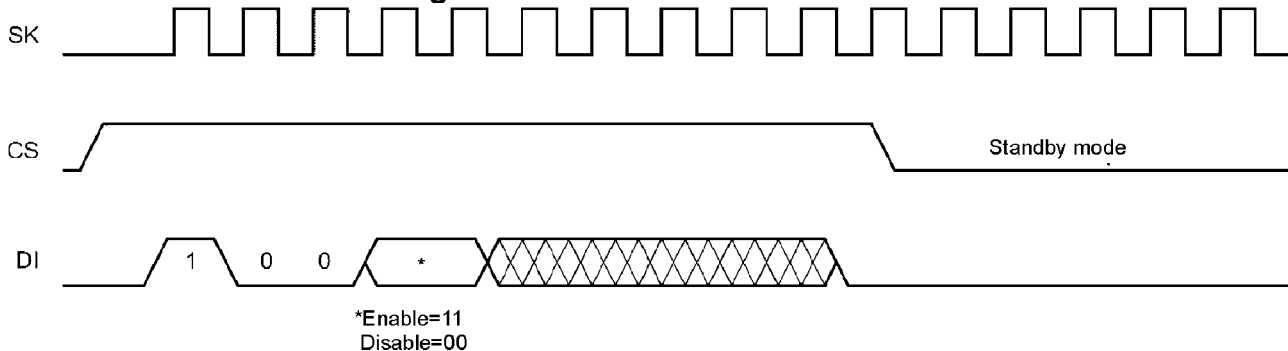
There are 7 instructions to execute WRITE, ERASE or READ operation

The format for all instructions sent to the device is a logical "1" start bit, a 2-bits (or 4-bits) operation code, 10-bit address (1024x16)/ 11-bit address (2048x8).

A 16-bit data field (organization 1024x16) or 8-bit data field (organization 4058x8) is additionally required for write operations.



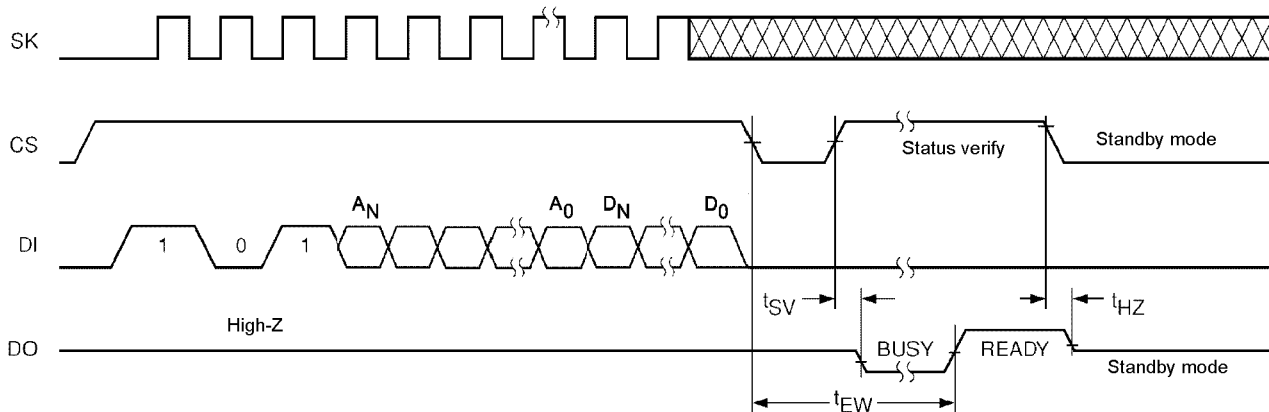
Read Instruction Timing



EWEN/EWDS Instruction Timing

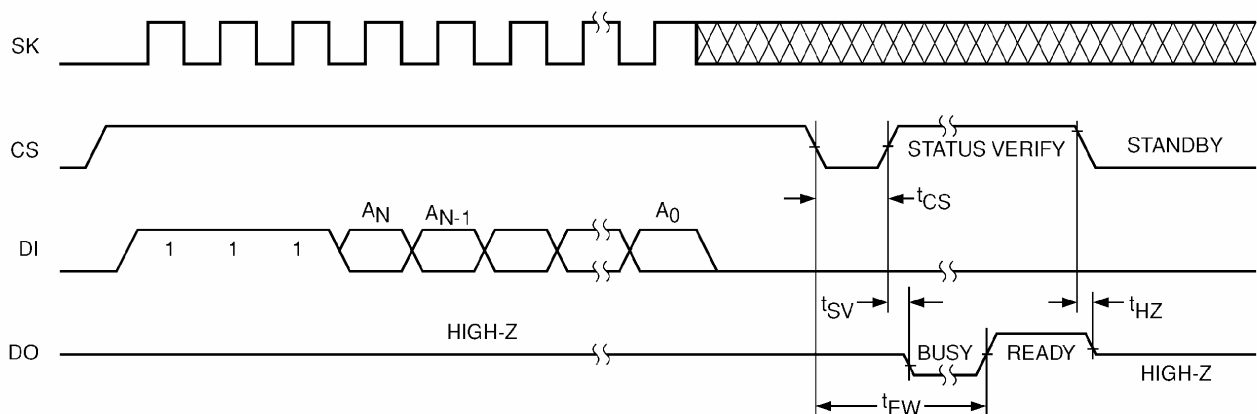
The IN93AA86 powers up switch IC to the write disable state. Any writing after power-up

or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction.



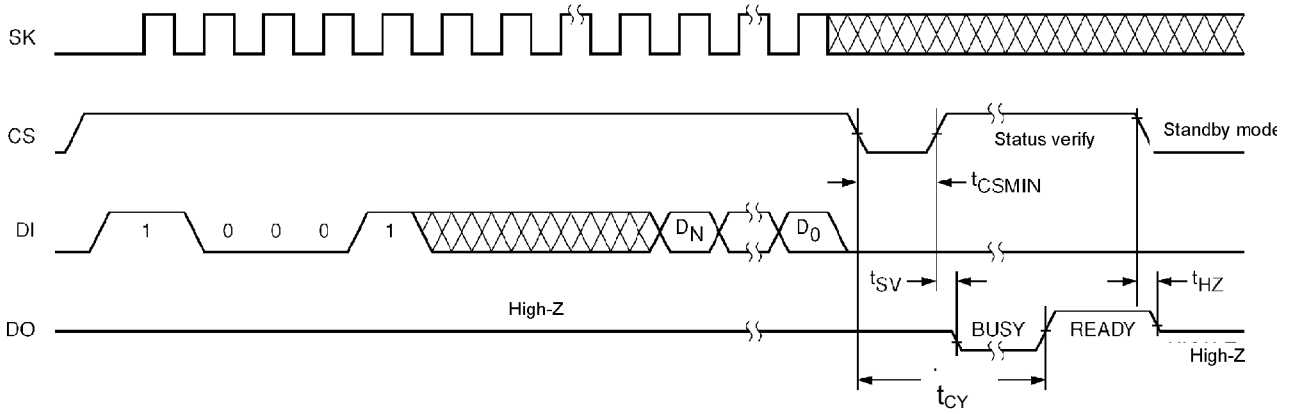
ERAL Instruction Timing

The IN93AA86 ignore all external signals applied to SK and DI pins during cycle of active programming. Erase/write cycle duration (t_{CY}) can be measured (controlled) by scanning of IC output. Low level (logical "0") means that programming still in progress, high level (logical "1") means that programming is already completed. Transition of output to High-Z state after programming cycle was completed is executed by applying low level (logic "0") to CS pin or applying high level (logical "1") to DI pin (for case CS = 1).

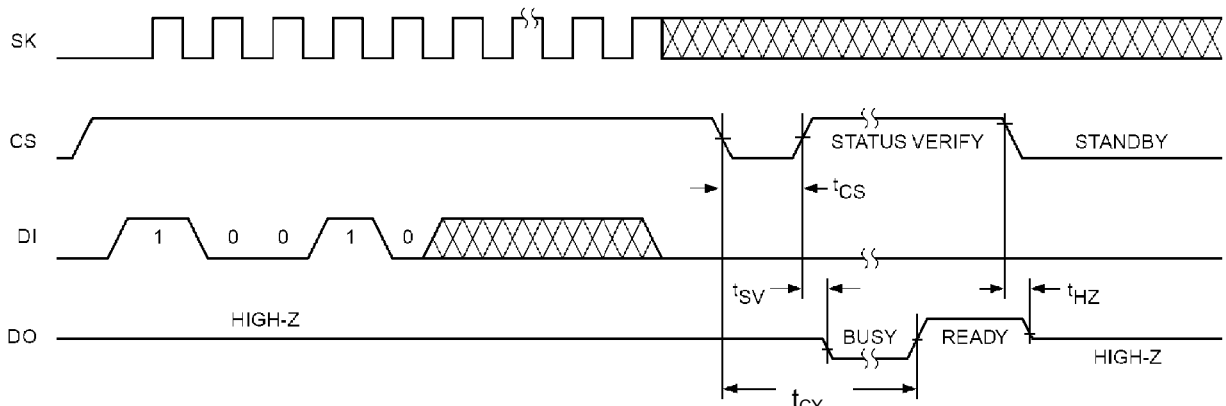


ERASE Instruction Timing

Once cleared, the content of a cleared location returns to a logical "1" state.

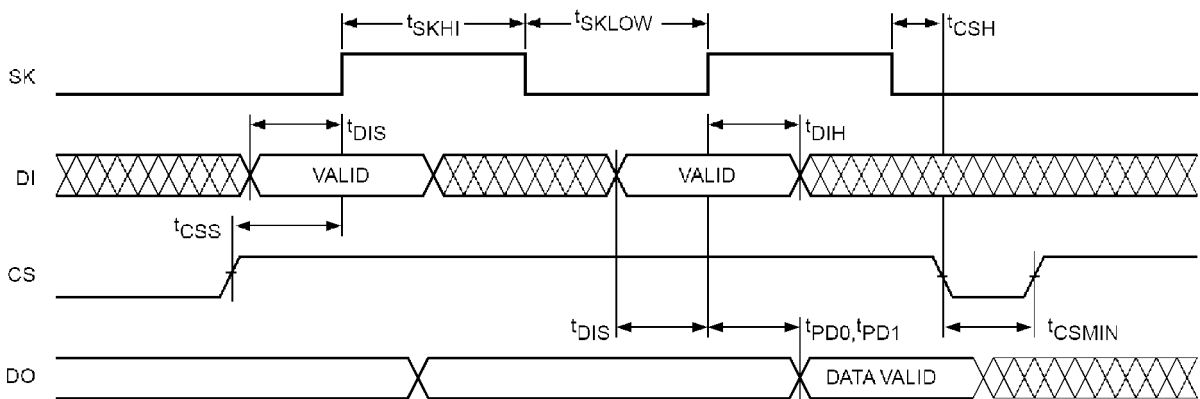


WRAL Instruction Timing



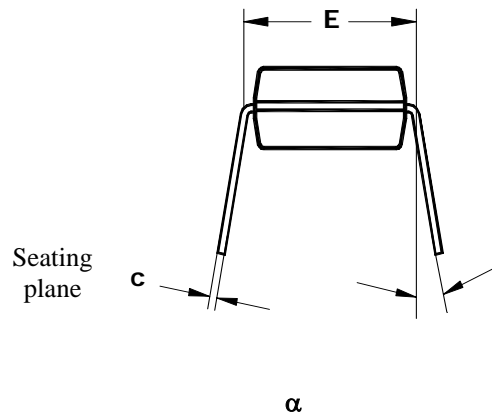
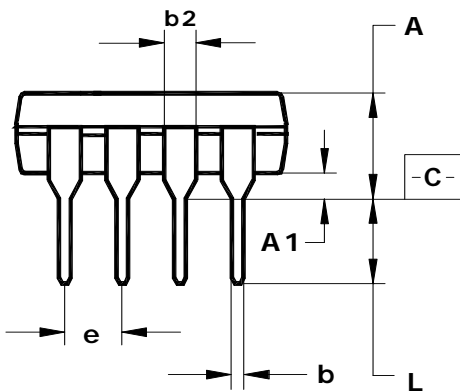
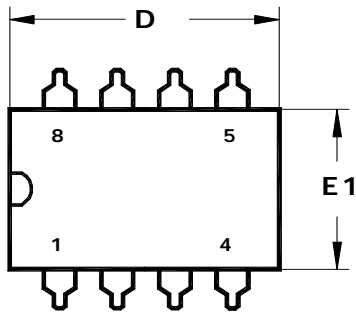
Once cleared, the contents of all memory bits return to a logical "1" state.

ERAL Instruction Timing



Synchronous Data Timing

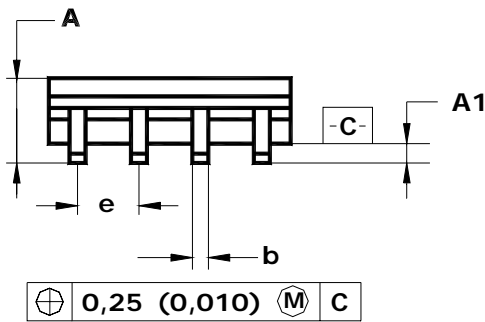
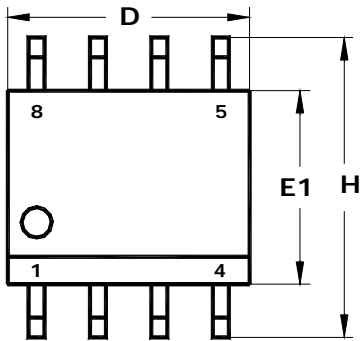
N SUFFIX PLASTIC DIP
(MS-001BA)



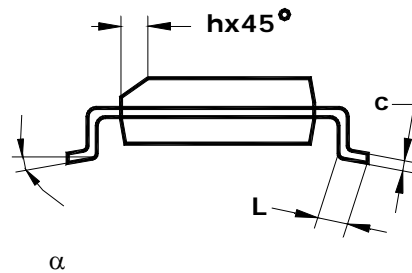
⊕ 0,25 (0,010) Ⓜ C

	D	E1	A	b	b2	e	α	L	E	c	A1
mm											
min	9.02	6.07	—	0.36	1.14		0°	2.93	7.62	0.20	0.38
max	10.16	7.11	5.33	0.56	1.78	2.54	15°	3.81	8.26	0.36	—
inches											
min	0.355	0.240	—	0.014	0.045		0°	0.115	0.300	0.008	0.015
max	0.400	0.280	0.210	0.022	0.070	0.1	15°	0.150	0.325	0.014	—

D SUFFIX PLASTIC SOP (MS-012AA)

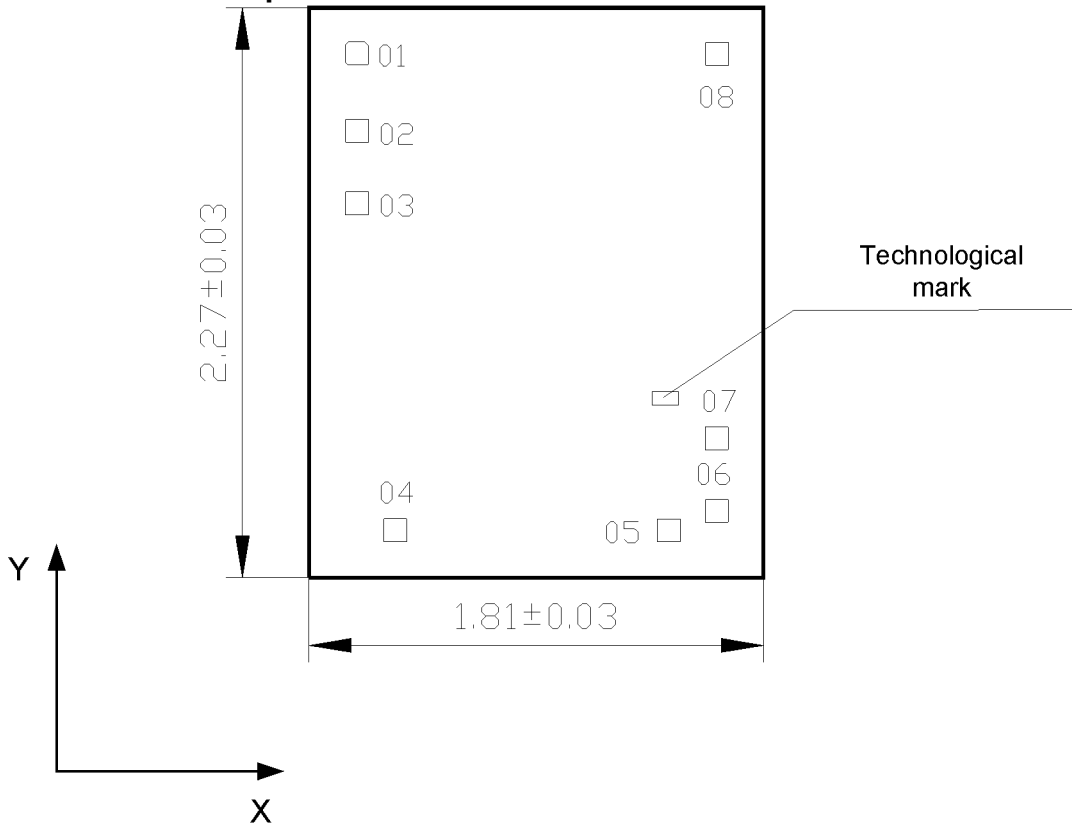


Seating
plane



	D	E1	H	b	e	α	A	A1	c	L	h
mm											
min	4.80	3.80	5.80	0.33		0°	1.35	0.10	0.19	0.41	0.25
max	5.00	4.00	6.20	0.51	1.27	8°	1.75	0.25	0.25	1.27	0.50
inches											
min	0.1890	0.1497	0.2284	0.013		0°	0.0532	0.0040	0.0075	0.016	0.0099
max	0.1968	0.1574	0.2440	0.020	0.100	8°	0.0688	0.0090	0.0098	0.050	0.0196

Die dimension & contact pad location



Technology mark coordinates, mm: left bottom corner $x = 1,383$, $y = 0,653$.
 Die thickness $0,46 \pm 0,02$ mm.

Pad location table

Pad number	Coordinates (left bottom corner), mm		Contact pad description
	X	Y	
01	0,1428	2,0412	CS
02	0,1451	1,7328	SK
03	0,1451	1,444	DI
04	0,2970	0,1427	DO
05	1,3870	0,1422	GND
06	1,5785	0,2199	NC (ORG*)
07	1,5785	0,5087	WE
08	1,5797	2,0405	Vcc

Note: Contact pad coordinates and dimensions 0,092 x 0,092 mm are indicated according passivation layer

* For ICs IN93AA86CN/CD