3.0 GHz Low Noise Silicon MMIC Amplifier

Technical Data

INA-54063

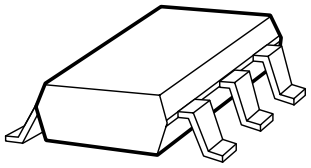
Features

- **Ultra-Miniature Package**
- **Single 5 V Supply (29 mA)**
- **21.5 dB Gain (1.9 GHz)**
- **8.0 dBm P_{1dB} (1.9 GHz)**
- **Positive Gain Slope**
- **Unconditionally Stable**

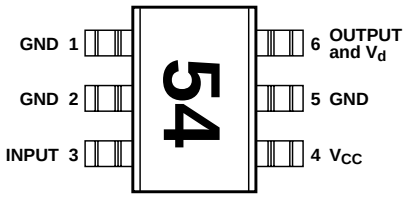
Applications

- **IF Amplifier for DBS Downconverter, Cellular, Cordless, Special Mobile Radio, PCS, ISM, and Wireless LAN Applications**

Surface Mount Package SOT-363 (SC-70)



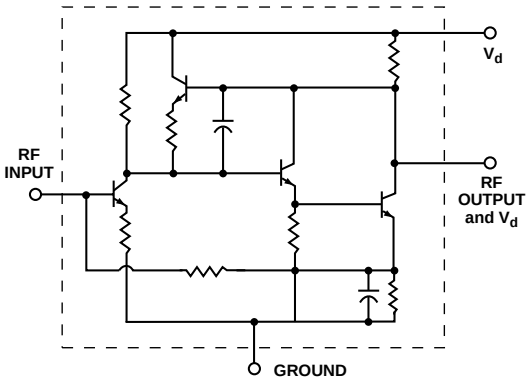
Pin Connections and Package Marking



Note:
Package marking provides orientation and identification.

Equivalent Circuit

(Simplified)



Description

Hewlett-Packard's INA-54063 is a Silicon monolithic amplifier that offers excellent gain and power output for applications to 3.0 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

With its wide bandwidth and high linearity, the INA-54063 is an excellent candidate for DBS IF applications. It also features a unique gain curve which increases over the range from 1 to 2 GHz. This gain slope compensates for the gain rolloff found in typical receiver systems.

The INA-54063 is fabricated using HP's 30 GHz f_{MAX} ISOSAT™ Silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metalization, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity, and reliability.

INA-54063 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Supply Voltage, to Ground	V	12
P_{in}	CW RF Input Power	dBm	13
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{j\text{-}c} = 165°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

Electrical Specifications, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_d = 5$ V, unless noted

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.	Std. Dev.[1]
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1900 MHz	dB	19	21.5		0.7
NF	Noise Figure	f = 1900 MHz	dB		5.0		0.4
P_{1dB}	Output Power at 1 dB Gain Compression	f = 1900 MHz	dBm		8.0		
IP_3	Third Order Intercept Point	f = 1900 MHz f = 2150 MHz	dBm		17 15.7		
$VSWR_{in}$	Input VSWR	f = 1900 MHz			1.4		
$VSWR_{out}$	Output VSWR	f = 1900 MHz			2.4		
I_d	Device Current		mA		29	36	1.8
t_d	Group Delay	f = 1900 MHz	ps		272		

Note:
1. Standard deviation number is based on measurement of at least 500 parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.

INA-54063 Typical Performance

$T_C = 25°C, Z_O = 50\,\Omega, V_d = 5\,V$, unless noted

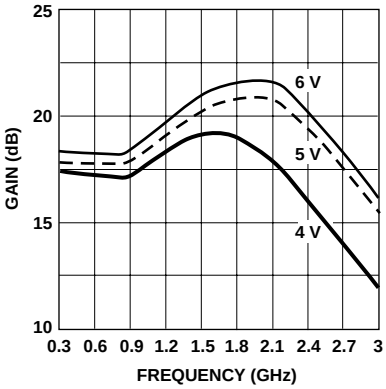


Figure 1. Gain vs. Frequency and Voltage.

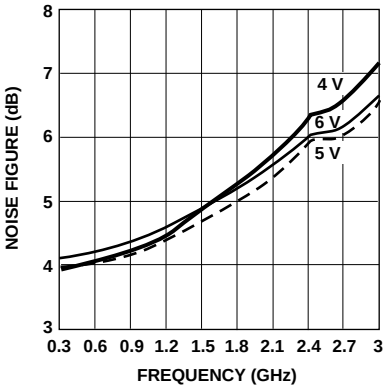


Figure 2. Noise Figure vs. Frequency and Voltage.

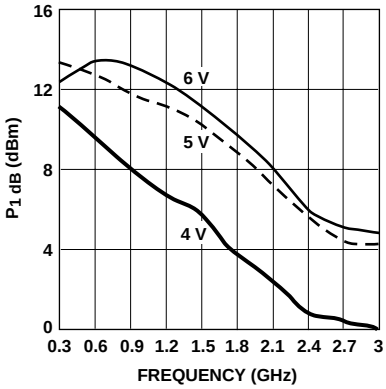


Figure 3. Output Power for 1 dB Gain Compression vs. Frequency and Voltage.

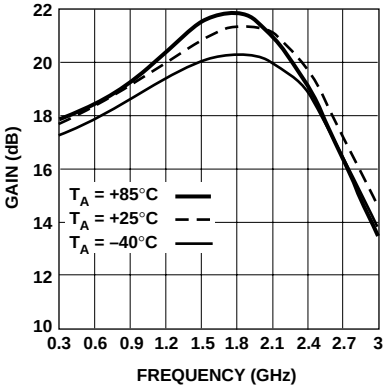


Figure 4. Gain vs. Frequency and Temperature.

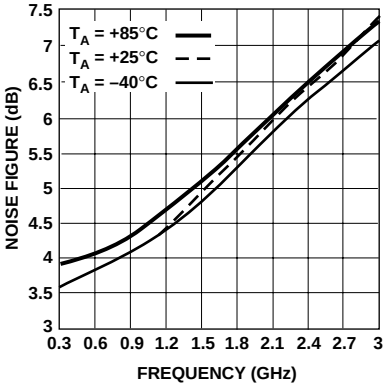


Figure 5. Noise Figure vs. Frequency and Temperature.

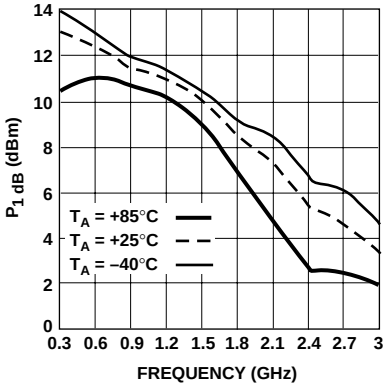


Figure 6. Output Power for P_{1dB} Gain Compression vs. Frequency and Temperature.

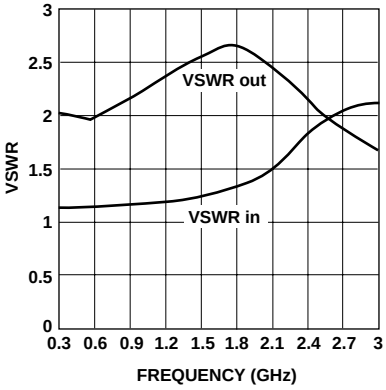


Figure 7. Input and Output VSWR vs. Frequency.

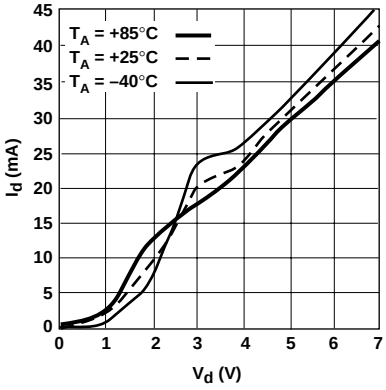


Figure 8. Supply Current vs. Voltage and Temperature.

INA-54063 Typical Scattering Parameters[1], $T_C = 25°C, Z_O = 50\,\Omega, V_d = 5.0\,V$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Factor
0.10	0.11	91	16.9	7.02	19	-27.7	0.04	21	0.47	75	1.50
0.20	0.09	64	17.6	7.56	2	-27.1	0.04	7	0.35	34	1.47
0.30	0.08	51	17.7	7.71	-7	-27.0	0.04	0	0.32	10	1.46
0.40	0.09	42	17.9	7.81	-14	-27.1	0.04	-5	0.31	-7	1.46
0.50	0.08	46	18.1	8.00	-21	-27.3	0.04	-9	0.30	-23	1.47
0.60	0.09	39	18.2	8.11	-27	-27.5	0.04	-12	0.30	-36	1.47
0.70	0.09	32	18.3	8.24	-33	-27.8	0.04	-15	0.31	-47	1.48
0.80	0.09	22	18.5	8.41	-39	-28.1	0.04	-17	0.33	-56	1.48
0.90	0.10	13	18.7	8.58	-45	-28.4	0.04	-19	0.34	-65	1.48
1.00	0.10	5	18.9	8.80	-51	-28.8	0.04	-21	0.35	-73	1.48
1.10	0.11	-3	19.1	9.05	-57	-29.2	0.03	-23	0.37	-80	1.48
1.20	0.11	-11	19.4	9.28	-64	-29.6	0.03	-25	0.38	-88	1.50
1.30	0.12	-20	19.6	9.58	-70	-30.1	0.03	-26	0.39	-94	1.50
1.40	0.12	-29	19.9	9.88	-78	-30.6	0.03	-27	0.40	-101	1.52
1.50	0.13	-36	20.2	10.19	-85	-31.1	0.03	-28	0.41	-108	1.54
1.60	0.14	-44	20.4	10.51	-93	-31.5	0.03	-29	0.41	-114	1.55
1.70	0.15	-53	20.7	10.86	-101	-32.0	0.03	-30	0.42	-120	1.57
1.80	0.16	-61	21.0	11.16	-111	-32.7	0.02	-31	0.42	-126	1.63
1.90	0.17	-68	21.1	11.36	-120	-33.5	0.02	-31	0.41	-132	1.74
2.00	0.20	-73	21.2	11.44	-130	-34.2	0.02	-29	0.40	-138	1.87
2.10	0.22	-80	21.2	11.43	-141	-34.9	0.02	-29	0.38	-144	2.04
2.20	0.24	-89	21.0	11.25	-152	-35.6	0.02	-28	0.37	-148	2.22
2.30	0.26	-99	20.7	10.86	-164	-36.0	0.02	-27	0.35	-151	2.41
2.40	0.27	-108	20.1	10.16	-175	-36.8	0.01	-26	0.34	-155	2.82
2.50	0.28	-112	19.5	9.39	175	-37.8	0.01	-24	0.32	-158	3.42
2.60	0.29	-117	18.6	8.55	166	-39.0	0.01	-23	0.31	-162	4.31
2.70	0.30	-124	17.8	7.79	157	-39.3	0.01	-15	0.29	-164	4.94
2.80	0.30	-130	16.9	7.03	150	-39.6	0.01	-16	0.28	-166	5.69
2.90	0.30	-133	16.1	6.35	144	-41.6	0.01	-15	0.26	-170	8.05
3.00	0.30	-136	15.3	5.83	138	-42.5	0.01	-5	0.25	-171	9.80
3.10	0.31	-138	14.6	5.35	132	-43.7	0.01	3	0.23	-173	12.33
3.20	0.31	-140	13.8	4.92	127	-45.4	0.01	13	0.22	-174	16.36
3.30	0.31	-142	13.2	4.57	121	-45.4	0.01	31	0.21	-174	17.56
3.40	0.31	-143	12.5	4.23	116	-45.7	0.01	47	0.20	-174	19.78
3.50	0.32	-145	11.9	3.93	111	-44.8	0.01	65	0.19	-174	19.14
3.60	0.32	-147	11.2	3.65	106	-43.4	0.01	75	0.19	-174	17.63
3.70	0.33	-148	10.6	3.38	101	-42.2	0.01	82	0.18	-174	16.53
3.80	0.34	-149	9.9	3.11	96	-41.1	0.01	88	0.18	-175	15.72
3.90	0.35	-152	9.1	2.84	92	-40.3	0.01	93	0.17	-175	15.60
4.00	0.35	-156	8.4	2.62	89	-39.3	0.01	99	0.16	-174	15.11
4.10	0.34	-159	7.8	2.46	85	-38.0	0.01	103	0.14	-171	14.09
4.20	0.33	-161	7.1	2.27	79	-37.6	0.01	104	0.13	-156	14.64
4.30	0.32	-161	5.6	1.91	75	-37.6	0.01	112	0.19	-135	17.07
4.40	0.33	-161	4.5	1.68	81	-35.8	0.02	127	0.31	-150	14.81
4.50	0.34	-162	4.8	1.73	82	-33.4	0.02	129	0.33	-170	10.72
4.60	0.35	-166	4.9	1.75	80	-31.7	0.03	128	0.32	180	8.78
4.70	0.35	-170	4.8	1.74	76	-30.4	0.03	126	0.30	173	7.69
4.80	0.33	-173	4.6	1.69	72	-29.3	0.03	124	0.30	167	7.09
4.90	0.34	-174	4.2	1.62	69	-28.2	0.04	123	0.29	164	6.57
5.00	0.34	-177	3.9	1.57	66	-27.2	0.04	122	0.29	160	6.04

Note 1: Reference plane per Figure 14 in Applications Information section.

INA-54063 Applications Information

Introduction

The INA-54063 is a silicon RFIC amplifier that is designed with an internal resistive feedback network to provide a 50 Ω input and near 75 Ω output impedance. With a 1-dB compressed Output Power of 8 dBm and Noise Figure of 5 dB, the INA-54063 is well suited for amplifier applications requiring high dynamic ranges.

A unique feature of the INA-54063 is a positive gain slope over the 1–2 GHz range that is useful in many satellite-based TV and datacom systems. When used for the IF amplifier, the up-slope in the gain of the INA-54063 is intended to compensate for the negative gain slope in many Low Noise Block downconverters (LNB) used in consumer and commercial TV delivery systems, such as DDS, DBS, and TVRO. The positive gain slope can also compensate for the high frequency attenuation characteristics of 75 Ω cables used to connect the outdoor LNBs to indoor set-top converters.

In addition to use in TV delivery systems, the INA-54063 will find many applications in 50 Ω input-50 Ω output gain and buffer stages in wireless communications systems.

Operating Details

The INA-54063 is a voltage biased device that operates from a +5 volt power supply with a typical current drain of 29 mA. All bias regulation circuitry is integrated into the RFIC. Figure 9 shows a typical implementation of the INA-54063. The supply voltage for the INA-54063 must be applied to two terminals, the V_{cc} pin and the RF Output pin.

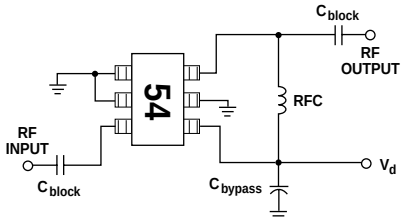


Figure 9. Basic Amplifier Application.

The V_d connection to the amplifier is RF bypassed by placing a capacitor to ground near the V_d pin of the amplifier package. The power supply connection to the RF Output pin is achieved by means of an RF choke (inductor). The value of the RF choke must be large relative to 50/75 Ω in order to prevent loading of the RF Output.

The supply voltage end of the RF choke is bypassed to ground with a capacitor. If the physical layout permits, this can be the same bypass capacitor that is used at the V_d terminal of the amplifier. Blocking capacitors are normally placed in series with the RF Input and the RF Output to isolate the DC voltages on these pins from circuits adjacent to the amplifier. The values for the blocking and bypass capacitors are selected to provide a reactance at the lowest frequency of operation that is small relative to 50 Ω.

Example Layout for 50 Ω Amplifier

An example layout for an amplifier using the INA-54063 with 50 Ω input and 50 Ω output is shown in Figure 10.

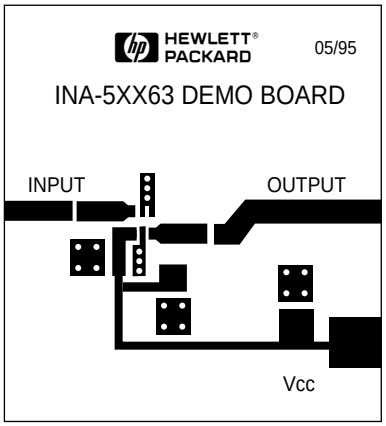


Figure 10. RF Layout for 50 Ω Input and Output.

This example uses a microstripline design (solid groundplane on the back side of the circuit board). The circuit board material is 0.031-inch thick FR-4. Plated through holes (vias) are used to bring the ground to the top side of the circuit where needed. Multiple vias are used to reduce the inductance of the path to ground.

Figure 11 shows an assembled amplifier. The +5 volt supply (V_{cc}) is fed directly into the V_d pin of the INA-54063 and into the RF Output pin through the RF choke (RFC). Capacitor C3 provides RF bypassing for both the V_d pin and the power supply end of the RFC.

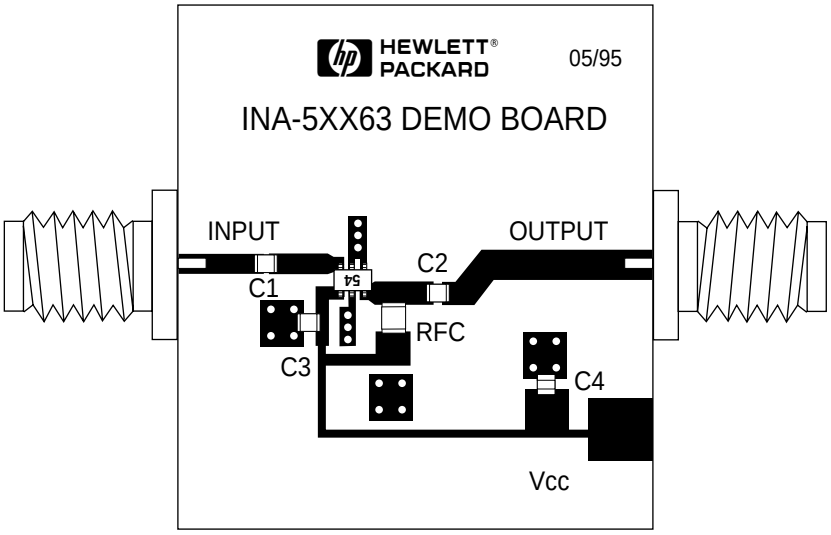


Figure 11. Assembled 50 Ω Amplifier.

Capacitor C4 is optional and may be used to add additional bypassing for the V_{cc} line. A well bypassed V_{cc} line is especially necessary in cascades of amplifier stages to prevent oscillation that may occur as a result of RF feedback through the power supply lines.

For this demonstration circuit, the value chosen for the RF choke was 220 nH (Coilcraft 1008CS-221 or equivalent). All of the blocking and bypass capacitors are 1000 pF. These values provide excellent amplifier performance from under 50 MHz through 2.5 GHz. Larger values for the choke and capacitors can be used to extend the lower end of the bandwidth. Since the gain of the INA-54063 extends down to DC, the frequency response of the amplifier is limited only by the values of the capacitors and choke.

A convenient method for making RF connection to the demonstration board is to use a PCB mounting type of SMA connector (Johanson 142-0701-881, or equivalent). These connectors can be slipped over the edge of the PCB and the center conductors soldered to the input and output lines. The ground pins of the connectors are soldered to the ground plane on the backside of the board. The extra ground pins for the top of the board are not needed and are clipped off.

The measured test results for the 50 Ω input/output example amplifier using the INA-54063 are shown in Figures 12 and 13.

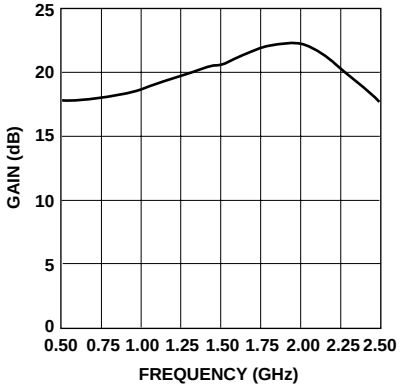


Figure 12. Measured Gain of 50 Ω Example Amplifier.

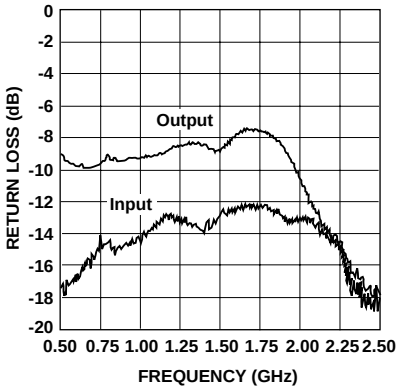


Figure 13. Measured Input and Output Return Loss for 50 Ω Example Amplifier.

PCB Materials

Typical choices for PCB material for low cost wireless applications are FR-4 or G-10 with a thickness of 0.025 or 0.031 inches. A thickness of 0.062 inches is the maximum that is recommended for use with this particular device. The use of a thicker board material increases the inductance of the plated through vias used for RF grounding and may deteriorate circuit performance. Adequate grounding is needed not only to obtain maximum amplifier performance but also to reduce any possibility of instability.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters for this device are shown in Figure 14. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

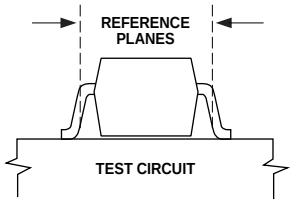


Figure 14. Phase Reference Planes.

SOT-363 PCB Layout

The INA-54063 is packaged in the miniature SOT-363 (SC-70) surface mount package. A PCB pad layout for the SOT-363 package is shown in Figure 15 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding pad parasitics that could impair the high frequency performance of the INA-54063. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads for reference.

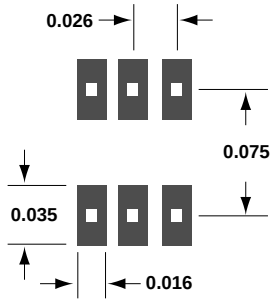


Figure 15. PCB Pad Layout for INA-54063 (dimensions in inches).

Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either "minimum or maximum," "typical," or "standard deviations." The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on of a minimum of 500 parts taken from 3 non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard "bell curve."

Parameters considered to be the most important to system performance are bounded by *minimum* or *maximum* values. For the INA-54063, these parameters are: Power Gain ($|S_{21}|^2$), Noise Figure (NF), and Device Current (I_d). Each of these guaranteed parameters is 100% tested.

Values for most of the parameters in the table of Electrical Specifications that are described by *typical* data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as S-parameters or Noise Parameters and the performance curves, the data represents a nominal part taken from the "center" of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate circuit using the INA-54063, but to also optimize and evaluate trade-offs that affect a complete wireless system, the *standard deviation* (σ) is provided for many of the Electrical Specifications parameters (at 25°C) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean.

Referring to Figure 16 for example, the probability of a parameter being between $\pm 1\sigma$ is 68.3%; between $\pm 2\sigma$ is 95.4%; and between $\pm 3\sigma$ is 99.7%.

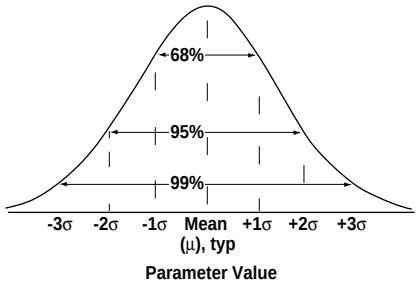


Figure 16. Normal Distribution.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-363 package, will reach solder reflow temperatures faster than those with a greater mass.

The INA-54063 is has been qualified to the time-temperature profile shown in Figure 17. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the

board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235°C.

These parameters are typical for a surface mount assembly process for the INA-54063. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

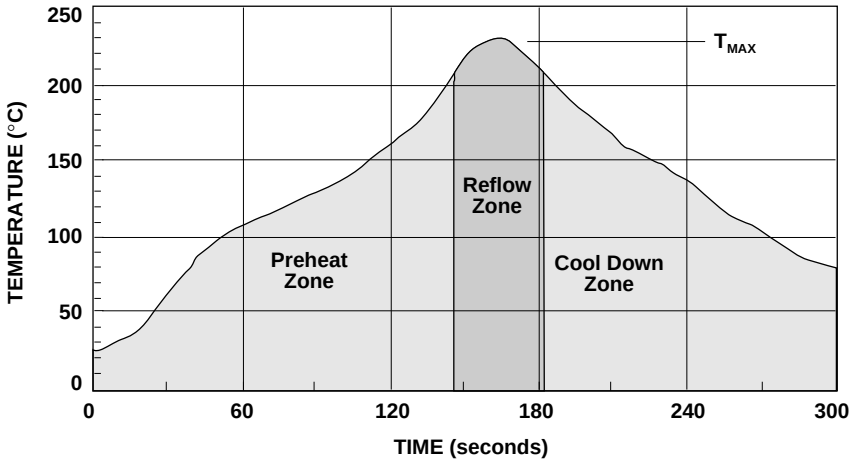


Figure 17. Surface Mount Assembly Profile.

Electrostatic Sensitivity

RFICs are electrostatic discharge (ESD) sensitive devices. Although the INA-54063 is robust in design, permanent damage may occur to these devices if they are subjected to high energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without detection and may result in degradation in performance, reliability, or failure. Electronic devices may be subjected to ESD damage in any of the following areas:

- Storage and handling
- Inspection and testing
- Assembly
- In-circuit use

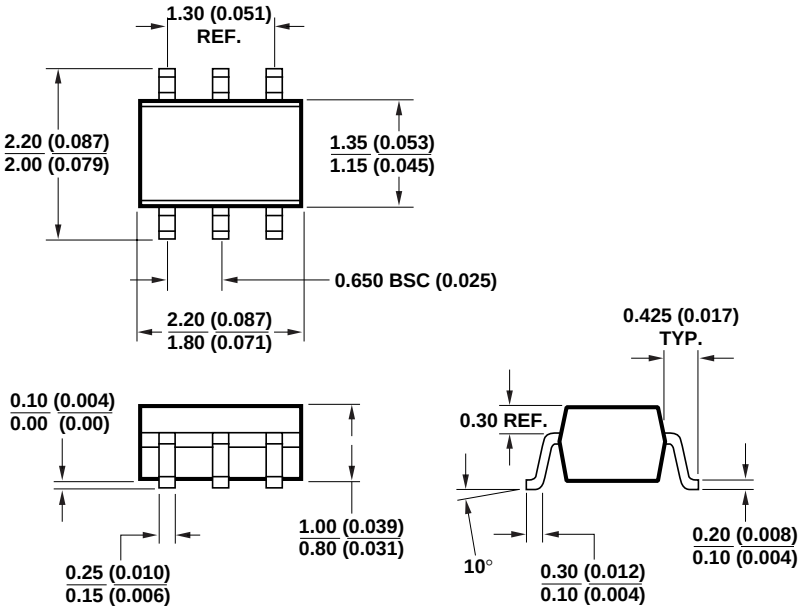
The INA-54063 is an ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, testing, assembling, and using these devices to avoid damage.

INA-54063 Part Number Ordering Information

Part Number	Devices per Container	Container
INA-54063-TR1	3000	7" reel
INA-54063-BLK	100	tape strip in antistatic bag

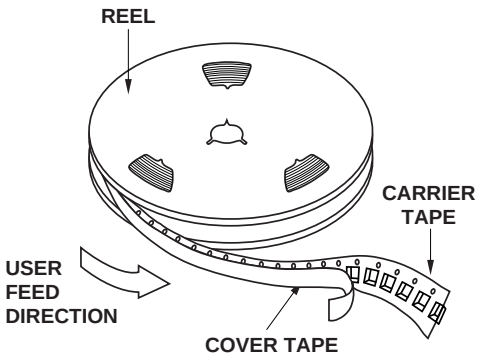
Package Dimensions

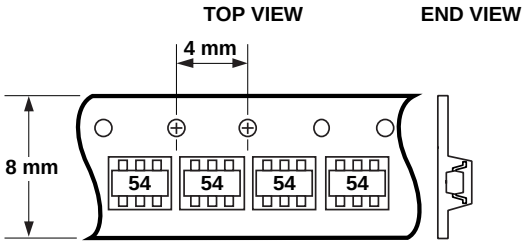
Outline 63 (SOT-363/SC-70)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

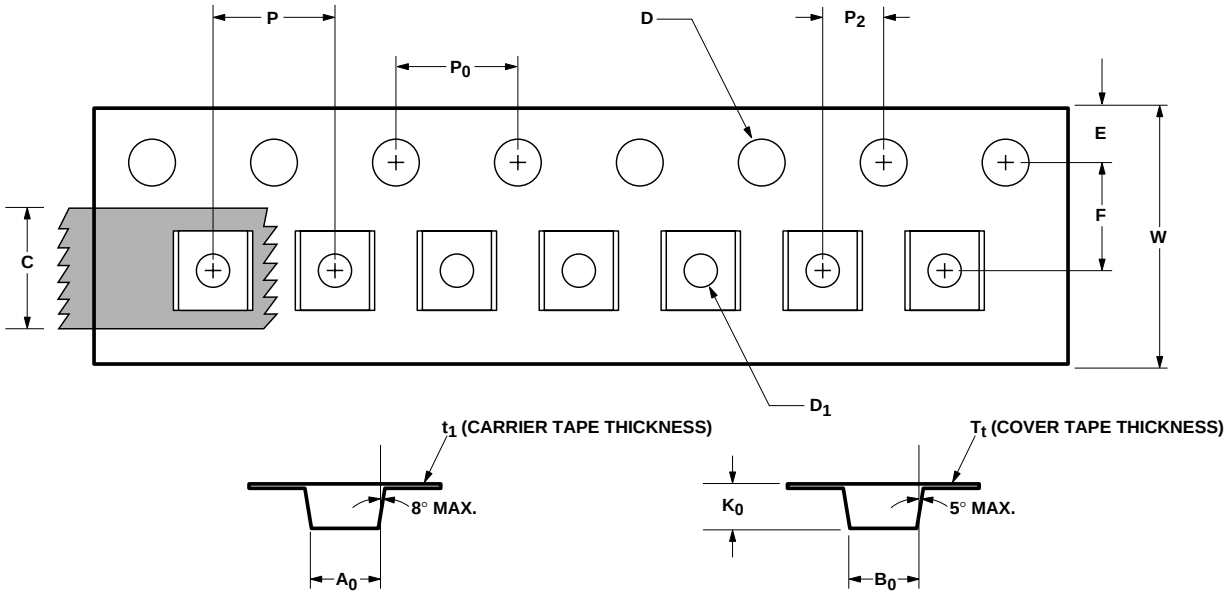
Device Orientation





Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002