1. FEATURES

- Easy to use
  - Gain set with one external resistor (gain range 1 to 10,000)
  - Wide power supply range (±2V to ±19V)
  - Higher performance than 3 op amp IA designs
  - Available in 8-lead SOIC packaging
  - Low power, 1.56mA supply current
- Excellent dc performance
  - 12μV max, input offset voltage
  - 3.0nA max, input bias current
  - 110dB min common-mode rejection ratio (G = 10)
- Low noise
  - 14nV/$\sqrt{Hz}$ @ 1kHz, input voltage noise
  - 3μV_{PP} noise (0.1Hz to 10Hz)
- Excellent ac specifications
  - 1300kHz bandwidth (G = 1)
  - 75μs settling time to 0.01%
- Operating temperature
  - INA101: –40°C to 85°C
  - INA102: –55°C to 125°C

2. APPLICATIONS

- Weigh scales
- ECG and medical instrumentation
- Transducer interface
- Data acquisition systems
- Industrial process controls
- Battery-powered and portable equipment

3. DESCRIPTION

The INA101/2 is a low cost, high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000. Furthermore, the INA101/2 features 8-lead SOIC packaging that is smaller than discrete designs and offers lower power (only 1.56mA supply current), making it a good fit for battery-powered, portable (or remote) applications.

The INA101/2, with its high accuracy of 0.8ppm maximum nonlinearity, low offset voltage of 12μV max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the INA101/2 make it well suited for medical applications, such as ECG and noninvasive blood pressure monitors.

The INA101/2 works well as a preamplifier due to its low input voltage noise of 14nV/$\sqrt{Hz}$ at 1kHz, 3μV_{PP} in the 0.1Hz to 10Hz band, and 0.35pA/$\sqrt{Hz}$ input current noise. Also, the INA101/2 is well suited for multiplexed applications with its settling time of 75μs to 0.01%, and its cost is low enough to enable designs with one in-amp per channel. See Table 1 for the order information.

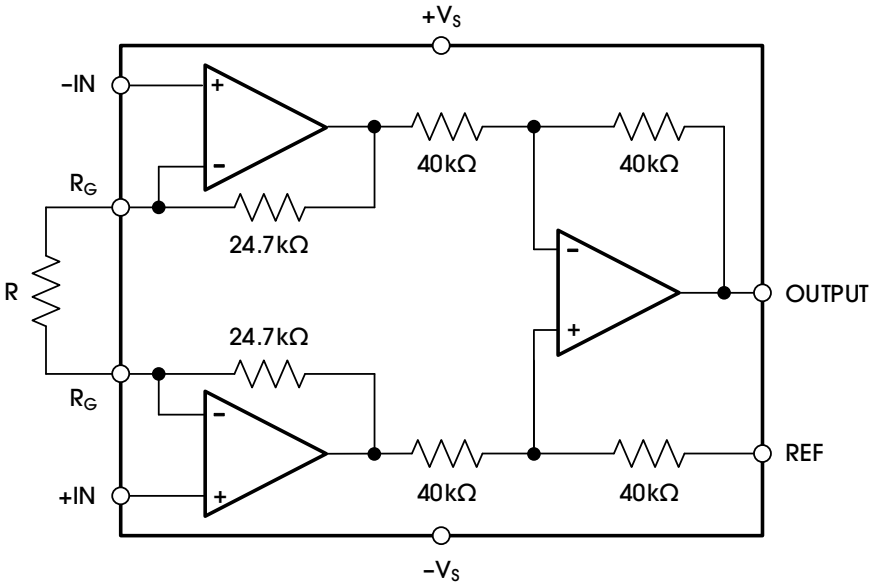


Table 1 lists the order information.

Table 1. Order Information

ORDER NUMBER	CH (#)	PACKAGE	MARK	I_Q PER CH (TYP) (mA)	BW (kHz)	GAIN	GAIN TYPE	OPERATING TEMP (°C)	PACKAGE OPTION
INA101ASOIC8	1	SOIC-8	INA101	1.56	1300	1-10000	R_G	–40-85	T/R-4000
INA102ASOIC8	1	SOIC-8	INA102	1.56	1300	1-10000	R_G	–55-125	T/R-4000

Table 2. Family Selection Guide

ORDER NUMBER	CH (#)	PACKAGE	MARK	I_Q PER CH (TYP) (mA)	BW (kHz)	GAIN	GAIN TYPE	OPERATING TEMP (°C)	PACKAGE OPTION
INA111ASOIC8(1)	1	SOIC-8	INA111	0.35	130	1-10000	R_G	–40-85	T/R-4000
INA112ASOIC8(1)	1	SOIC-8	INA112	0.35	130	1-10000	R_G	–55-125	T/R-4000
INA201ASOIC8(1)	1	SOIC-8	INA201	1.56	2560	10-100	R_G and OS	–40-125	T/R-4000
INA202ASOIC8(1)	1	SOIC-8	INA202	1.56	2560	10-100	R_G and OS	–55-125	T/R-4000
INA211ASOIC8(1)	1	SOIC-8	INA211	0.35	130	10-100	R_G and OS	–40-125	T/R-4000
INA212ASOIC8(1)	1	SOIC-8	INA212	0.35	130	10-100	R_G and OS	–40-125	T/R-4000
INA501LASOIC8(1)	1	SOIC-8	INA501L	1.56	1300	2	Fixed	–40-125	T/R-4000
INA501MASOIC8(1)	1	SOIC-8	INA501M	1.56	1300	5	Fixed	–40-125	T/R-4000
INA501HASOIC8(1)	1	SOIC-8	INA501H	1.56	1300	10	Fixed	–40-125	T/R-4000
INA501NASOIC8(1)	1	SOIC-8	INA501N	1.56	1300	20	Fixed	–40-125	T/R-4000
INA501PASOIC8(1)	1	SOIC-8	INA501P	1.56	1300	25	Fixed	–40-125	T/R-4000
INA501RASOIC8(1)	1	SOIC-8	INA501R	1.56	1300	50	Fixed	–40-125	T/R-4000
INA501SASOIC8(1)	1	SOIC-8	INA501S	1.56	1300	75	Fixed	–40-125	T/R-4000
INA501TASOIC8(1)	1	SOIC-8	INA501T	1.56	1300	100	Fixed	–40-125	T/R-4000
INA501KASOIC8(1)	1	SOIC-8	INA501K	1.56	1300	125	Fixed	–40-125	T/R-4000
INA501JASOIC8(1)	1	SOIC-8	INA501J	1.56	1300	200	Fixed	–40-125	T/R-4000
INA501GASOIC8(1)	1	SOIC-8	INA501G	1.56	1300	250	Fixed	–40-125	T/R-4000
INA501FASOIC8(1)	1	SOIC-8	INA501F	1.56	1300	500	Fixed	–40-125	T/R-4000
INA511LASOIC8(1)	1	SOIC-8	INA511L	0.35	130	2	Fixed	–40-125	T/R-4000
INA511MASOIC8(1)	1	SOIC-8	INA511M	0.35	130	5	Fixed	–40-125	T/R-4000
INA511HASOIC8(1)	1	SOIC-8	INA511H	0.35	130	10	Fixed	–40-125	T/R-4000
INA511NASOIC8(1)	1	SOIC-8	INA511N	0.35	130	20	Fixed	–40-125	T/R-4000
INA511PASOIC8(1)	1	SOIC-8	INA511P	0.35	130	25	Fixed	–40-125	T/R-4000
INA511RASOIC8(1)	1	SOIC-8	INA511R	0.35	130	50	Fixed	–40-125	T/R-4000
INA511SASOIC8(1)	1	SOIC-8	INA511S	0.35	130	75	Fixed	–40-125	T/R-4000
INA511TASOIC8(1)	1	SOIC-8	INA511T	0.35	130	100	Fixed	–40-125	T/R-4000
INA511KASOIC8(1)	1	SOIC-8	INA511K	0.35	130	125	Fixed	–40-125	T/R-4000
INA511JASOIC8(1)	1	SOIC-8	INA511J	0.35	130	200	Fixed	–40-125	T/R-4000
INA511GASOIC8(1)	1	SOIC-8	INA511G	0.35	130	250	Fixed	–40-125	T/R-4000
INA511FASOIC8(1)	1	SOIC-8	INA511F	0.35	130	500	Fixed	–40-125	T/R-4000

Note : Available in the future.

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.

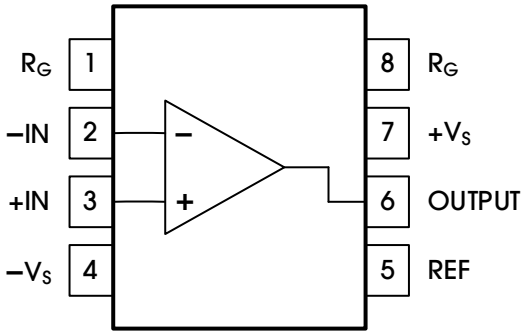


Figure 1. Pin Configuration

Table 3 lists the pin functions.

Table 3. Pin Functions

POSITION	NAME	TYPE	DESCRIPTION
1, 8	R_G	Analog output	Connect a resistor between two R_G to set gain. See more information in the GAIN SELECTION section.
2	–IN	Analog input	Signal negative input
3	+IN	Analog input	Signal positive input
4	$–V_S$	Power supply	Negative power supply
5	REF	Analog input	Output reference voltage input
6	OUTPUT	Analog output	Output
7	$+V_S$	Power supply	Positive power supply

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 4 lists the absolute maximum ratings of the INA101/2.

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Voltage	Supply		±20	V
	Input voltage	$-V_S$ – 0.3	$+V_S$ + 0.3	V
Current	Any pin except power supply	–10	+10	mA
Output Short-Circuit Duration		Indefinite		
Temperature	Operating, T_A, INA101	–40	85	°C
	Operating, T_A, INA102	–55	125	
	Storage, T_{stg}, Q	–65	150	
	Soldering, 10s		300	

Note 1: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: Specification is for device in free air—8-lead plastic package: θ_{JA} = 95°C.

5.2 ESD RATINGS

Table 5 lists the ESD ratings of the INA101/2.

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1), all pins except –IN and +IN	±2000	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1), –IN and +IN pin	±3500	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

Table 6 lists the recommended operating conditions for the INA101/2.

Table 6. Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNITS
Operating Voltage Range	Split supply	±2	±18	±19	V
	Single supply	4	36	38	V
Specified Temperature Range	INA101	–40		85	°C
	INA102	–55		125	°C

5.4 THERMAL INFORMATION

Table 7 lists the thermal information for the INA101/2.

Table 7. Thermal Information

PARAMETER	SYMBOL	SOIC-8	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	90.6	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	47.6	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	3.6	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	47	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	35	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	50.8	°C/W

5.5 ELECTRICAL CHARACTERISTICS

Table 8 lists the electrical characteristics of INA101/2. Typical at 25°C, V_S = ±18V, and R_L = 2kΩ to GND, unless otherwise noted.

Table 8. Electrical Characteristics

PARAMETER	CONDITIONS	INA101			INA102			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
GAIN								
Gain Range	G = 1 + (49.4kΩ / R_G)	1		10K	1		10K	
Gain Error(1)	V_{OUT} = ±10V, G = 1		0.02	0.04		0.02	0.04	%
	V_{OUT} = ±10V, G = 10		0.03	0.08		0.03	0.08	%
	V_{OUT} = ±10V, G = 100		0.03	0.08		0.03	0.08	%
	V_{OUT} = ±10V, G = 1000		0.03	0.15		0.03	0.15	%
Nonlinearity	V_{OUT} = –10V to +10V, G = 1, R_L = 10kΩ		0.8			0.8		ppm
	V_{OUT} = –10V to +10V, G = 10, R_L = 10kΩ		4			4		ppm
	V_{OUT} = –10V to +10V, G = 100, R_L = 10kΩ		30			30		
	V_{OUT} = –10V to +10V, G = 1000, R_L = 10kΩ		60			60		ppm
Gain vs. Temperature	G = 1(5)		0.5	2		0.5	2.5	ppm/°C
	Gain > 1(1)(5)		4	24		5	26	ppm/°C
VOLTAGE OFFSET(2)								
Input Offset, V_{OSI}	V_S = ±18V		±2.5	±12		±2.5	±12	µV
	V_S = ±2V to ±19V, overtemperature(5)			±17			±17	µV
	V_S = ±2V to ±19V, average TC(5)		0.02			0.02		µV/°C
Output Offset, V_{OSO}	V_S = ±18V		±40	±240		±40	±240	µV
	V_S = ±2V to ±19V, overtemperature(5)			±420			±420	µV
	V_S = ±2V to ±19V, average TC(5)		0.03			0.05		µV/°C
Offset Referred to The Input vs. Supply (PSR)	V_S = ±2V to ±20V, G = 1	108	133		108	133		dB
	V_S = ±2V to ±20V, G = 1, overtemperature(5)	105			105			dB
	V_S = ±2V to ±20V, G = 10	126	140		125	140		dB
	V_S = ±2V to ±20V, G = 10, overtemperature(5)	125			125			dB
	V_S = ±2V to ±20V, G = 100	130	144		130	144		dB
	V_S = ±2V to ±20V, G = 100, overtemperature(5)	130			130			dB
	V_S = ±2V to ±20V, G = 1000	130	146		130	146		dB
	V_S = ±2V to ±20V, G = 1000, overtemperature(5)	130			130			dB
INPUT CURRENT								
Input Bias Current			1	3		1	3	nA
	Overtemperature(5)			3.5			10	nA
Input Offset Current			0.6	2.2		0.6	2.2	nA
	Overtemperature(5)			2.4			4.0	nA
INPUT								
Input Impedance	Differential		34 || 5			34 || 5		GΩ_pF
	Common-Mode		34 || 6			34 || 6		GΩ_pF

PARAMETER	CONDITIONS	INA101			INA102			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range[3]	V_S = ±2V to ±19V	$-V_S$ + 0.1		$+V_S$ – 2	$-V_S$ + 0.1		$+V_S$ – 2	V
COMMON-MODE REJECTION								
Common-Mode Rejection Ratio DC	V_{CM} = ($-V_S$ + 0.1V) to ($+V_S$ – 2V), G = 1	97	104		97	104		dB
	V_{CM} = ($-V_S$ + 0.1V) to ($+V_S$ – 2V), G = 1, overtemp[5]	90			90			dB
	V_{CM} = ($-V_S$ + 0.1V) to ($+V_S$ – 2V), G = 10	110	124		110	124		dB
	V_{CM} = ($-V_S$ + 0.1V) to ($+V_S$ – 2V), G = 10, overtemp[5]	107			107			dB
	V_{CM} = ($-V_S$ + 0.1V) to ($+V_S$ – 2V), G = 100	129	141		129	141		dB
	V_{CM} = ($-V_S$ + 0.1V) to ($+V_S$ – 2V), G = 100, overtemp[5]	128			128			dB
	V_{CM} = ($-V_S$ + 0.1V) to ($+V_S$ – 2V), G = 1000	136	157		136	157		dB
	V_{CM} = ($-V_S$ + 0.1V) to ($+V_S$ – 2V), G = 1000, overtemp[5]	136			136			dB
OUTPUT								
Output Swing	R_L = 10kΩ, V_S = ±2V to ±19V, overtemperature[5]	$-V_S$ + 0.2		$+V_S$ – 0.2	$-V_S$ + 0.2		$+V_S$ – 0.3	V
Short Circuit Current	Overtemperature		±17			±17		mA
DYNAMIC RESPONSE								
Small Signal –3dB Bandwidth	G = 1		1300			1300		kHz
	G = 10		230			230		kHz
	G = 100		28			28		kHz
	G = 1000		2.8			2.8		kHz
Slew Rate	G = 1, 10V step		1.6			1.6		V/µs
	G = 100, 10V step		0.5			0.5		V/µs
Settling Time to 0.01%, 10V Step	G = 1		75			75		µs
	G = 100		200			200		µs
NOISE								
Voltage Noise, 1kHz[4]	Input, Voltage Noise, e_{ni}		14			14		$nV/\sqrt{Hz}$
	Output, Voltage Noise, e_{no}		70			70		$nV/\sqrt{Hz}$
RTI, 0.1Hz to 10Hz	G = 1		3			3		μV_{PP}
	G = 100		0.38			0.38		μV_{PP}
Current Noise	f = 1kHz		350			350		$fA/\sqrt{Hz}$
	0.1Hz to 10Hz		10			10		pA_{PP}
REFERENCE INPUT								
R_{IN}			40			40		kΩ
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1.2	23		1.2	27	µV/V
POWER SUPPLY								
Operating Range		±2		±19	±2		±19	V
Quiescent Current	V_S = ±2V to ±19V		1.56	1.9		1.56	1.9	mA
Overtemperature				2			2	mA
TEMPERATURE RANGE								
For Specified Performance		–40		+85	–55		+125	°C

Note 1: Does not include effects of external resistor R_G.
Note 2: Total RTI Error = V_{OSI} + V_{OSO} / G
Note 3: One input grounded. G = 1.
Note 4: Total RTI Noise = $\sqrt{e^2ni + (e_{no} / G)^2}$
Note 5: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by bench test lot.

6. TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = ±18V, R_L = 2kΩ, unless otherwise noted.

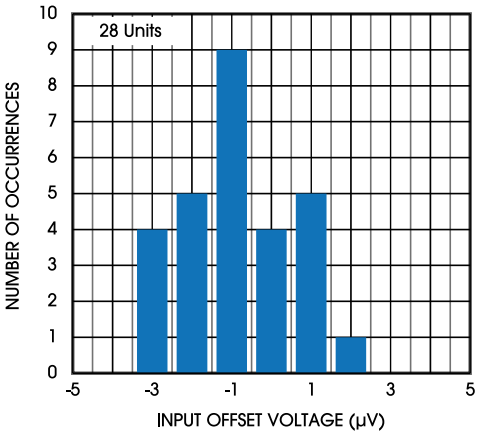


Figure 2. Typical Distribution of Input Offset Voltage

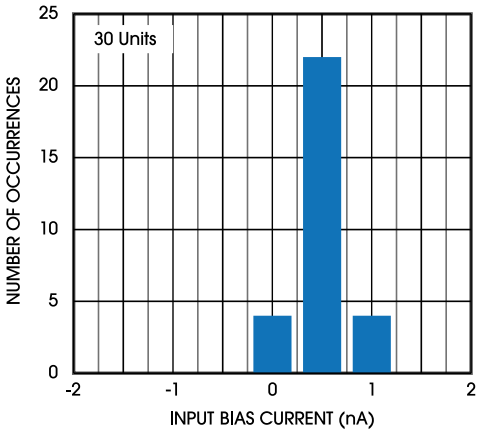


Figure 3. Typical Distribution of Input Bias Current

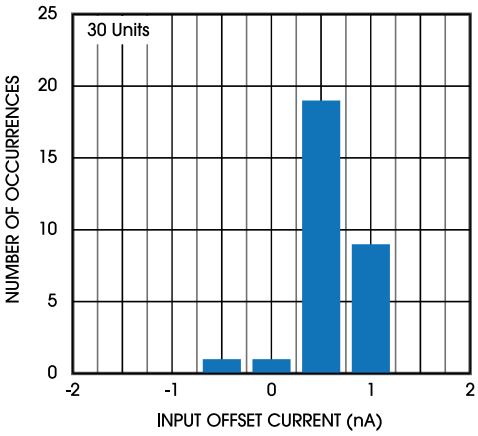


Figure 4. Typical Distribution of Input Offset Current

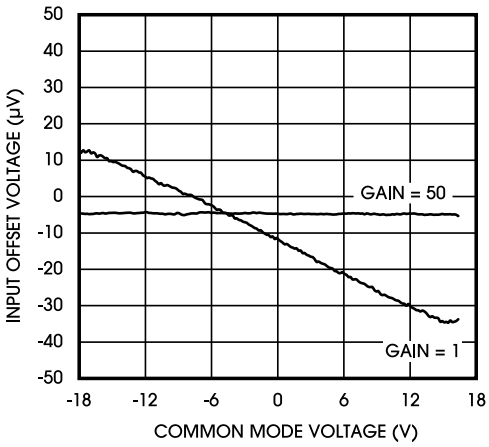


Figure 5. Input Offset Voltage vs. Common Mode Voltage

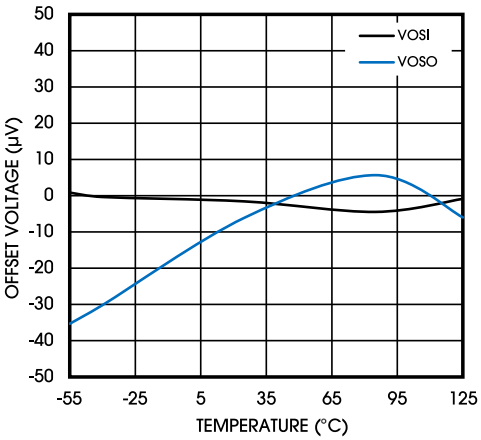


Figure 6. Input Offset Voltage vs. Temperature

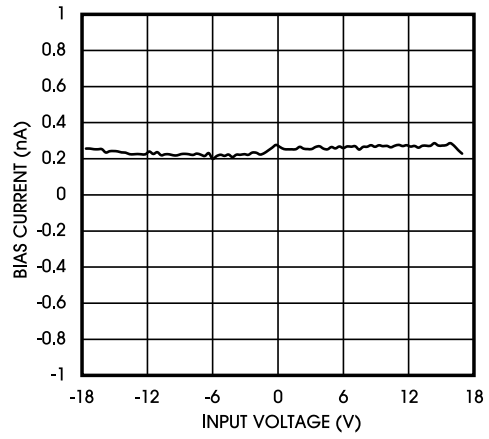


Figure 7. Input Bias Current vs. Common Mode Voltage (25°C)

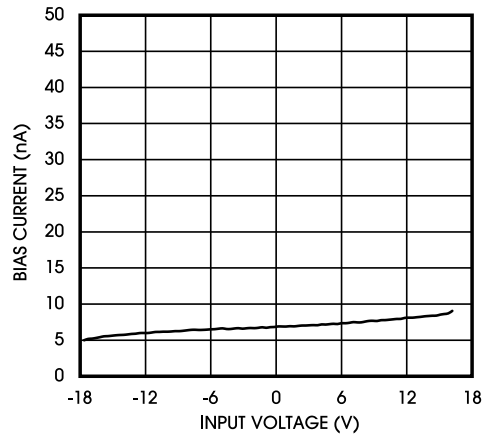


Figure 8. Input Bias Current vs. Common Mode Voltage (125°C)

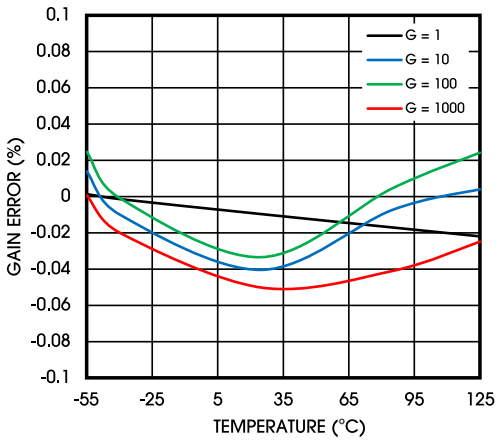


Figure 9. Gain vs. Temperature

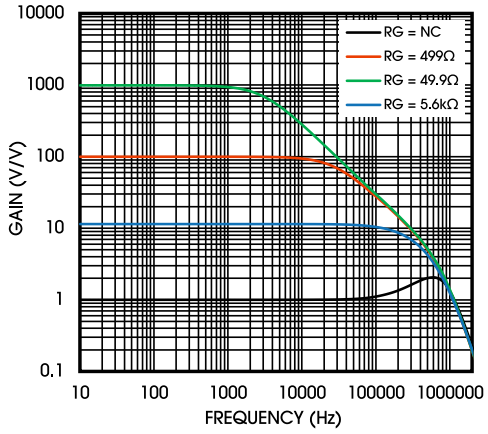


Figure 10. Gain vs. Frequency

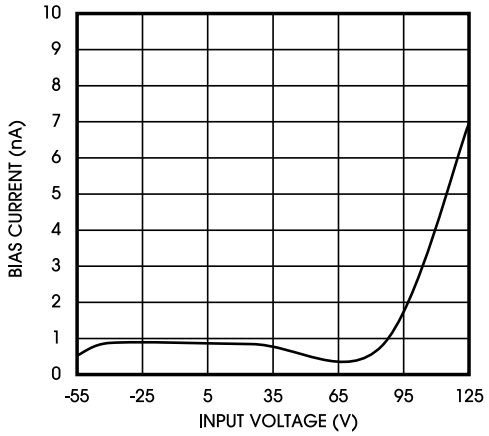


Figure 11. Bias Current vs. Temperature

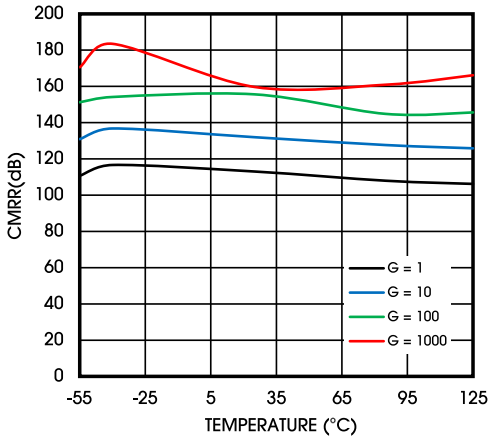


Figure 12. CMRR vs. Temperature

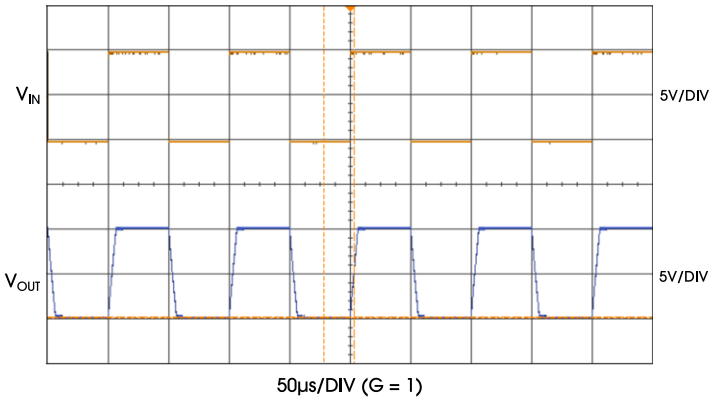


Figure 13. Large Signal Response (G = 1)

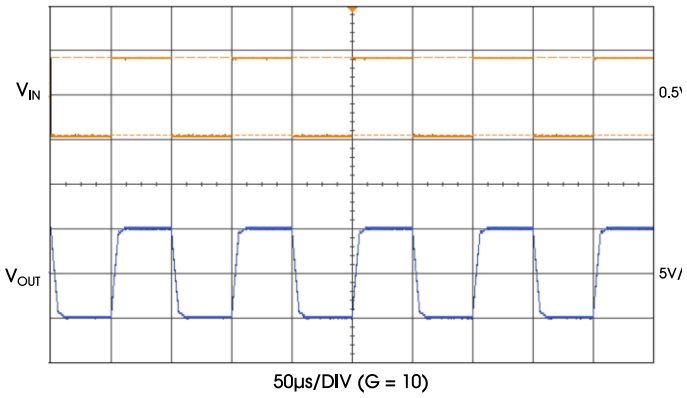


Figure 14. Large Signal Response (G = 10)

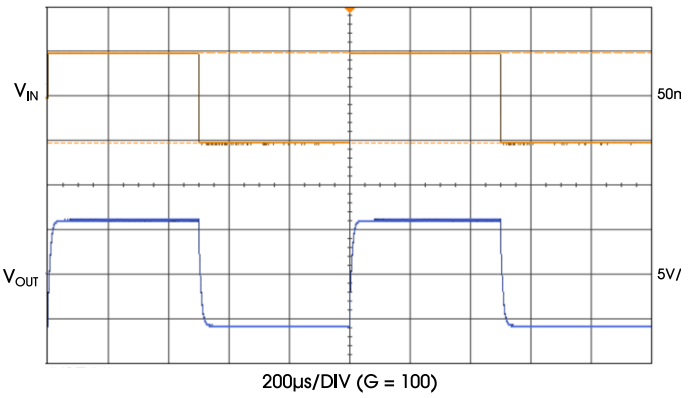


Figure 15. Large Signal Response (G = 100)

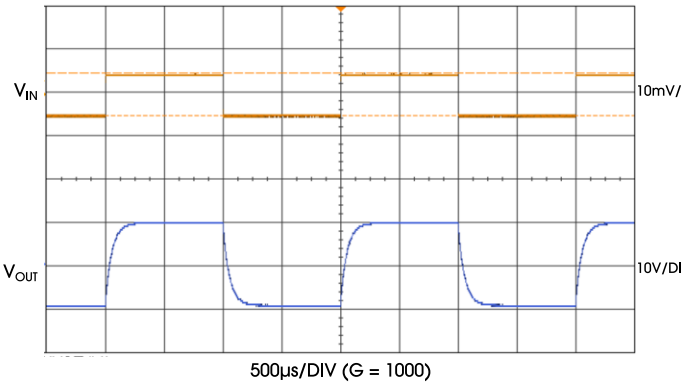


Figure 16. Large Signal Response (G = 1000)

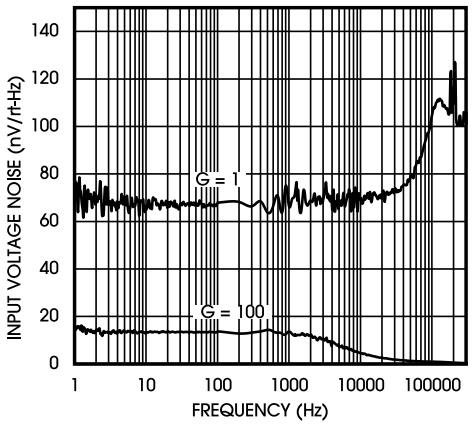


Figure 17. Input Voltage Noise Density

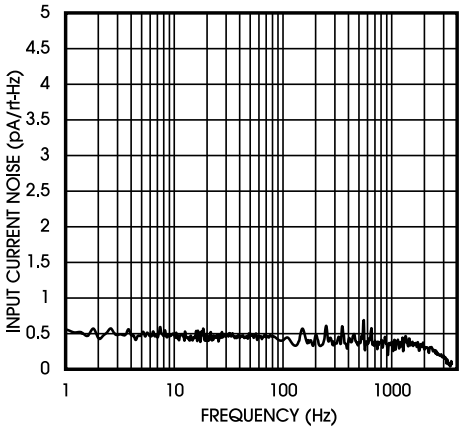


Figure 18. Input Current Noise Density

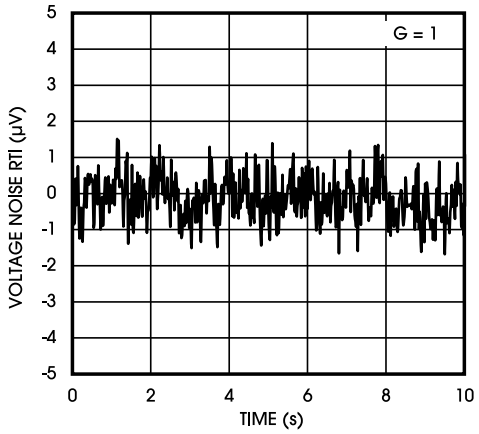


Figure 19. 0.1Hz to 10Hz RTI Voltage Noise

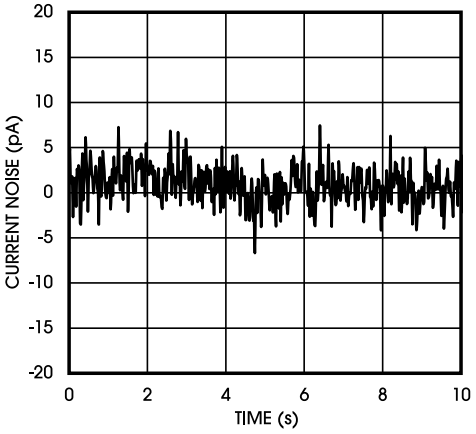


Figure 20. 0.1Hz to 10Hz RTI Current Noise

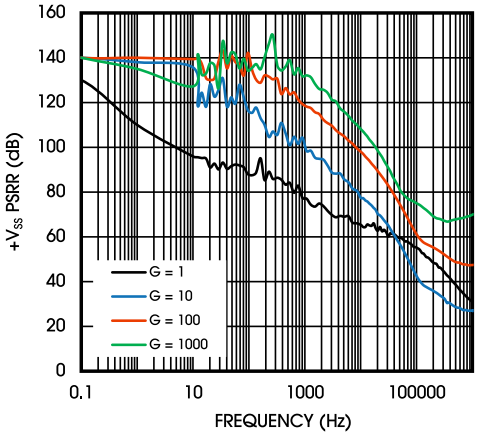


Figure 21. Positive PSR vs. Frequency

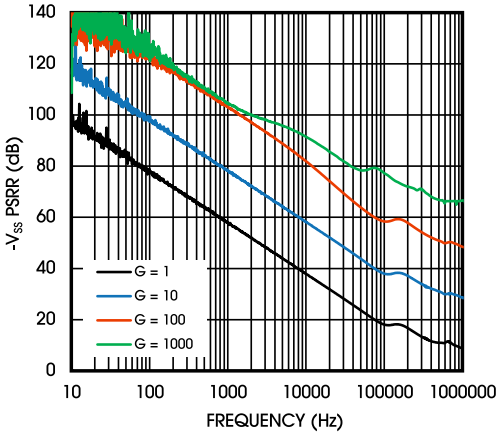


Figure 22. Negative PSR vs. Frequency

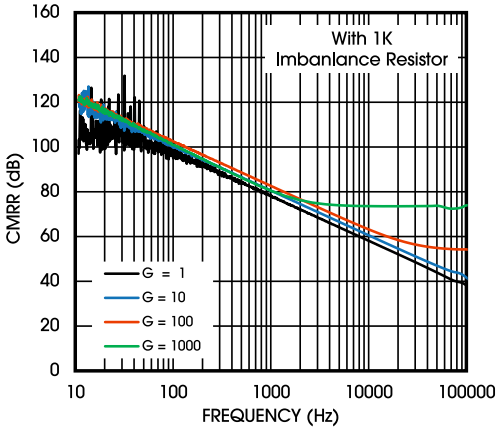


Figure 23. Imbalance CMRR vs. Frequency

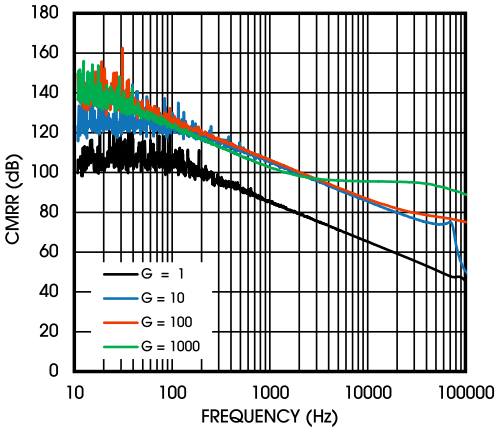


Figure 24. CMRR vs. Frequency

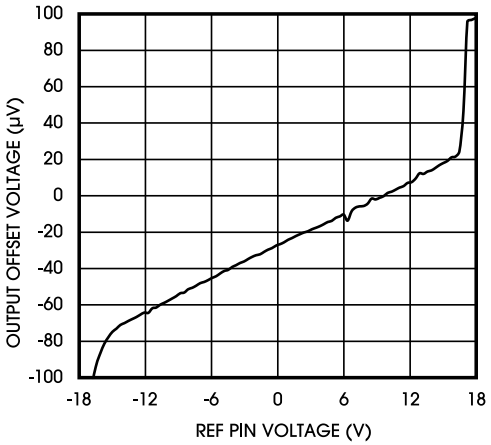


Figure 25. Reference Voltage vs. Output Offset Voltage

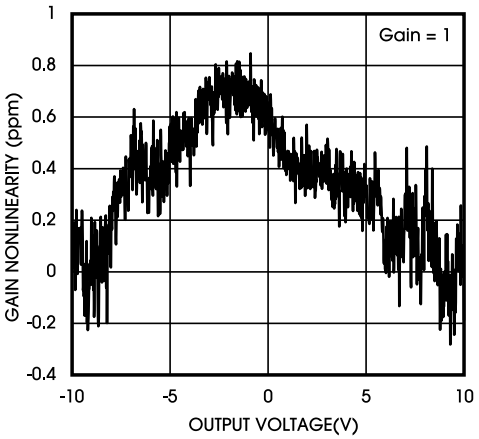


Figure 26. Gain Nonlinearity (G = 1)

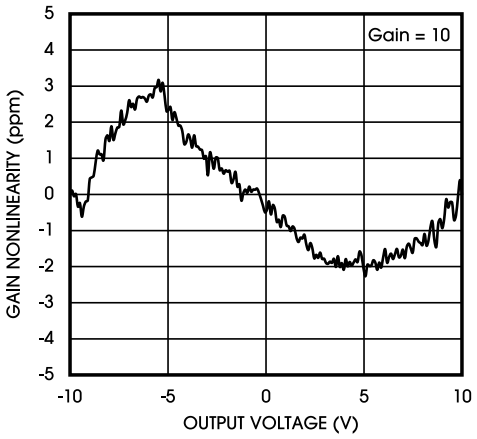


Figure 27. Gain Nonlinearity (G = 10)

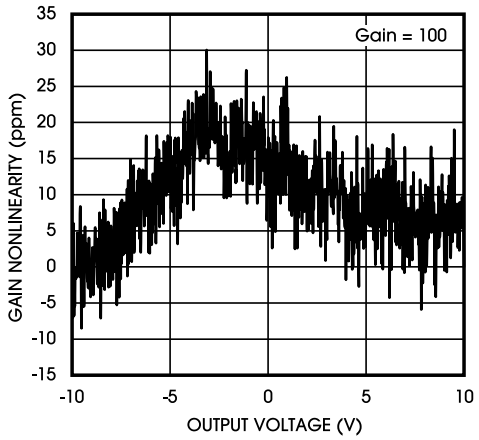


Figure 28. Gain Nonlinearity (G = 100)

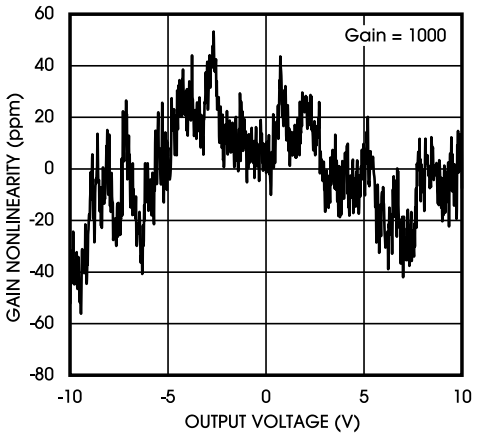


Figure 29. Gain Nonlinearity (G = 1000)

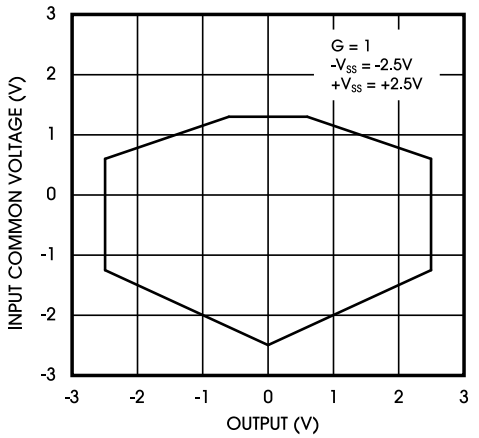


Figure 30. Input Common-Mode Range vs. Output Voltage

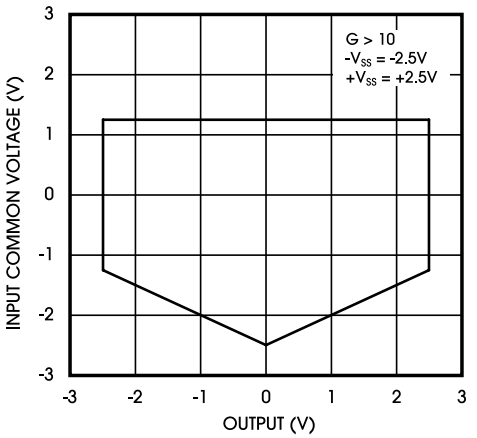


Figure 31. Input Common-Mode Range vs. Output Voltage

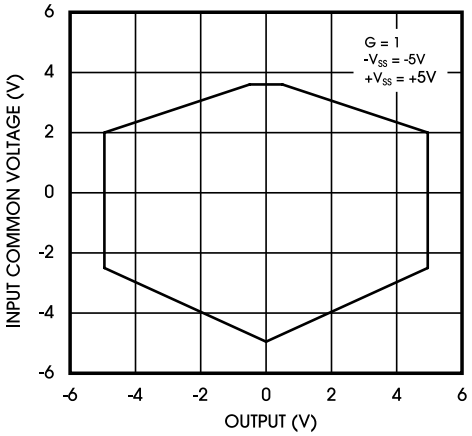


Figure 32. Input Common-Mode Range vs. Output Voltage

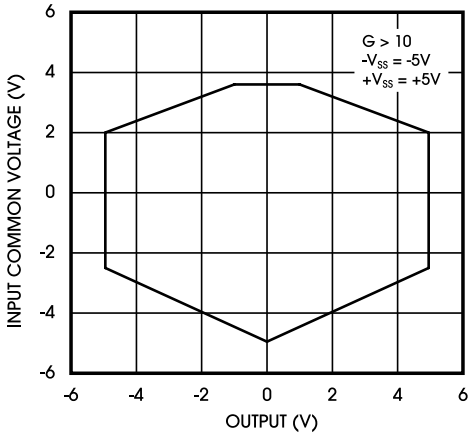


Figure 33. Input Common-Mode Range vs. Output Voltage

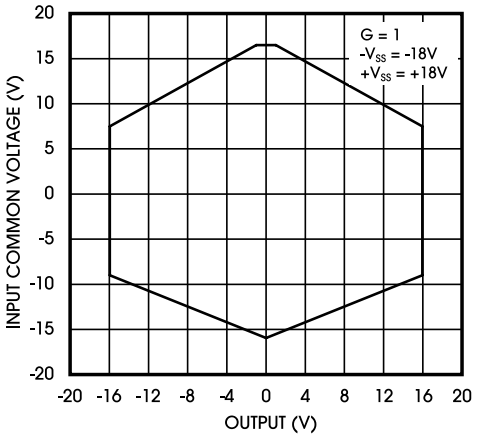


Figure 34. Input Common-Mode Range vs. Output Voltage

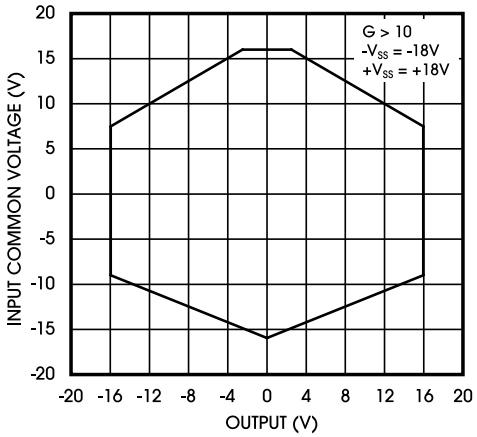


Figure 35. Input Common-Mode Range vs. Output Voltage

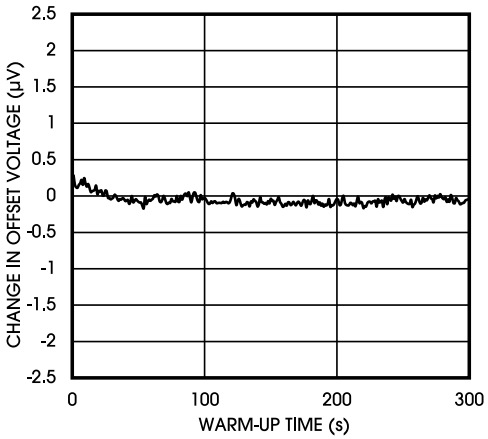


Figure 36. Warm-Up Time

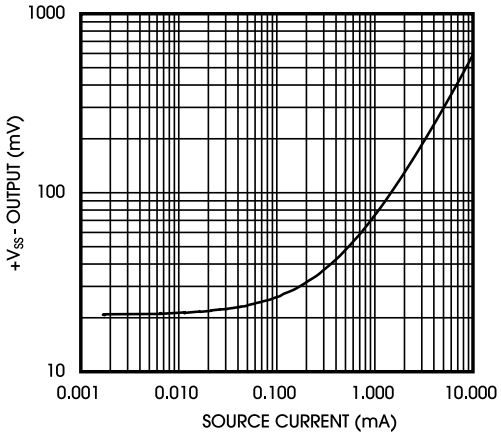


Figure 37. V_{OH} vs. Source Current

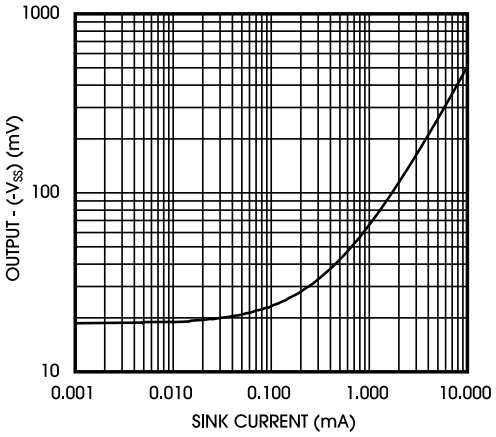


Figure 38. V_{OL} vs. Sink current

7. DETAILED DESCRIPTION

7.1 OVERVIEW

The INA101/2 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain accurately with only one resistor. Monolithic construction and trimming allow the tight matching and tracking of circuit components, thus ensuring the high level of performance inherent in this circuit.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then:

$$G = \frac{49.4k\Omega}{R_G} + 1 \quad (1)$$

$$R_G = \frac{49.4k\Omega}{G - 1} \quad (2)$$

As a single-ended output referred to the REF pin, connect the REF pin to ground or a low resistance source.

7.2 FUNCTIONAL BLOCK DIAGRAM

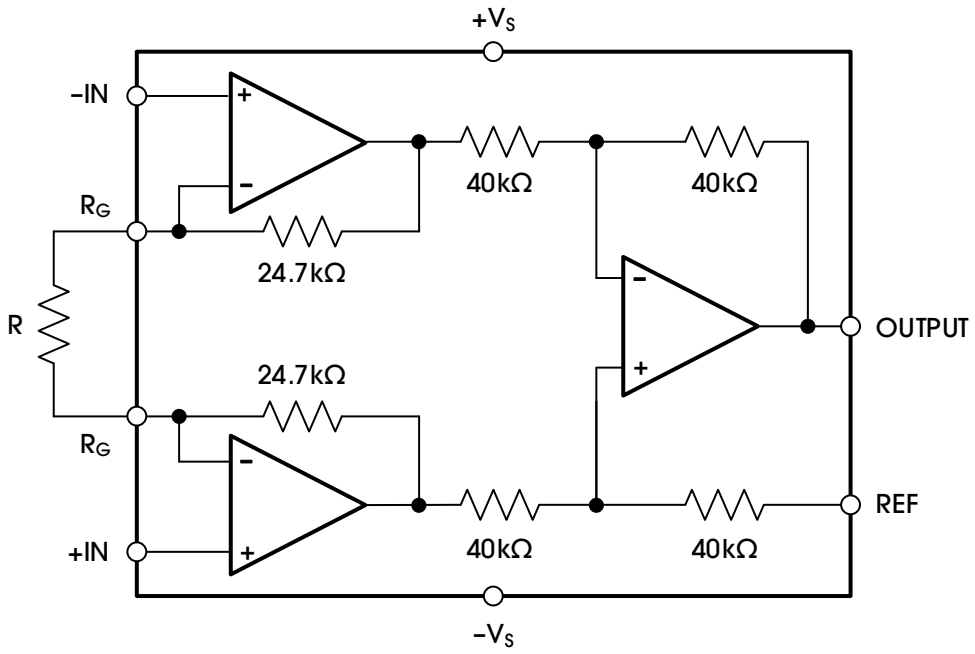


Figure 39. Functional Block Diagram

7.3 FEATURE DESCRIPTION

7.3.1 PRECISION V-I CONVERTER

The INA101/2, along with another op amp and two resistors, makes a precision current source (Figure 40). The op amp buffers the reference terminal to maintain good CMR. The output voltage, V_X, of the INA101/2 appears across R1, which converts it to a current. This current, less only the input bias current of the op amp, then flows out to the load.

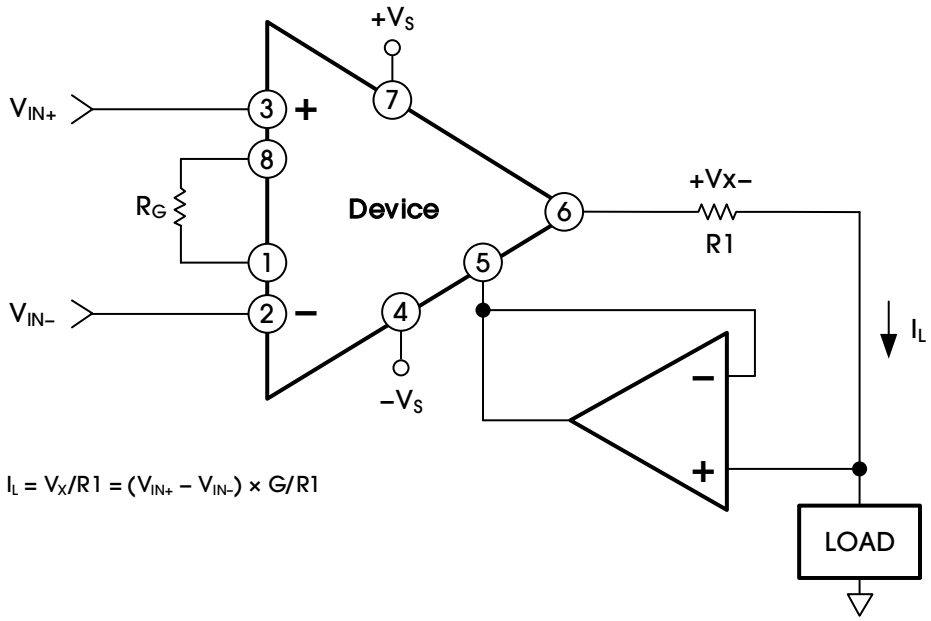


Figure 40. Precision Voltage-to-Current Converter

7.3.2 GAIN SELECTION

The INA101/2 gain is resistor-programmed by R_G, or more precisely, by whatever impedance appears between pins 1 and 8. The INA101/2 is designed to offer accurate gains using 0.1% to 1% resistors. Table 9 shows required values of R_G for various gains. Note that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated by using the formula:

$$R_G = \frac{49.4k\Omega}{G - 1} \tag{3}$$

To minimize gain error, avoid high parasitic resistance in series with R_G; to minimize gain drift, R_G should have a low TC—less than 10ppm/°C for the best performance.

Table 9. Required Values of Gain Resistors

1% STD TABLE VALUE OF R_G (Ω)	CALCULATED GAIN	0.1% STD TABLE VALUE OF R_G (Ω)	CALCULATED GAIN
49.9k	1.990	49.3k	2.002
12.4k	4.984	12.4k	4.984
5.49k	9.998	5.49k	9.998
2.61k	19.93	2.61k	19.93
1.00k	50.40	1.01k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003.0

7.3.3 INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the INA101/2 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains, and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as:

$$\text{Total Error RTI} = \text{Input Error} + (\text{Output Error} / G) \quad (4)$$

$$\text{Total Error RTO} = (\text{Input Error} \times G) + \text{Output Error} \quad (5)$$

7.3.4 REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

7.3.5 INPUT PROTECTION

For input voltages beyond the supplies, a protection resistor should be placed in series with each input to limit the current to 10mA. These can be the same resistors as those used in the RFI filter. High values of resistance can impact the noise and AC CMRR performance of the system. Low leakage diodes (such as the BAV199) can be placed at the inputs to reduce the required protection resistance.

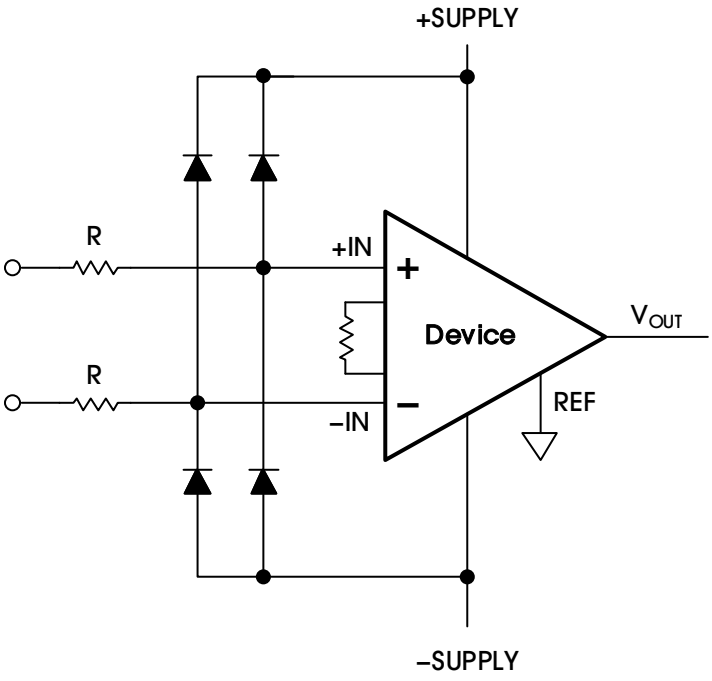


Figure 41. Diode Protection for Voltages Beyond Supply

7.3.6 RF INTERFERENCE

All instrumentation amplifiers rectify small out of band signals. The disturbance may appear as a small dc voltage offset. High frequency signals can be filtered with a low pass R-C network placed at the input of the instrumentation amplifier. Figure 42 demonstrates such a configuration. The filter limits the input signal according to the following relationship:

$$\text{FilterFreq}_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)} \quad (6)$$

$$\text{FilterFreq}_{CM} = \frac{1}{2\pi RC_C} \quad (7)$$

Where:

- $C_D \geq 10C_C$.

C_D affects the difference signal. C_C affects the common-mode signal. Any mismatch in R × C_C degrades the INA101/2 CMRR. To avoid inadvertently reducing CMRR-bandwidth performance, make sure that C_C is at least one magnitude smaller than C_D. The effect of mismatched C_Cs is reduced with a larger C_D:C_C ratio.

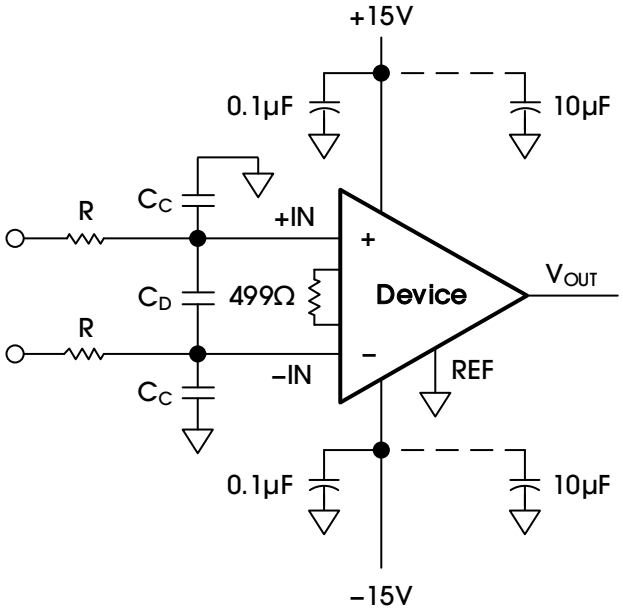


Figure 42. Circuit to Attenuate RF Interference

7.3.7 COMMON-MODE REJECTION

Instrumentation amplifiers, such as the INA101/2, offer high CMR, which is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR, the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications, shielded cables are used to minimize noise; for best CMR over frequency, the shield should be properly driven. Figure 43 and Figure 44 show active data guards that are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

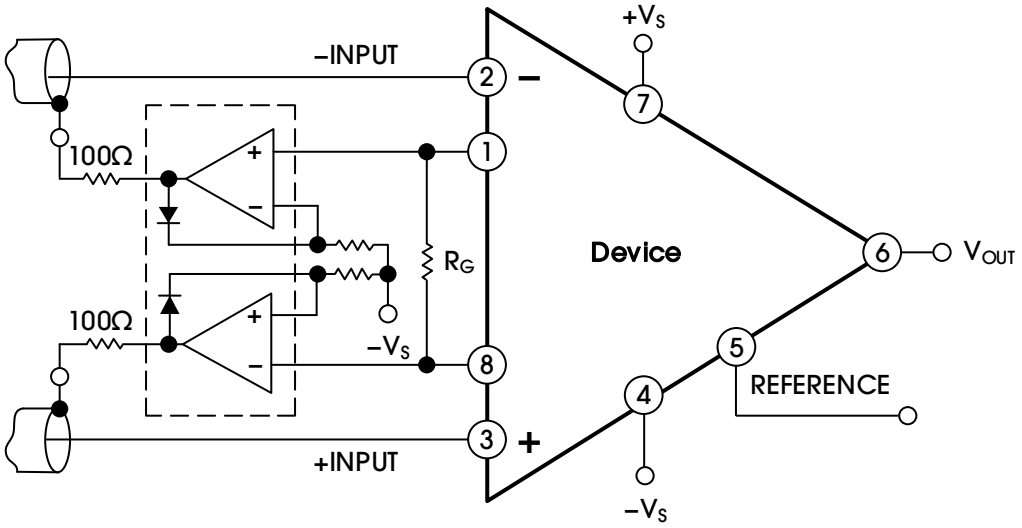


Figure 43. Differential Shield Driver

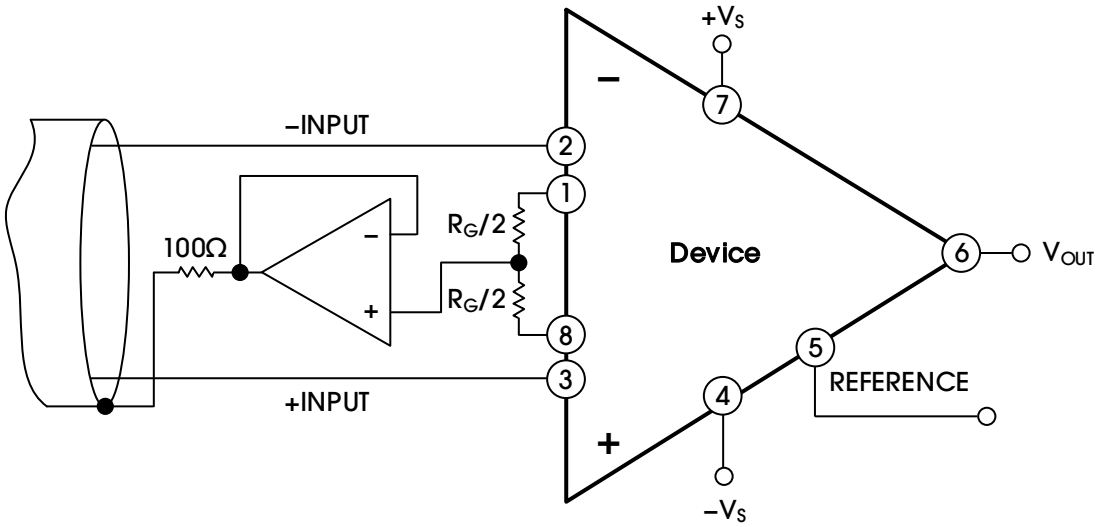


Figure 44. Common-Mode Shield Driver

7.3.8 GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents. Therefore, when amplifying "floating" input sources, such as transformers or ac-coupled sources, there must be a dc path from each input to ground, as shown in Figure 45, Figure 46, and Figure 47.

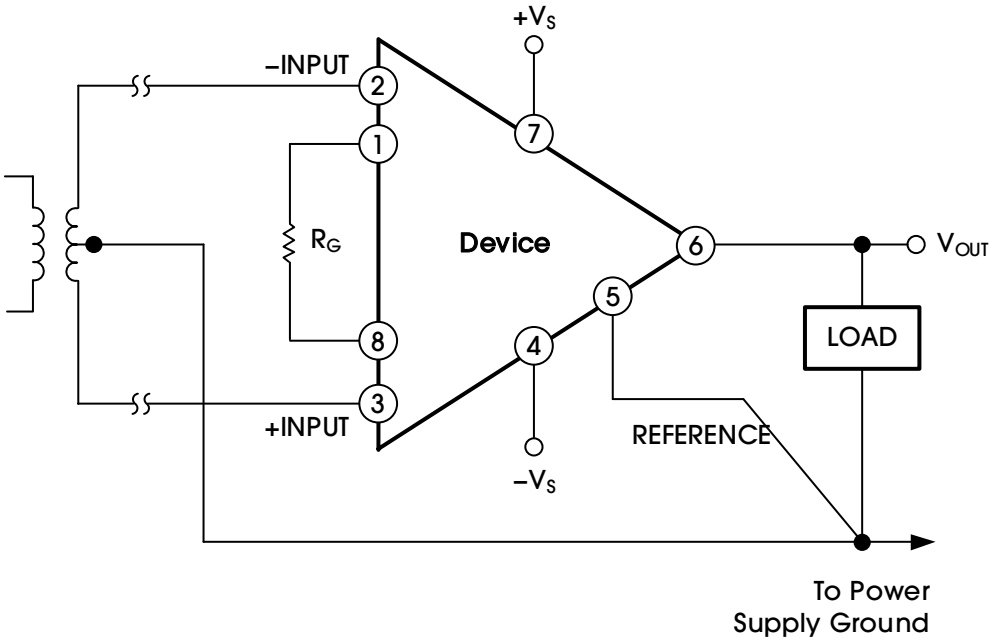


Figure 45. Ground Returns for Bias Currents with Transformer-Coupled Inputs

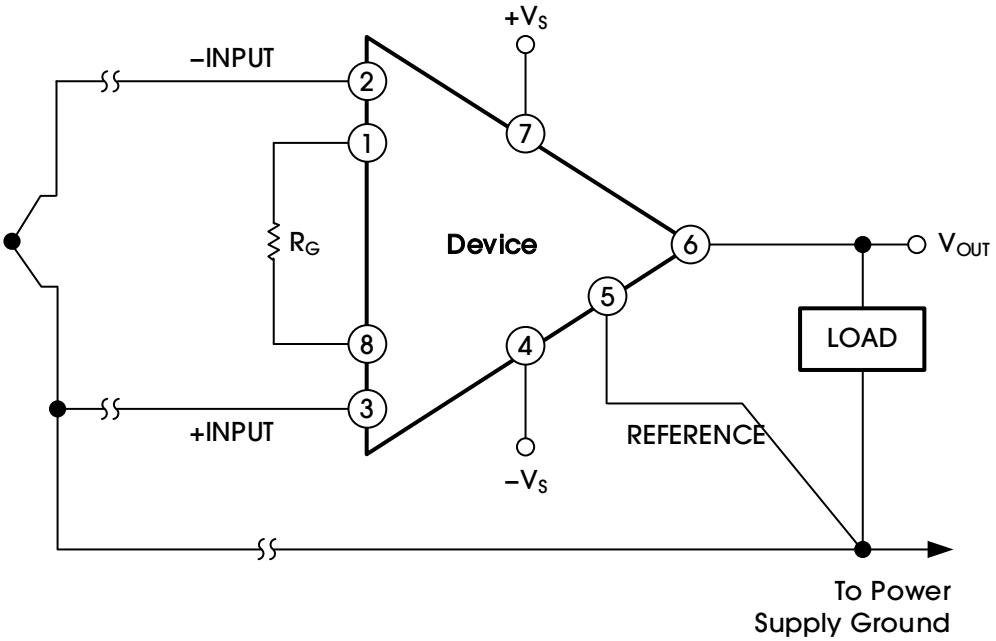


Figure 46. Ground Returns for Bias Currents with Thermocouple Inputs

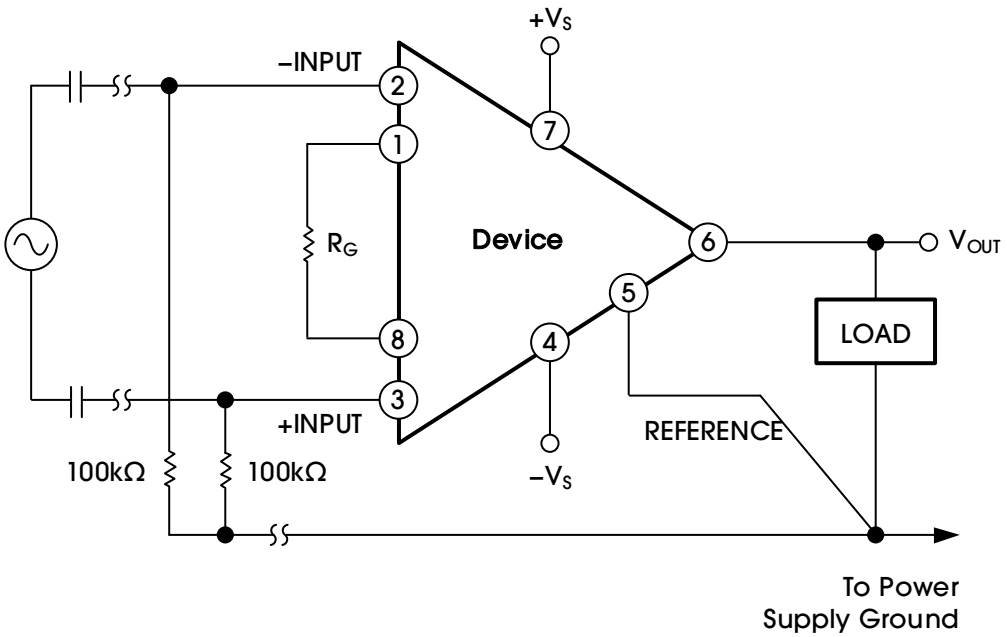


Figure 47. Ground Returns for Bias Currents with AC-Coupled Inputs

8. PACKAGE INFORMATION

The INA101/2 is available in the SOIC-8 package. Figure 48 shows the package view.

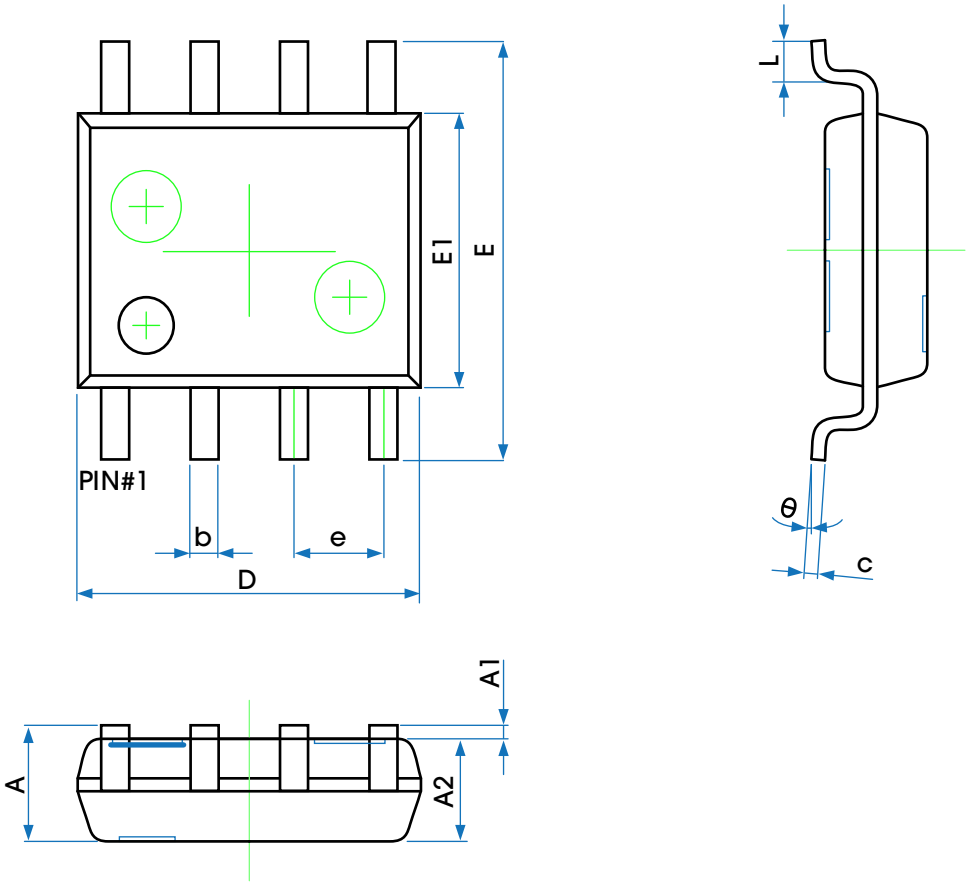


Figure 48. Package View

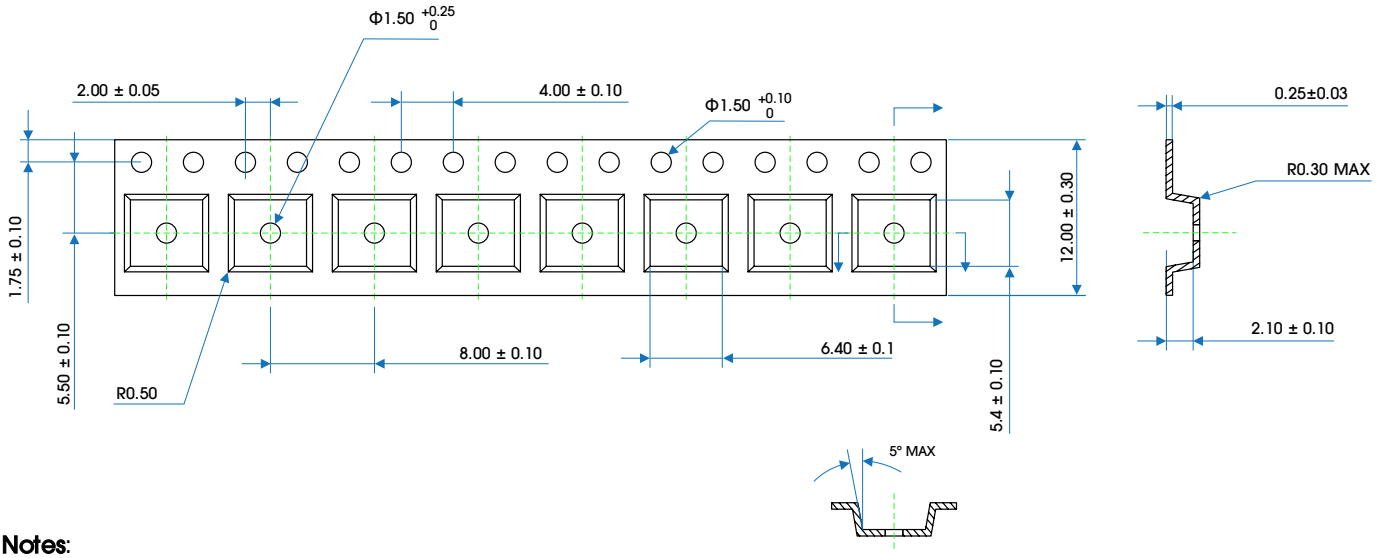
Table 10 provides detailed information about the dimensions.

Table 10. Dimensions

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

9. TAPE AND REEL INFORMATION

Figure 49 illustrates the carrier tape.



Notes:
1. Cover tape width: 9.5 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 1mm in 100mm.
4. Mold#: SOIC-8.
5. All dimensions: mm.
6. Direction of view:

Figure 49. Carrier Tape Drawing

Table 11 provides information about tape and reel.

Table 11. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
SOIC-8	13''	4000	1	8	32000	358*340*50	430*380*390

Figure 50 shows the product loading orientation—pin 1 is assigned at Q1.

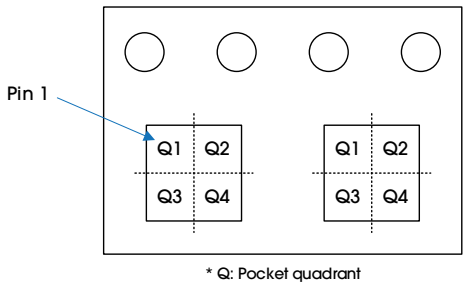


Figure 50. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	12 January 2023	Rev A release.