INA105 Precision Unity Gain Differential Amplifier

1 Features

- Unity-gain difference amplifier configuration
- High common-mode rejection (CMRR): 72dB (minimum)
- Low gain error: 0.025% (maximum)
- Low gain drift: 5ppm/°C (maximum)
- Low nonlinearity: 0.001% (maximum)
- Bandwidth: 1MHz (typical)
- Low offset voltage: 500µV (maximum)
- Low offset voltage drift: 20µV/°C (maximum)

2 Applications

- Battery cell formation & test equipment
- Sensor tag & data logger
- Servo drive position feedback
- Level transmitter
- String inverter

3 Description

The INA105 is a monolithic Gain = 1 differential amplifier consisting of a precision operational amplifier (op amp) and on-chip metal film resistor network. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent tracking of resistors (TCR) maintains gain accuracy and common-mode rejection over temperature. The input common-mode range extends beyond the positive and negative supply rails.

The differential amplifier is the foundation of many commonly used circuits. The INA105 provides precision circuit function without using an expensive precision resistor network. The INA105 is available in 8-pin plastic DIP, SOIC surface-mount and TO-99 metal packages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA105	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.90mm × 6.00mm
	LMC (TO-CAN, 8)	8.96mm × 8.96mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

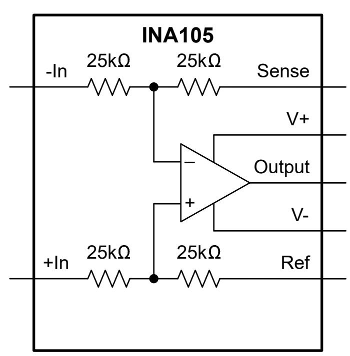

Figure 3-1. Precision Unity Gain Differential Amplifier

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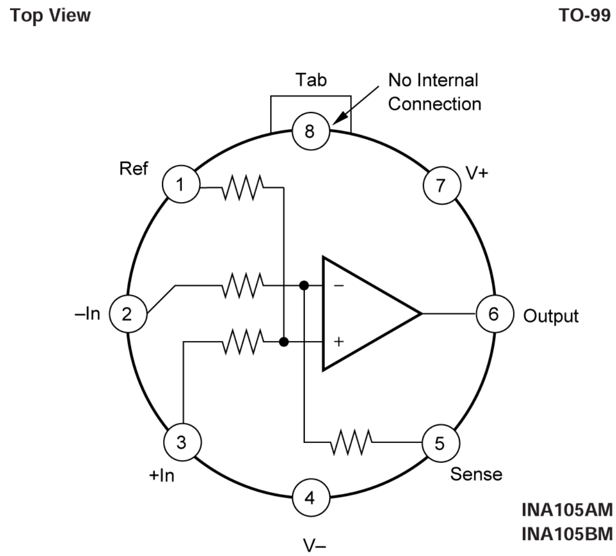
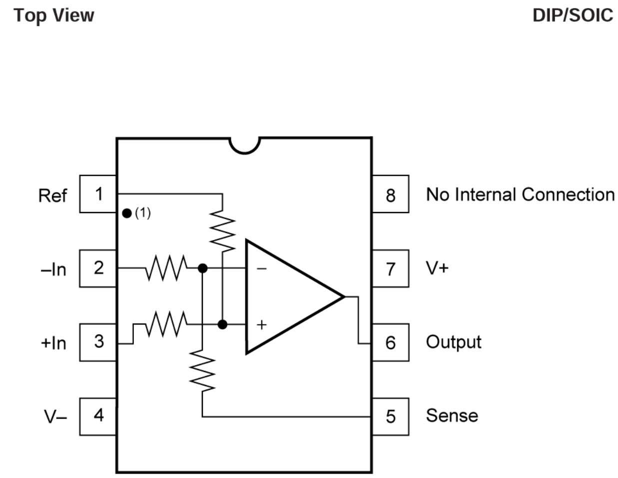
4 Pin Configuration and Functions



Case internally connected to V–. Make no connection.



NOTE: Performance grade identifier box for small outline surface mount. Blank indicates K grade. Part is marked INA105U.

Table 4-1. Pin Functions

NAME	NO.	TYPE	DESCRIPTION
+In	3	Input	Positive (noninverting) input 25kΩ resistor to noninverting terminal of op amp
-In	2	Input	Negative (inverting) input 25kΩ resistor to inverting terminal of op amp
Output	6	Output	Output
Ref	1	Input	Reference input 25kΩ resistor to noninverting terminal of op amp
V+	7	–	Positive (highest) power supply
V-	4	–	Negative (lowest) power supply
Sense	5	Input	Sense input 25kΩ resistor to inverting terminal of op amp
NC	8	–	No internal connection (can be left floating)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	36	V
Signal input pins	Single Supply, +In, –In, Sense, and REF	0	V_S	V
Output short-circuit(2)		Continuous		
Temperature	Operating, T_A (INA105KP, KU)	–40	85	°C
	Operating, T_A (INA105AM, BM)	–55	125	°C
	Junction, T_J		150	
	Storage, T_{stg} (INA105KP, KU)	–40	125	
	Storage, T_{stg} (INA105AM, BM)	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	Single supply	10		36	V
	Dual supply	±5		±18	
Specified temperature		–40		85	°C

5.3 Thermal Information

THERMAL METRIC(1)		INA105		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.9	74.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.9	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	38.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.8	18.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55.7	37.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage	RTO(1) (2)	INA105AM		50	250	µV
			INA105BM		50	250	µV
			INA105KP, KU		50	500	µV
	Offset voltage drift	T_A = –40°C to +85°C, RTO(1) (2)	INA105AM		5	20	µV/°C
			INA105BM		5	10	µV/°C
			INA105KP, KU		5	20	µV/°C
PSRR	Power-supply rejection ratio	RTO(1) (2), V_S = ±6V to ±18V	INA105AM		1	25	µV/V
			INA105BM		1	15	µV/V
			INA105KP, KU		1	25	µV/V
	Long-term stability	RTO(1) (2)			20		µV/mo
ZIN-DM	Differential impedance (3)				50		kΩ
ZIN-CM	Common-mode impedance(3)				50		kΩ
V_{CM}	Operating common-mode input voltage(4)			–20		20	V
V_{DM}	Operating differential-mode input voltage(4)			–10		10	V
CMRR	Common-mode rejection ratio(5)	T_A = –40°C to +125°C	INA105AM	80	90		dB
			INA105BM	86	100		dB
			INA105KP, KU	72	90		dB
NOISE VOLTAGE							
e_N	Voltage noise	RTO(1) (6)	f_O = 10kHz		60		nV/√Hz
			f_B = 0.01Hz to 10Hz		2.4		$µV_{PP}$
GAIN							
GE	Gain error	INA105AM			±0.005	±0.01	%
		INA105BM			±0.005	±0.01	%
		INA105KP, KU			±0.01	±0.025	%
	Gain drift				1	5	ppm/°C
	Gain nonlinearity				±0.0002	±0.001	% of FSR
OUTPUT							
	Output voltage	I_O = –5mA, 20mA		10	12		V
	Load capacitance stability				1000		pF
I_{SC}	Sourcing	Continuous to V_S / 2			40 to 70		mA
	Sinking				10 to 70		mA
Z_O	Output Impedance				0.01		Ω

5.4 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
BW	Bandwidth, –3dB			1		MHz
FPBW	Full Power Bandwidth, –3dB	V_O = 20Vpp	30	50		kHz
SR	Slew rate		2	3		V/μs
t_S	Settling time	0.1%, V_{STEP} = 10V		4		μs
		0.01%, V_{STEP} = 10V		5		μs
		0.01%, $V_{CM\text{-}STEP}$ = 10V, V_{DIFF} = 0V		1.5		μs
POWER SUPPLY						
I_Q	Quiescent current	V_O = 0V		±1.5	±2	mA

(1) Referred to output in unity-gain difference configuration.
(2) Includes effects of input bias and offset currents of the amplifier.
(3) 25kΩ resistors are ratio matched but have ±20% absolute value.
(4) Maximum input voltage without protection is 10V more than either ±15V supply (±25V). Limit I_{IN} to 1mA.
(5) With zero source impedance.
(6) Includes effects of the input current noise of the amplifier and thermal noise contribution of resistor network.

5.5 Typical Characteristics

at T_A = 25°C, V_S = ±15V (unless otherwise noted)

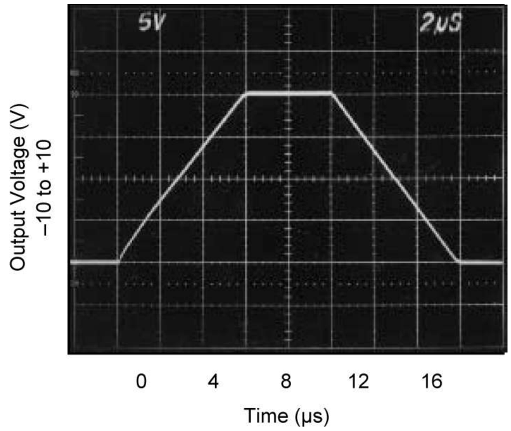


Figure 5-1. Step Response

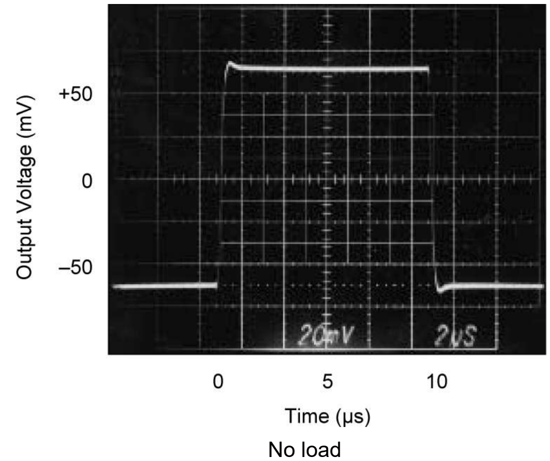


Figure 5-2. Small Signal Response (No Load)

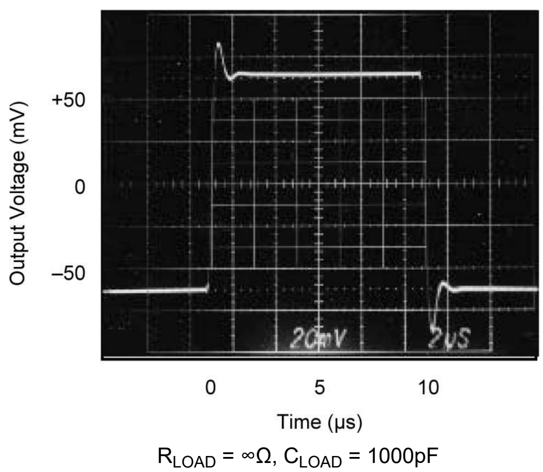


Figure 5-3. Small Signal Response

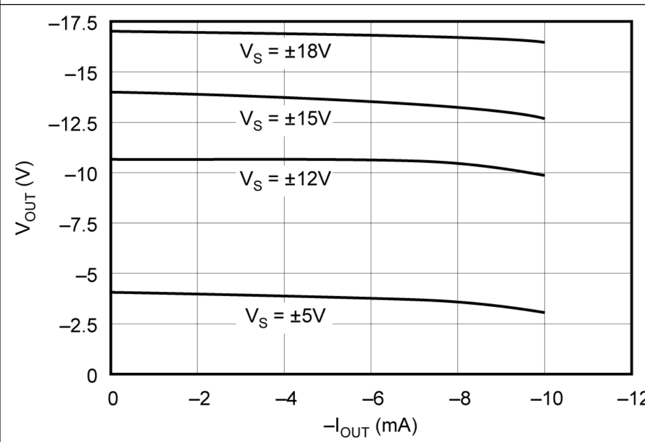


Figure 5-4. Maximum V_{OUT} vs I_{OUT} (Negative Swing)

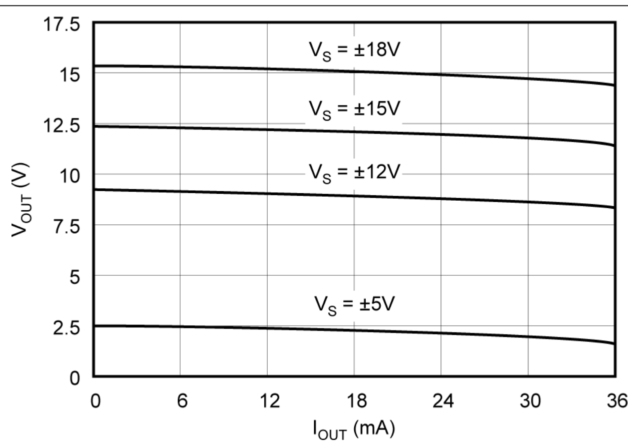


Figure 5-5. Maximum V_{OUT} vs I_{OUT} (Positive Swing)

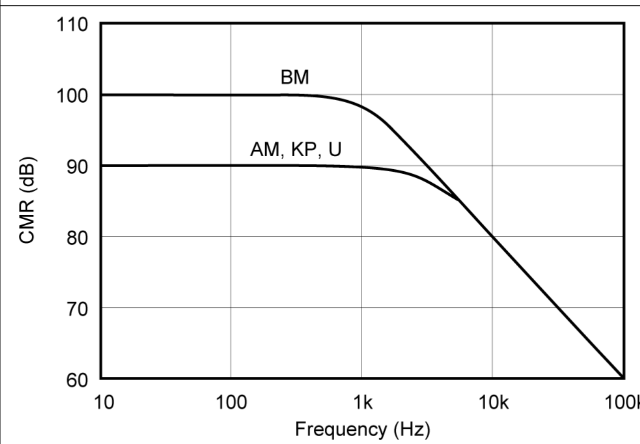


Figure 5-6. CMR vs Frequency

5.5 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V (unless otherwise noted)

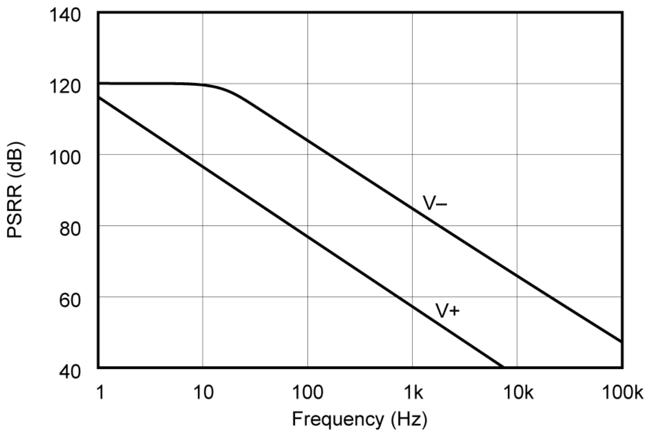
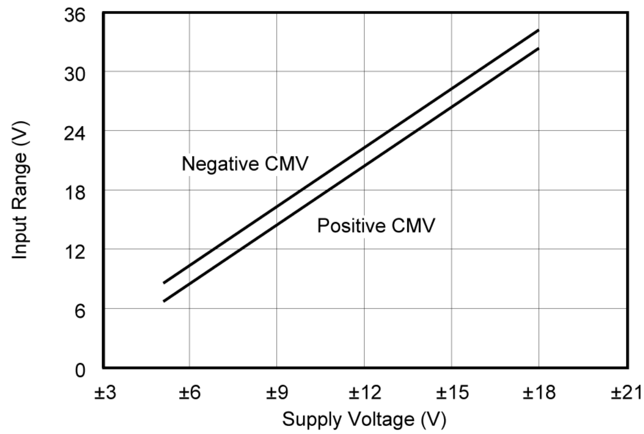


Figure 5-7. Power Supply Rejection vs Frequency



Difference amplifier connected, V_{OUT} = 0

Figure 5-8. Common-Mode Input Range vs Supply

6 Detailed Description

6.1 Overview

The INA105 consists of a high-precision operational amplifier and four trimmed, on-chip resistors. The device can be configured to make a wide variety of amplifier configurations, including difference, non-inverting, and inverting configurations. The integrated, matched resistors provide an advantage over discrete implementation.

Much of the DC performance of op amp circuits depends on the accuracy of the surrounding resistors. The resistors on the INA105 are laid out to be tightly matched. The resistors of each part are matched on-chop and tested for matching accuracy. As a result, the INA105 provides high accuracy for specifications such as gain drift, common-mode rejection ratio, and gain error.

6.2 Functional Block Diagram

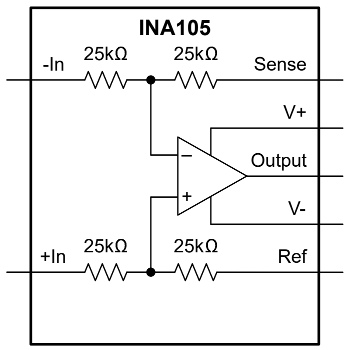


Figure 6-1. INA105 Internal Schematic

6.3 Feature Description

6.3.1 Gain Error and Drift

Gain error in the INA105 is limited by the mismatch of the integrated precision resistors. Gain drift is limited by the slight mismatch of the temperature coefficient of integrated resistors. The integrated resistors are precision-matched with low temperature coefficient resistors to improve overall gain drift compared to the discrete implementation of differences amplifiers build when using external resistors.

6.3.2 Input Voltage Range

The INA105 difference amplifier is able to achieve a wide input common-mode voltage range by dividing down the input signal with high-precision resistor divider. The internal resistors divide down the voltage before the voltage reaches the internal op amp and provide protection to the op amp inputs. Figure 6-2 shows an example of how the voltage division works in a difference-amplifier configuration. For the INA105 with a supply voltage of ±15V, the input common-mode voltage range is ±20V.

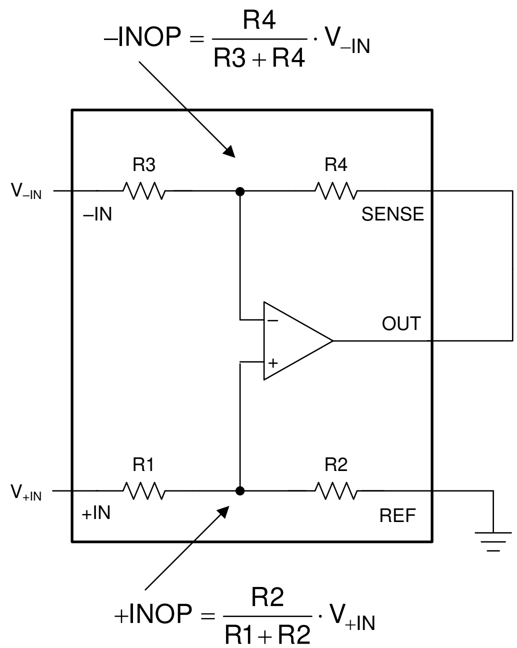


Figure 6-2. Voltage Division in the Difference Amplifier Configuration

6.4 Device Functional Modes

The INA105 has one functional mode. The device is specified on a power supply of ±15V and can operate on a power supply from ±5V to ±18V with derated performance. See *Typical Characteristics*.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Figure 7-1 shows the basic connections required for operation of the INA105. Connect power-supply bypass capacitors close to the device pins.

The differential input signal is connected to pins 2 and 3, as shown. The source impedances connected to the inputs must be nearly equal for good common-mode rejection. A 5Ω mismatch in source impedance can degrade the common-mode rejection of a typical device to approximately 80dB. If the source has a known mismatch in source impedance, an additional resistor in series with one input can be used to preserve good common-mode rejection.

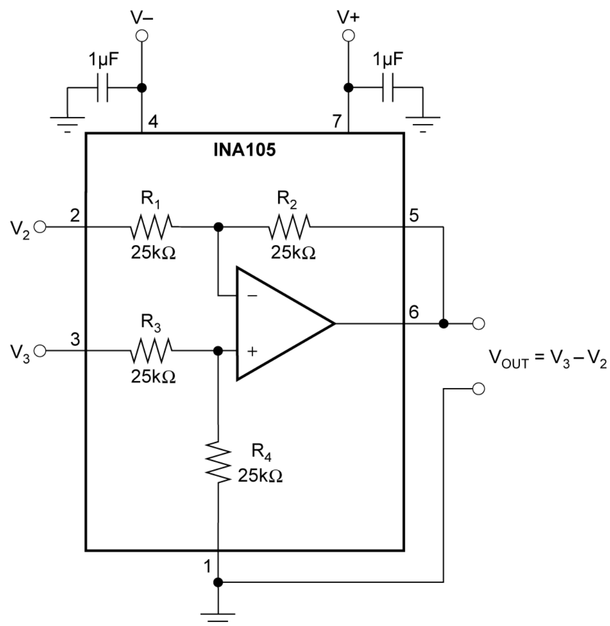


Figure 7-1. Basic Power-Supply and Signal Connections

The output is referred to the output reference terminal (pin 1) which is normally grounded. A voltage applied to the Ref terminal is summed with the output signal. This can be used to null offset voltage as shown in Figure 7-2. To maintain good common-mode rejection, keep the source impedance of a signal applied to the Ref terminal less than 10Ω.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR.

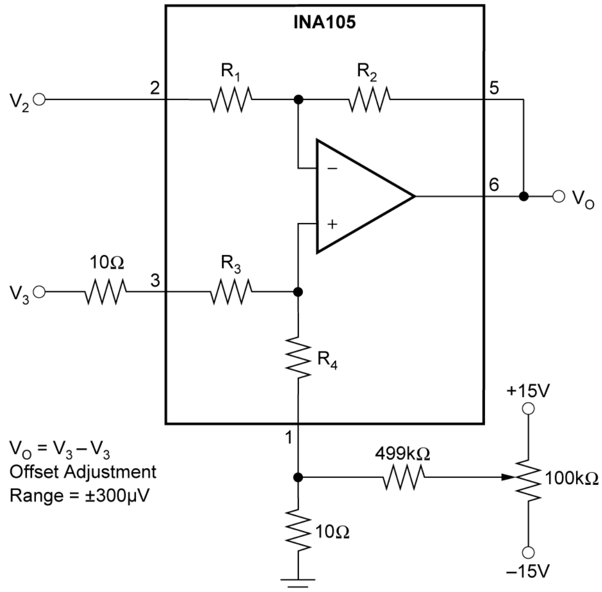


Figure 7-2. Offset Adjustment

7.2 Typical Application

The INA105 can be used in a variety of applications. Figure 7-3 shows one example.

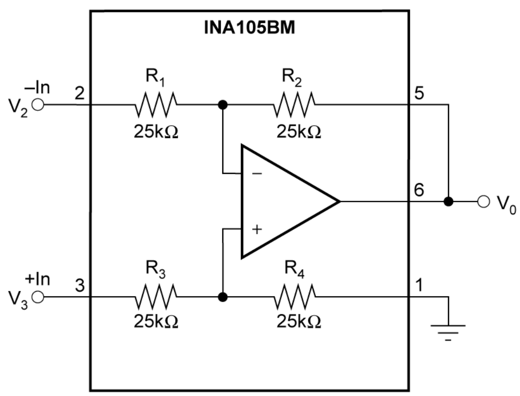


Figure 7-3. Precision Difference Amplifier

7.3 Additional Applications

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. The following section shows additional application circuit ideas.

7.3.1 Operational Amplifier Circuits

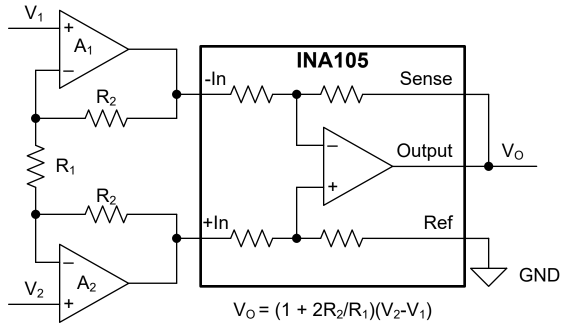


Figure 7-4. Precision Instrumentation Amplifier

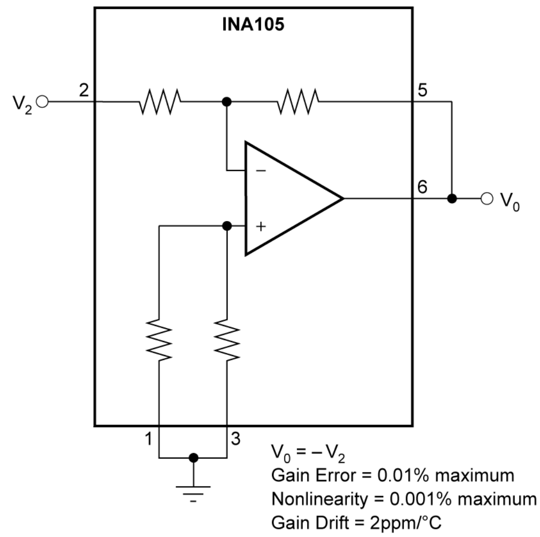


Figure 7-5. Precision Unity-Gain Inverting Amplifier

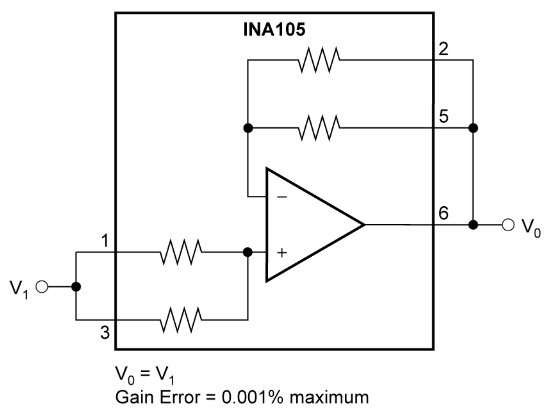


Figure 7-6. Precision Unity-Gain Buffer

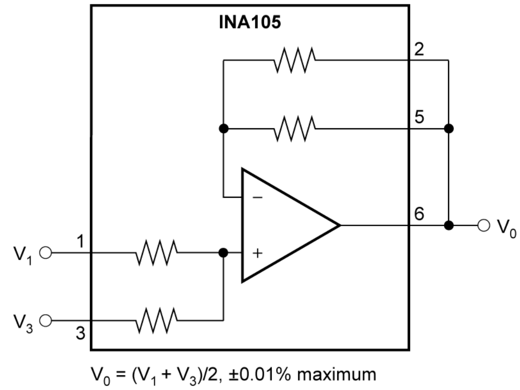


Figure 7-7. Precision Average-Value Amplifier

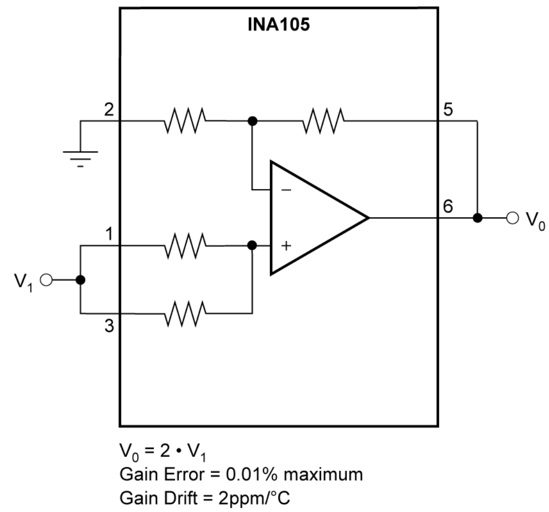


Figure 7-8. Precision Gain = 2 Amplifier

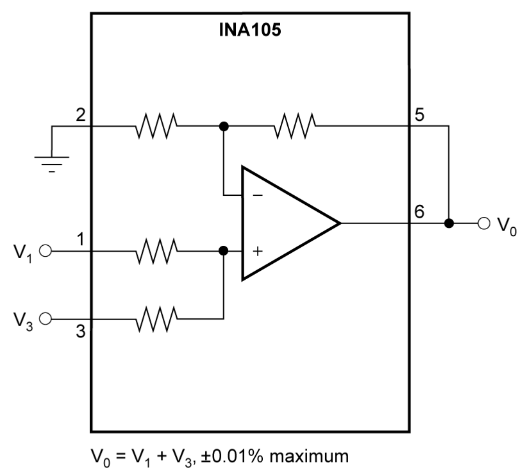


Figure 7-9. Precision Summing Amplifier

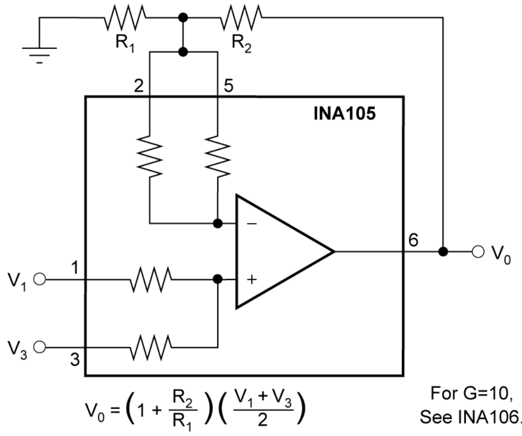


Figure 7-10. Precision Summing Amplifier With Gain

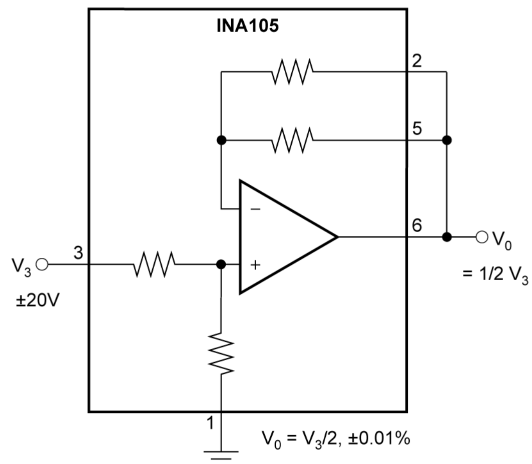
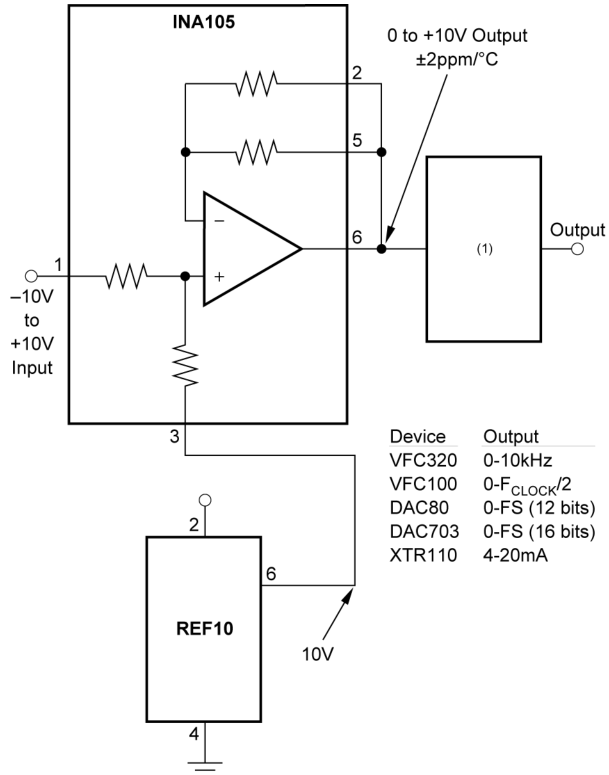


Figure 7-11. Precision Gain = 1/2 Amplifier



Unipolar input device.

Figure 7-12. Precision Bipolar Offsetting

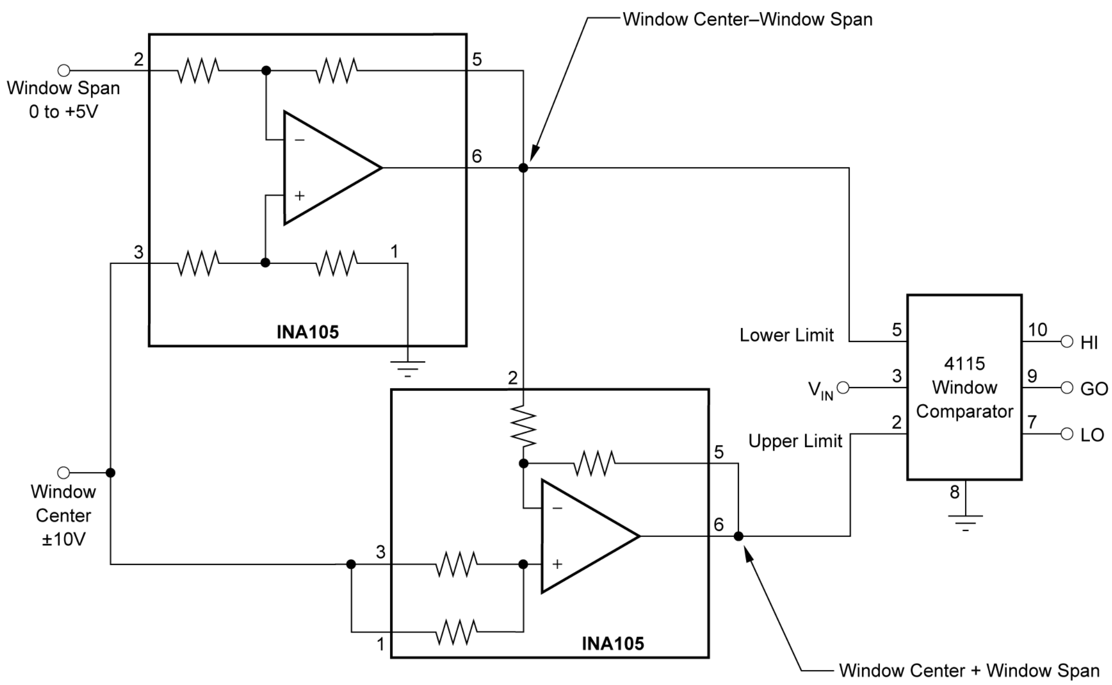
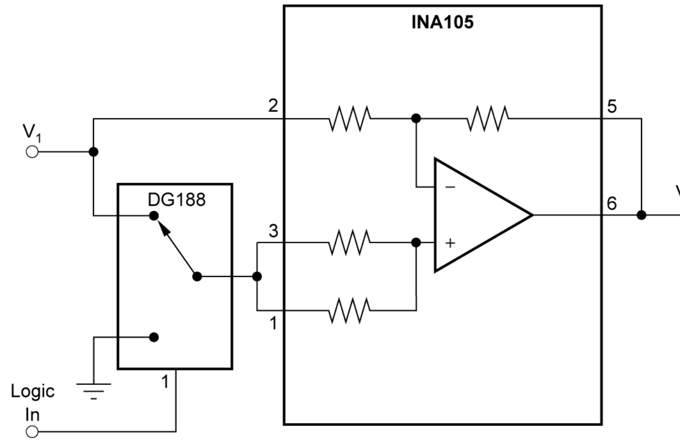


Figure 7-13. Window Comparator With Window-Span and Window-Center Inputs



Logic In	V_O
0	$-V_1$
1	$+V_1$

Figure 7-14. Digitally Controlled Gain of ±1 Amplifier

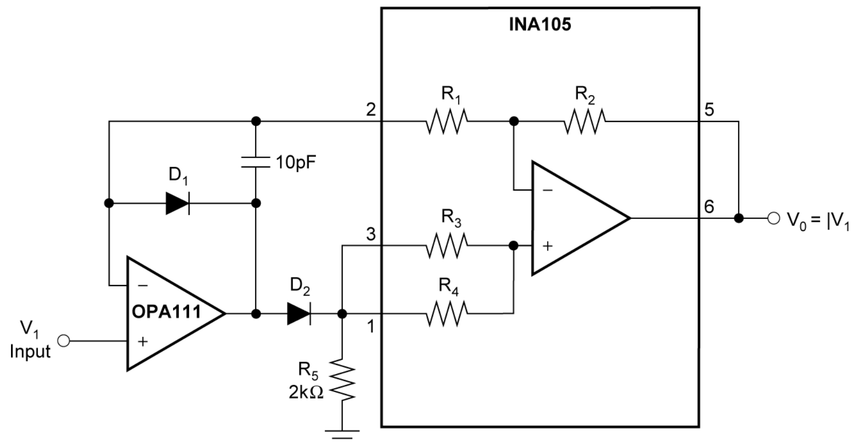


Figure 7-15. Precision Absolute-Value Buffer

7.3.2 Instrumentation Amplifier Circuits

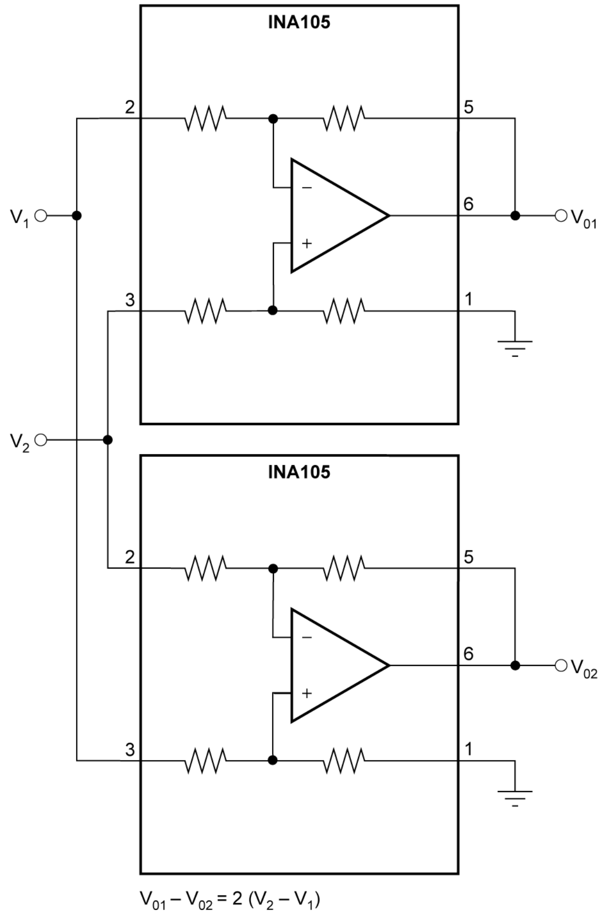


Figure 7-16. Differential Output Difference Amplifier

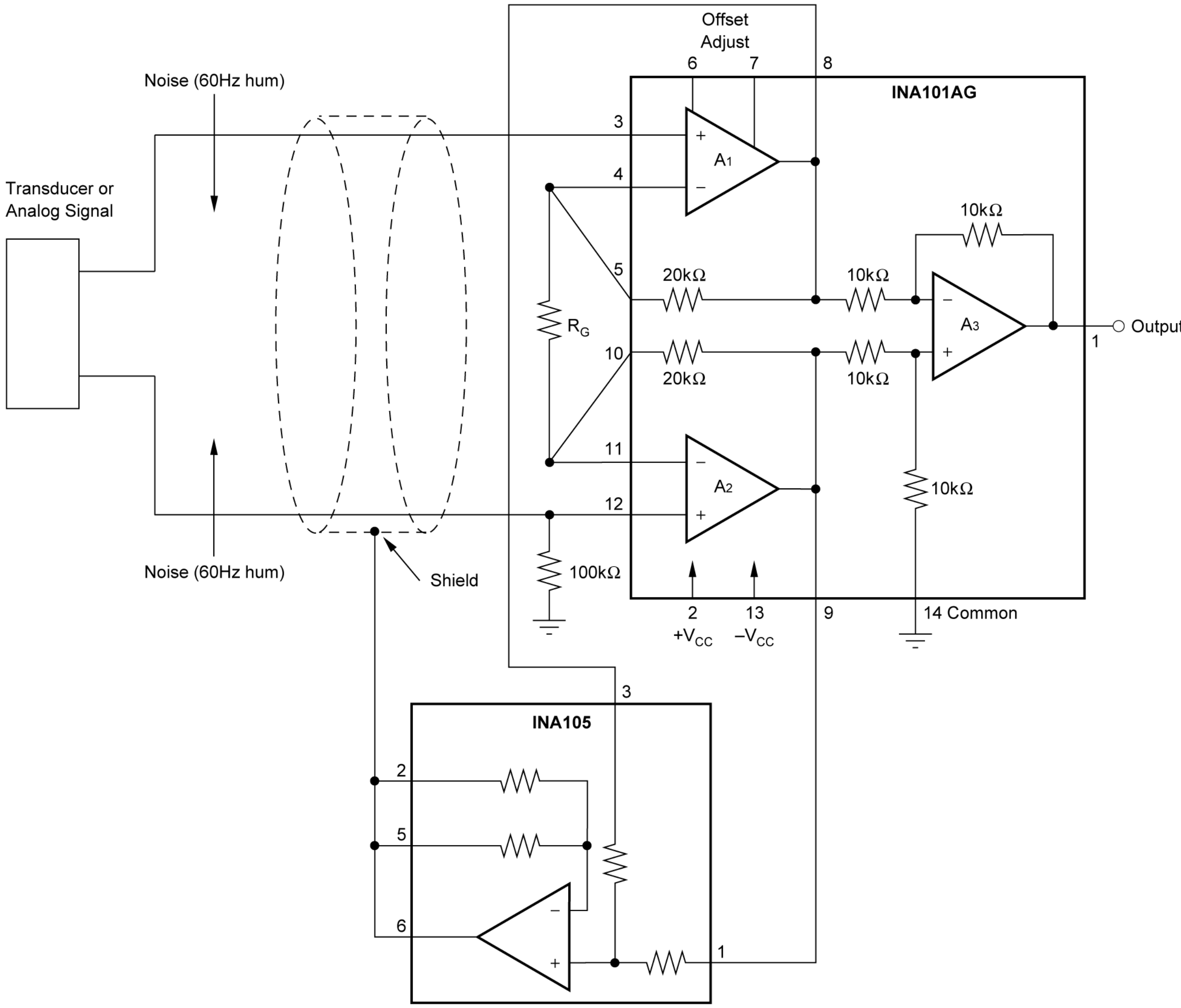


Figure 7-17. Instrumentation Amplifier Guard Drive Generator

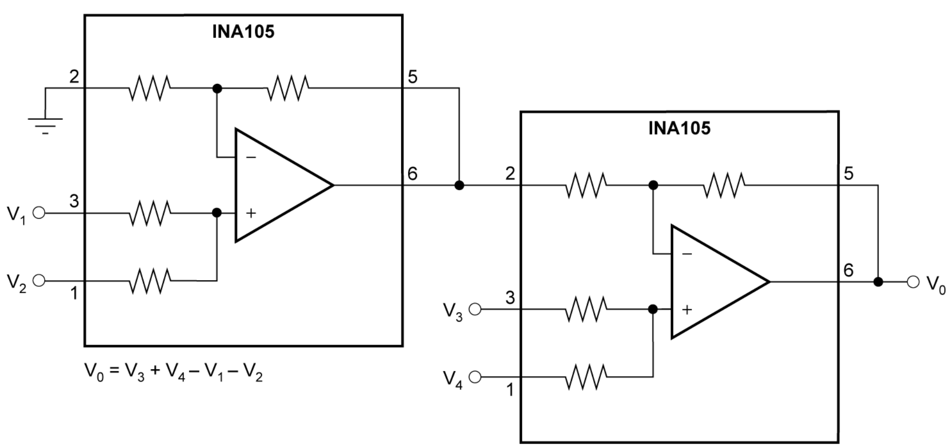


Figure 7-18. Precision Summing Instrumentation Amplifier

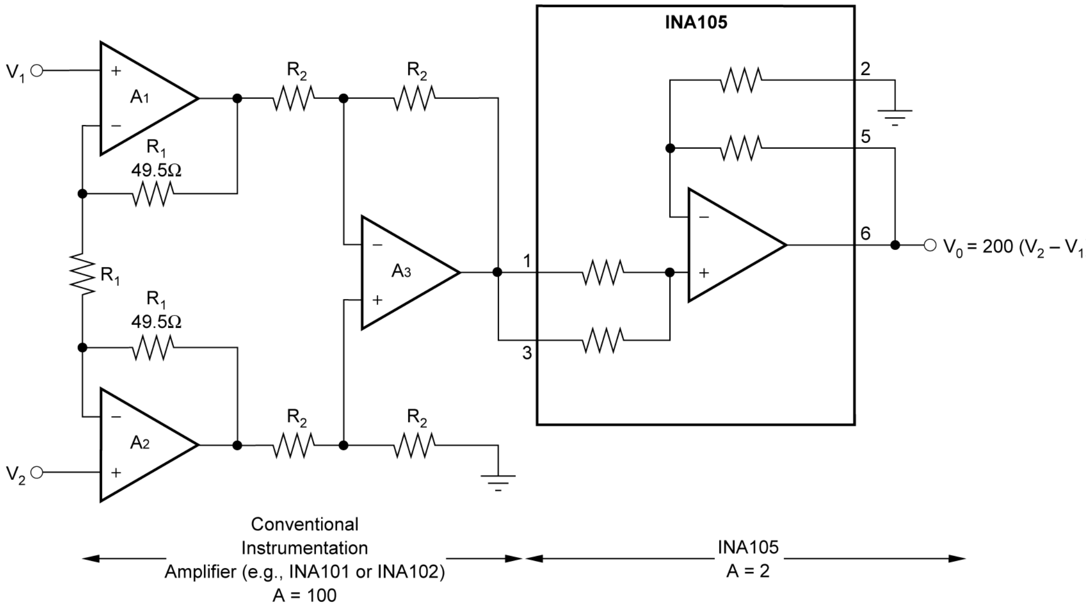


Figure 7-19. Boosting Instrumentation Amplifier Common-Mode Range From ±5V to ±7.5V With 10V Full-Scale Output

7.3.3 Voltage Reference Circuits

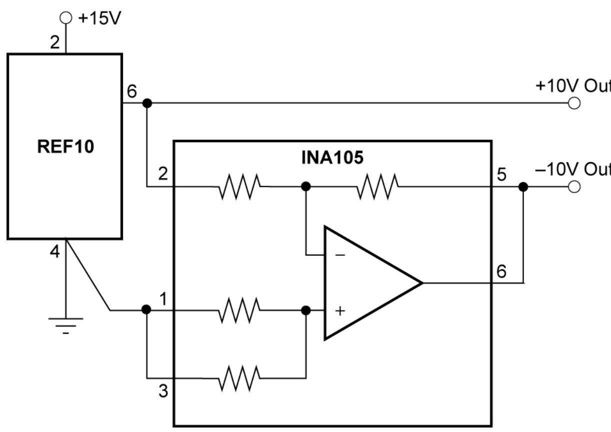


Figure 7-20. ±10V Precision Voltage Reference

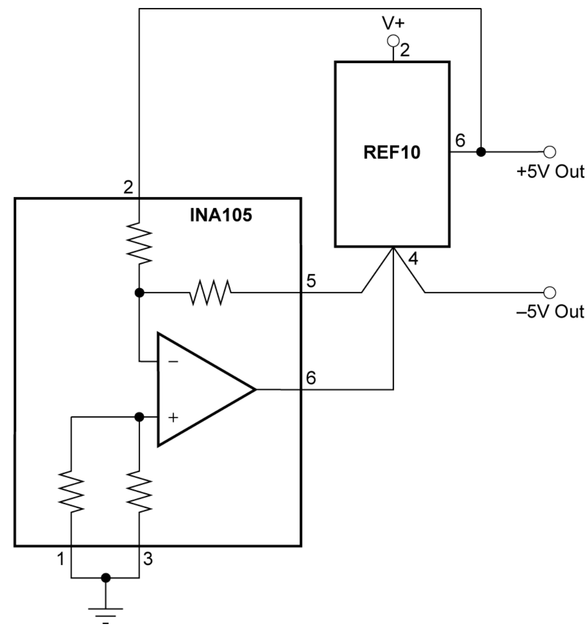


Figure 7-21. ±5V Precision Voltage Reference

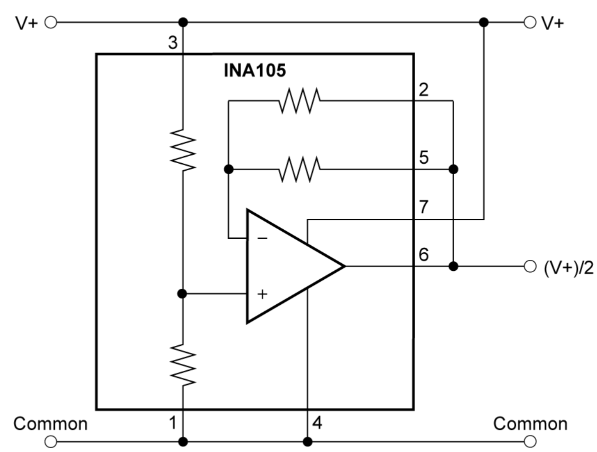


Figure 7-22. Pseudoground Generator

7.3.4 Special Function Circuits

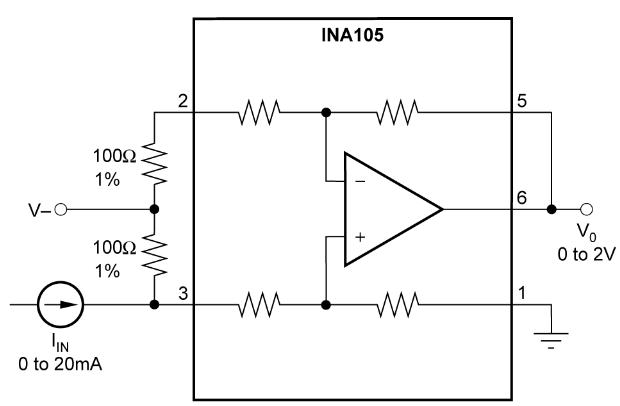


Figure 7-23. Current Receiver With Compliance to Rails

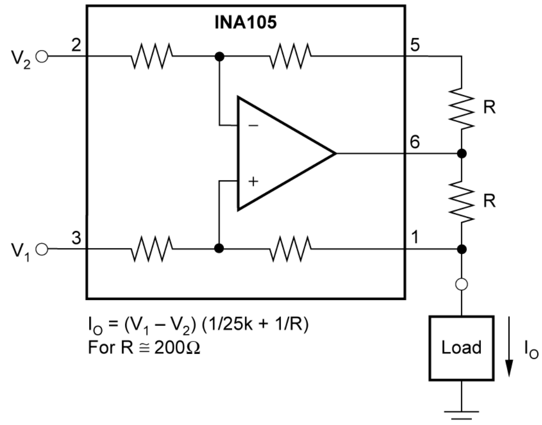


Figure 7-24. Precision Voltage-to-Current Converter With Differential Inputs

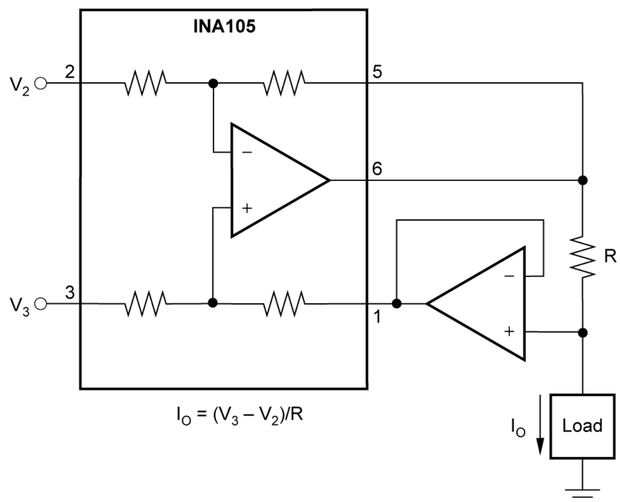


Figure 7-25. Differential Input Voltage-to-Current Converter for Low I_{OUT}

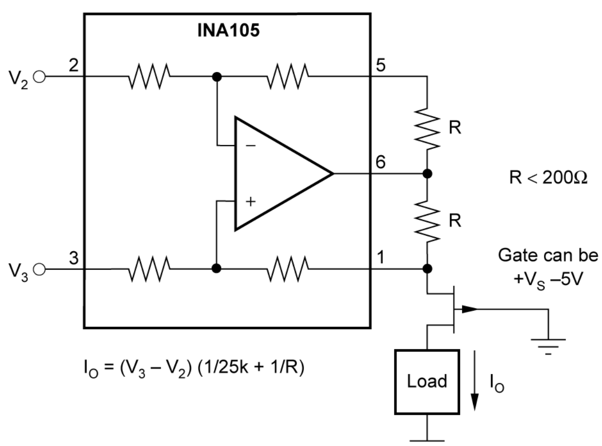


Figure 7-26. Isolating Current Source

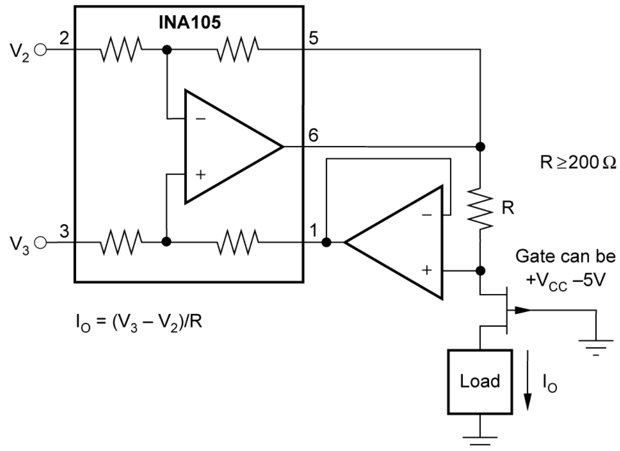


Figure 7-27. Isolating Current Source With Buffering Amplifier for Greater Accuracy

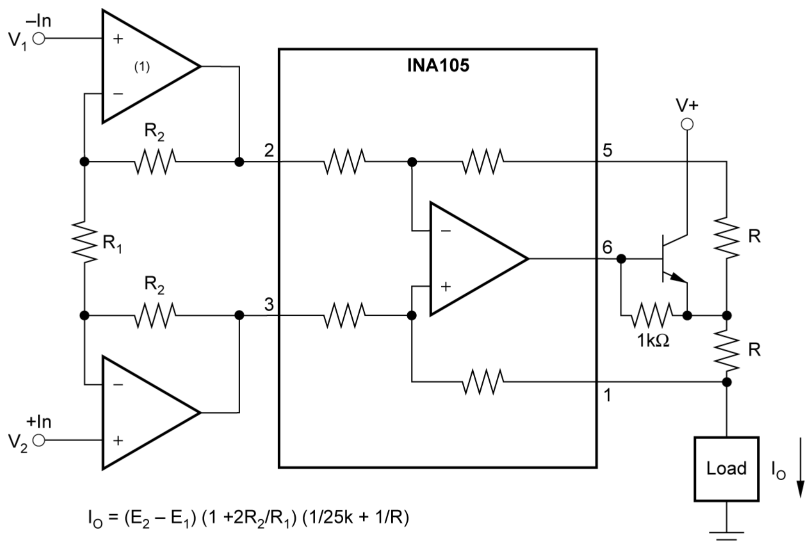


Figure 7-28. Precision Voltage-Controlled Current Source With Buffered Differential Inputs and Gain.

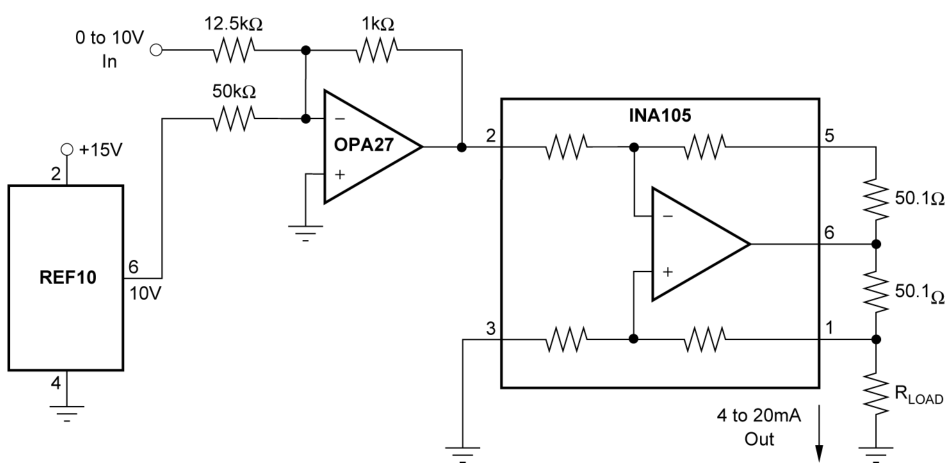


Figure 7-29. Precision 4mA to 20mA Current Transmitter

7.4 Power Supply Recommendations

The nominal performance of the INA105 is specified with a supply voltage of ±15V. The device operates using power supplies from ±5V to ±18V with varying performance. Parameters varying across the operating voltage and reference voltage range can be referenced in the *Typical Characteristics*.

TI highly recommends to add low-ESR ceramic bypass capacitors (C_{BYP}) between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Place the C_{BYP} as close to the device as possible to reduce coupling errors from noisy or high-impedance power supplies. Route the power supply trace through C_{BYP} before reaching the device power supply terminals. For more information, see *Layout Guidelines*.

7.5 Layout

7.5.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, route the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is preferred over crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

7.5.2 Layout Examples

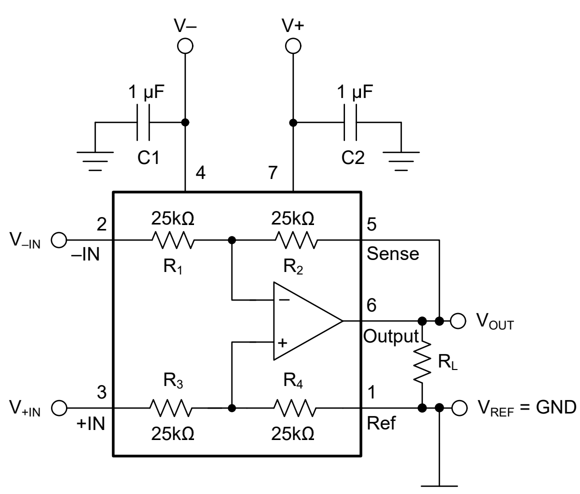


Figure 7-30. Example Schematic

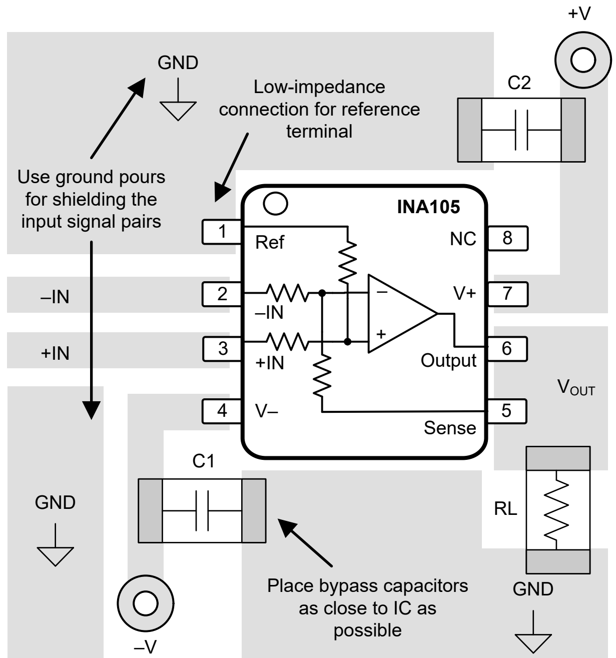


Figure 7-31. Associated PCB Layout for SOIC and PDIP Packages

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 Development Support

For development support on this product, see the following:

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA105AM	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	N / A for Pkg Type		INA105AM	Samples
INA105BM	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	N / A for Pkg Type		INA105BM	Samples
INA105KP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		INA105KP	Samples
INA105KU	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	INA 105U	
INA105KU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 105U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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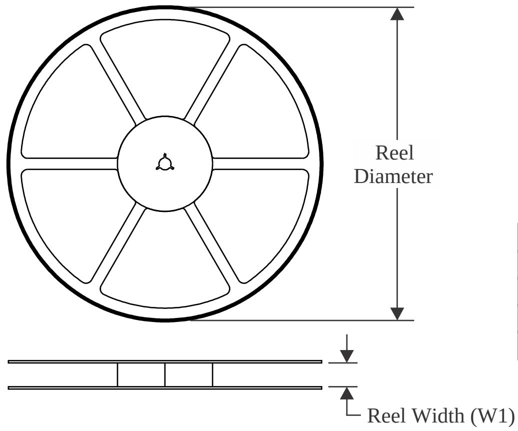
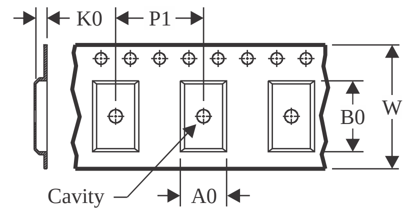
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

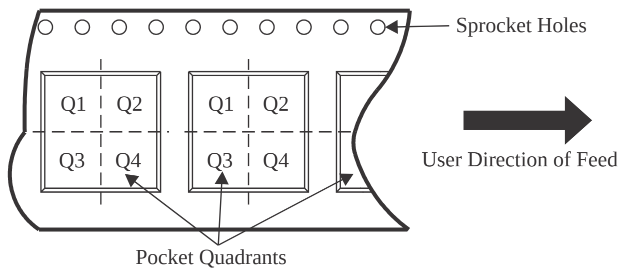


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

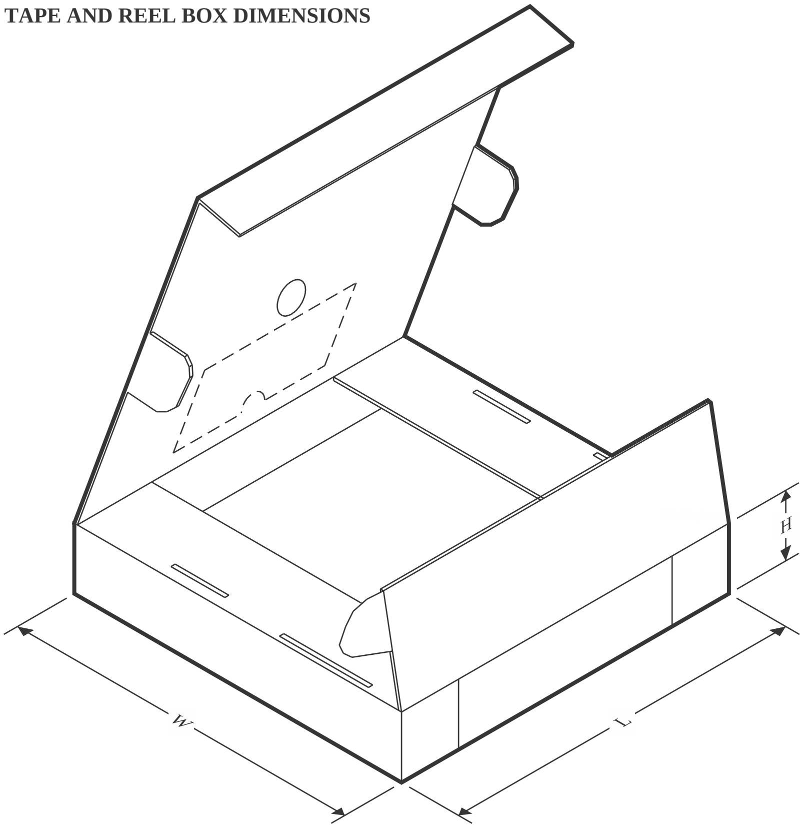
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA105KU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

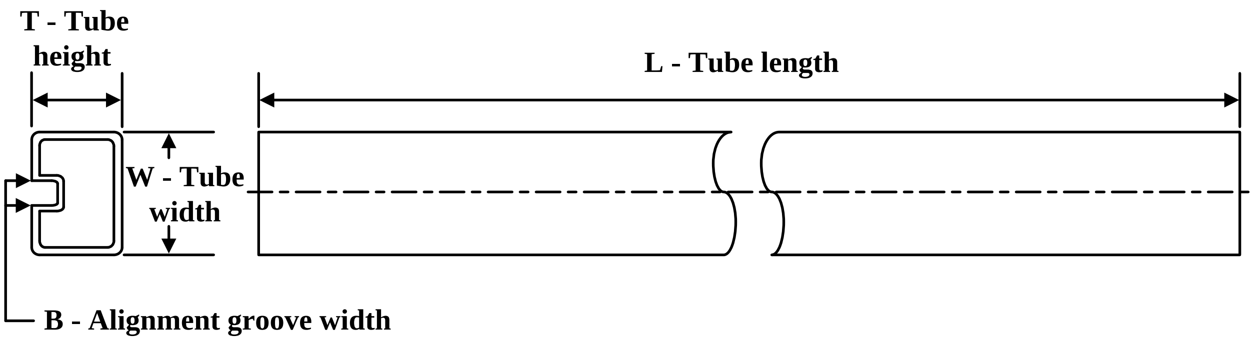
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA105KU/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA105AM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA105BM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA105KP	P	PDIP	8	50	506	13.97	11230	4.32
INA105KP	P	PDIP	8	50	506	13.97	11230	4.32

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