Burr-Brown Products from Texas Instruments

INA209

SBOS403 – JUNE 2007

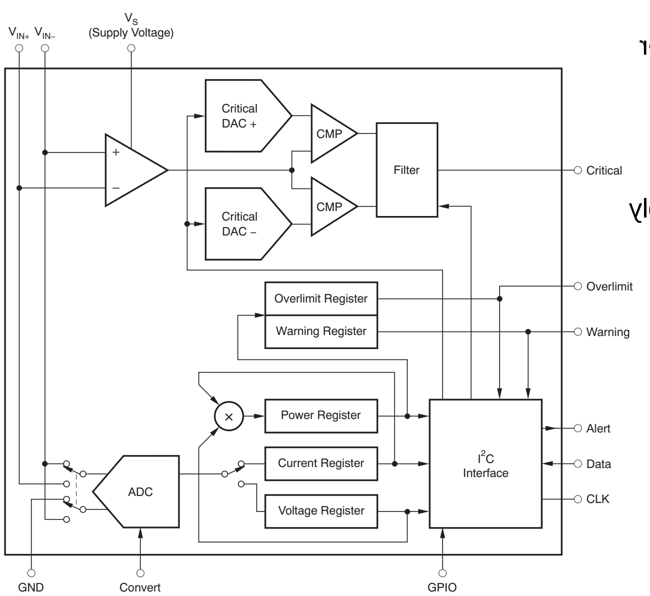
High-Side Measurement, Bi-Directional Current/Power Monitor with I2C™ Interface

FEATURES

- SENSES BUS VOLTAGES FROM 0V TO +26V
- REPORTS CURRENT, VOLTAGE, AND POWER; STORES PEAKS
- TRIPLE WATCHDOG LIMITS:
  - Warning with Delay
  - Over-limit with Delay
  - Critical Fast
- HIGH ACCURACY: 1% MAX OVER TEMP

APPLICATIONS

- SERVERS
- TELECOM EQUIPMENT
- AUTOMOTIVE
- POWER MANAGEMENT
- BATTERY CHARGERS
- WELDING EQUIPMENT
- POWER SUPPLIES
- TEST EQUIPMENT



DESCRIPTION

The INA209 is a high-side current shunt and power monitor with an I2C interface. The INA209 monitors both shunt drop and supply voltage. A programmable calibration value, combined with an internal multiplier, enables direct readouts in amperes. An additional multiplying register calculates power in watts. The INA209 features separate, onboard watchdog capabilities: warning comparator and over-limit comparator. The warning comparator is useful for monitoring lower limits with user-defined delay. The over-limit comparator assists monitoring upper limits that could require immediate system shutdown.

The INA209 also includes an analog comparator and a programmable digital-to-analog converter (DAC) that combine to provide the fastest possible responses to current overload conditions.

The INA209 can be used together with hot-swap controllers that already use current sense resistors. The INA209 full-scale range can be selected to be either the same or different than the hot-swap controller sense limits, within enough range to include them.

The INA209 senses across shunts on buses that can vary from 0V to 26V. The device uses a single +3V to +5.5V supply, drawing a maximum of 1.5mA of supply current. It is specified for operation from –25°C to +85°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA209	TSSOP-16	PW	INA209A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		INA209	UNIT
Supply Voltage, V_S		6	V
Analog Inputs, V_{IN+}, V_{IN-}	Differential $(V_{IN+}) - (V_{IN-})$(2)	–26 to 26	V
	Common-Mode	–0.3 to +26	V
Open-Drain Digital Output		GND – 0.3 to +6	V
GPIO, Convert Pins		GND – 0.3 to V_S + 0.3	V
Input Current Into Any Pin		5	mA
Open-Drain Digital Output Current		10	mA
Operating Temperature		–40 to +125	°C
Storage Temperature		–40 to +150	°C
Junction Temperature		+150	°C
ESD Ratings	Human Body Model	2000	V
	Charged-Device Model	1000	V
	Machine Model (MM)	150	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) V_{IN+} and V_{IN-} may have a differential voltage of –26V to +26V; however, the voltage at these pins must not exceed the range –0.3V to +26V.

ELECTRICAL CHARACTERISTICS: $+3.3V_S$

Boldface limits apply over the specified temperature range, T_A = **–25°C to +85°C**.
At T_A = +25°C, V_S = +3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32mV, PGA = ÷1, and BRNG = 1, unless otherwise noted.(1)

PARAMETER		CONDITIONS	INA209 MIN	TYP	MAX	UNIT
INPUT						
Full-Scale Current Sense (Input) Voltage Range		PGA = ÷1	0		±40	mV
		PGA = ÷2	0		±80	mV
		PGA = ÷4	0		±160	mV
		PGA = ÷8	0		±320	mV
Bus Voltage (Input Voltage) Range(2)		BRNG = 1	0		32	V
		BRNG = 0	0		16	V
Common-Mode Rejection	CMRR	V_{IN+} = 0V to 26V	100	120		dB
Offset Voltage, RTI(3)	V_{OS}	PGA = ÷1		±10	±100	μV
		PGA = ÷2		±20	±125	μV
		PGA = ÷4		±30	±150	μV
		PGA = ÷8		±40	±200	μV
vs Temperature				**0.1**		**μV/°C**
vs Power Supply	PSRR	V_S = 3V to 5.5V		10		μV/V
Current Sense Gain Error				±40		m%
vs Temperature				**10**		**ppm/°C**
Input Impedance		Active Mode				
V_{IN+} Pin				20		μA
$V_{IN–}$ Pin				20 || 320		μA || kΩ
Input Leakage		Power-Down Mode				
V_{IN+} Pin				0.1	±0.5	μA
$V_{IN–}$ Pin				0.1	±0.5	μA
DC ACCURACY						
ADC Basic Resolution				12		Bits
1 LSB Step Size						
Shunt Voltage				10		μV
Bus Voltage				4		mV
Current Measurement Error				±0.2	±0.5	%
over Temperature					**±1**	**%**
Bus Voltage Measurement Error				±0.2	±0.5	%
over Temperature					**±1**	**%**
Differential Nonlinearity				±0.1		LSB
Critical DAC Full-Scale Range				255		mV
Critical DAC Accuracy				±0.5	±1	%
Critical DAC Resolution				8		Bits
Critical DAC 1 LSB Step Size				1		mV
Critical DAC Comparator Offset				±0.3	±1.6	mV
Critical DAC Comparator Hysteresis(4)				See(4)		
Critical DAC Comparator Delay				5		μs

(1) BRNG is bit 13 of the Configuration Register.
(2) This parameter expresses the full-scale range of the ADC scaling. In no event should more than 26V be applied to this device.
(3) Referred-to-input (RTI).
(4) User-programmable. See the Critical DAC and Comparator Register sections.

TEXAS INSTRUMENTS
www.ti.com

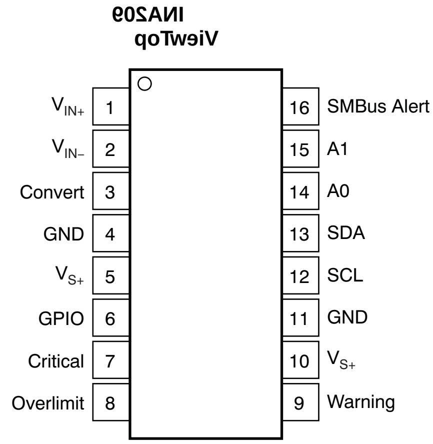
ELECTRICAL CHARACTERISTICS (V_S = +3.3V) (continued)

Boldface limits apply over the specified temperature range, **T_A = –25°C to +85°C**.
At T_A = +25°C, V_S = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – V_{IN-}) = 32mV, PGA = ÷ 1, and BRNG = 1, unless otherwise noted.

PARAMETER	CONDITIONS	INA209 MIN	TYP	MAX	UNIT
ADC TIMING					
ADC Conversion Time	12-Bit		532	586	μs
	11-Bit		276	304	μs
	10-Bit		148	163	μs
	9-Bit		84	93	μs
Minimum Convert Input Low Time		4			μs
SMBus					
SMBus Timeout[5]			28	35	ms
DIGITAL INPUTS (SDA as Input, SCL, A0, A1, GPIO and Convert)					
Input Capacitance			3		pF
Leakage Input Current	$0 \leq V_{IN} \leq V_S$		0.1	1	μA
Input Logic Levels:					
V_{IH}		0.7 (V_S)		6	V
V_{IL}		–0.3		0.3 (V_S)	V
Hysteresis			500		mV
DIGITAL OUTPUTS					
Low Output Pin (GPIO)	I_{SINK} = 3mA		0.15	0.4	V
High Output Pin (GPIO)	I_{SOURCE} = 3mA	V_S – 0.4	V_S – 0.15		V
OPEN-DRAIN DIGITAL OUTPUTS (SDA, Alert, Warning, Over-Limit, Critical)					
Logic Output Level	I_{SINK} = 3mA		0.15	0.4	V
High-Level Output Leakage Current	V_{OUT} = V_S		0.1	1	μA
POWER SUPPLY					
Operating Supply Range		+3		+5.5	V
Quiescent Current			1	1.5	mA
Quiescent Current, Power-Down Mode			6	15	μA
Power-On Reset Threshold			2		V
TEMPERATURE RANGE					
Specified Temperature Range		–25		+85	°C
Operating Temperature Range		–40		+125	°C
Thermal Resistance	θ_{JA}				
TSSOP-16			+150		°C/W

(5) SMBus timeout in the INA209 resets the interface any time SCL is low for over 28ms.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

PIN NO.	NAME	DESCRIPTION
1	V_{IN+}	Positive differential shunt voltage. Connect to positive side of shunt resistor.
2	V_{IN-}	Negative differential shunt voltage. Connect to negative side of shunt resistor. Bus voltage is measured from this pin to ground.
3	Convert	Used to trigger conversions in triggered mode. In triggered mode, this pin should normally be held low, and brought high to start each conversion. The ADC conversion is taken immediately after the pin is returned low, 4μs after high. Convert should be tied high if this pin is not used; the triggered mode command is written via the bus.
4	GND	Connect together with pin 11 to ground.
5	V_{S+}	Connect together with pin 10, 3V to 5.5V supply.
6	GPIO	General-purpose user-programmable input/output. Totem-pole output. Connect to ground or supply if unused. Default condition is as an input.
7	Critical	Open-drain Critical watchdog output (filter set in Critical DAC Register); Default condition disabled; transparent active-low (non-latched).
8	Overlimit	Open-drain over-limit watchdog output. Default condition disabled; transparent active-low (non-latched).
9	Warning	Open-drain warning watchdog output (delay set in Critical DAC Register); Default condition is disabled; transparent active-low (non-latched).
10	V_{S+}	Connect together with pin 5, 3V to 5.5V supply.
11	GND	Connect together with pin 4 to ground.
12	SCL	Serial bus clock line.
13	SDA	Serial bus data line.
14	A0	Address pin. Table 1 shows pin settings and corresponding addresses.
15	A1	Address pin. Table 1 shows pin settings and corresponding addresses.
16	SMBus Alert	Open-drain SMBus Alert output controlled by SMBus Alert Mask Register. Default disabled.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32mV, PGA = 8, and BRNG = 11, unless otherwise noted.

RESPONSE FREQUENCY

Figure 1.

TEMPERATURE OFFSET SHUNT ADC

Figure 2.

TEMPERATURE GAIN SHUNT ADC

Figure 3.

TEMPERATURE OFFSET VOLTAGE ADC

Figure 4.

TEMPERATURE GAIN BUS ADC

Figure 5.

NONLINEARITY VOLTAGE

Figure 6.

(continued)

Critical Comparator +
Critical Comparator –
Offset (mV)
Temperature (°C)

Critical Comparator –
Critical Comparator +
Full-Scale Error (mV)
Temperature (°C)

V_{S+} = 5V
V_{S+} = 3V
V_{S+} = 3V
V_{S+} = 5V
Input Currents (mA)
V_{IN-} Voltage (V)

V_S = 5V
V_S = 3V
I_Q (mA)
Temperature (°C)

V_S = 5V
V_S = 3V
I_Q (µA)
Temperature (°C)

V_S = 5V
V_S = 3V
I_Q (mA)
SCL Frequency (Hz)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – 32mV), PGA = ÷1, and BRNG = 32V, unless otherwise noted.

Figure 13.

FUNCTIONAL BLOCK DIAGRAM

Figure 14.

APPLICATION INFORMATION

The INA209 is a digital current-shunt monitor with an I²C- and SMBus-compatible interface. It provides digital current, voltage, and power readings necessary for accurate decision-making in precisely-controlled systems. Programmable registers allow flexible configuration for measurement resolution, continuous-versus-triggered operation, and warning, critical limits. Detailed register information appears at the end of this data sheet, beginning with Table 2. See the Functional Block Diagram for a block diagram of the INA209.

The INA209 offers compatability with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another. I²C will be used throughout this data sheet, with SMBus being specified only when a difference between the two systems is being addressed. Two bi-directional lines, SCL and SDA, connect the INA209 to the bus. Both SCL and SDA are open-drain connections. Figure 15 shows a typical application circuit.

BUS OVERVIEW

The device that initiates the transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions.

To address a specific device, a master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH will be interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The INA209 includes a 28ms timeout on its interface to prevent locking up an SMBus.

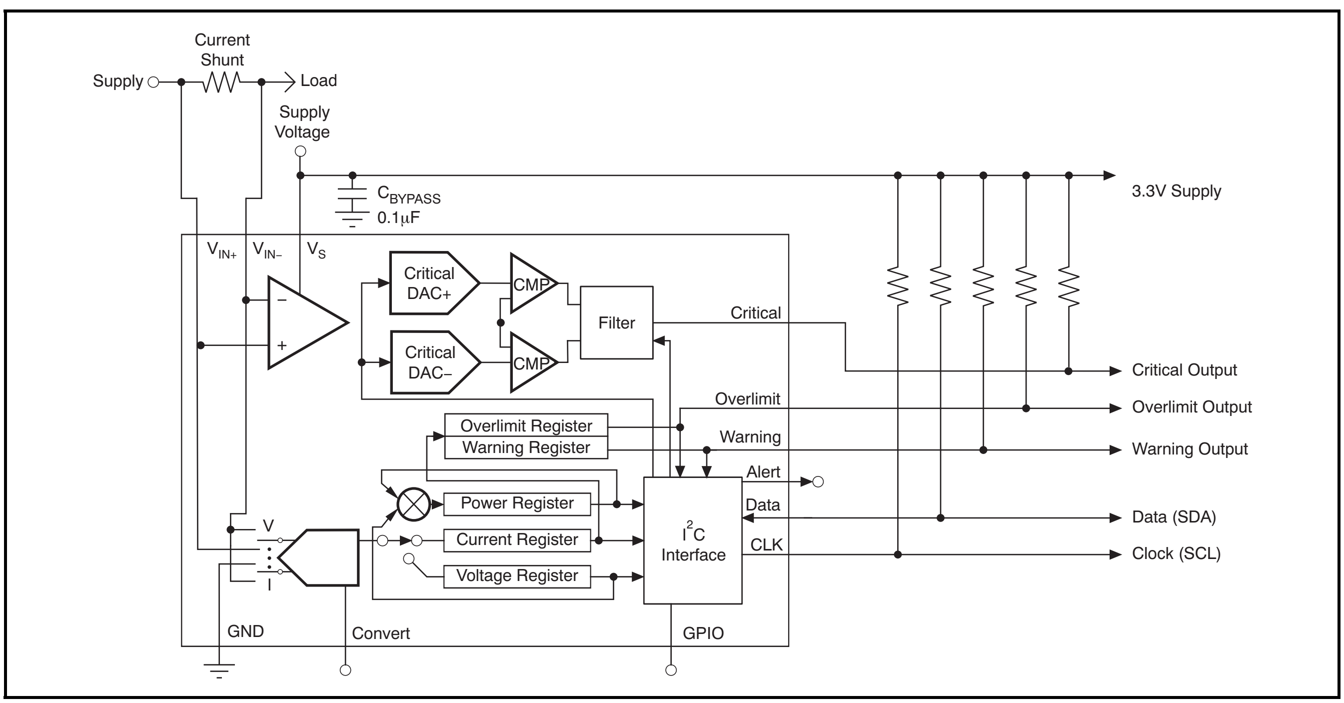


Figure 15. Typical Application Circuit

Serial Bus Address

The INA209 has two address pins, A0 and A1. The address pins are read at the start of each communication event.

Table 8. INA209 Address Pins and Slave Addresses

A1	A0	ADDRESS
GND	GND	1000000
GND	$+V_S$	1000001
GND	SDA	1000010
GND	SCL	1000011
$+V_S$	GND	1000100
$+V_S$	$+V_S$	1000101
$+V_S$	SDA	1000110
$+V_S$	SCL	1000111
SDA	GND	1001000
SDA	$+V_S$	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	$+V_S$	1001101
SCL	SDA	1001110
SCL	SCL	1001111

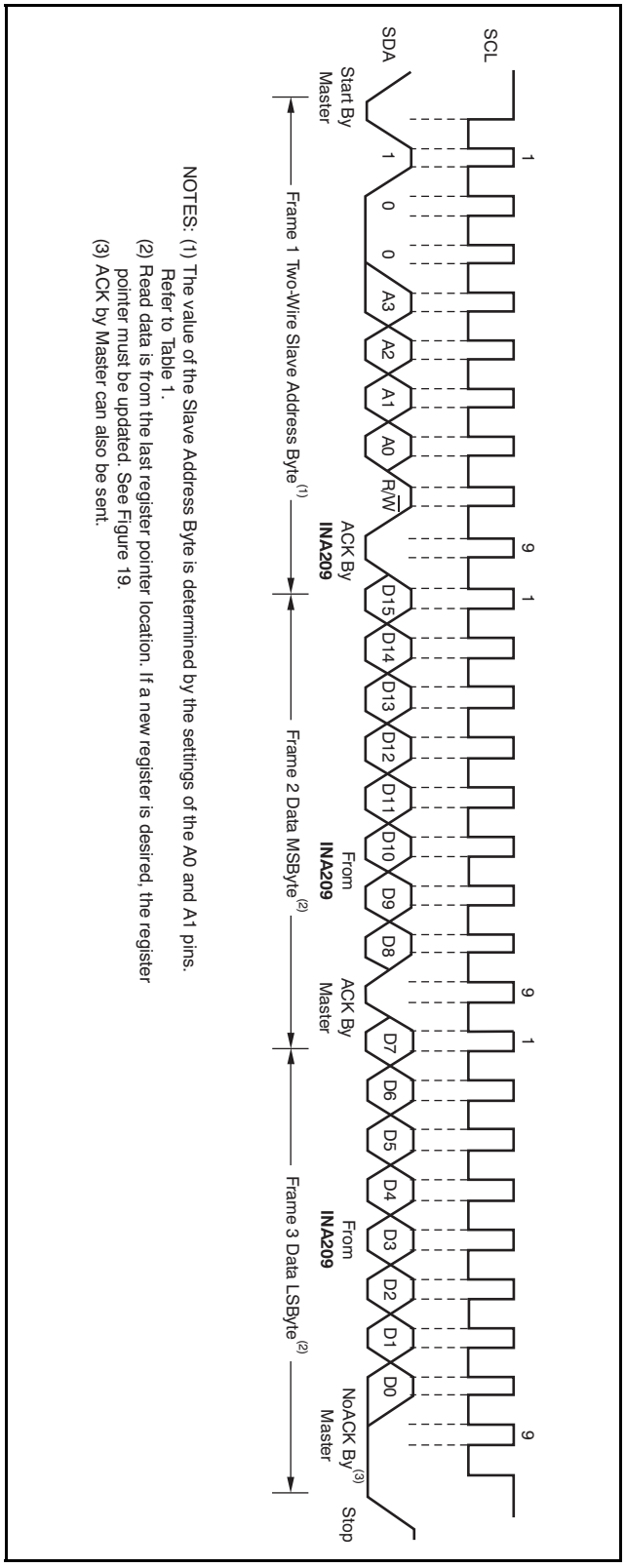
Serial Interface

WRITING TO/READING FROM THE INA209

register. The next two bytes are written to

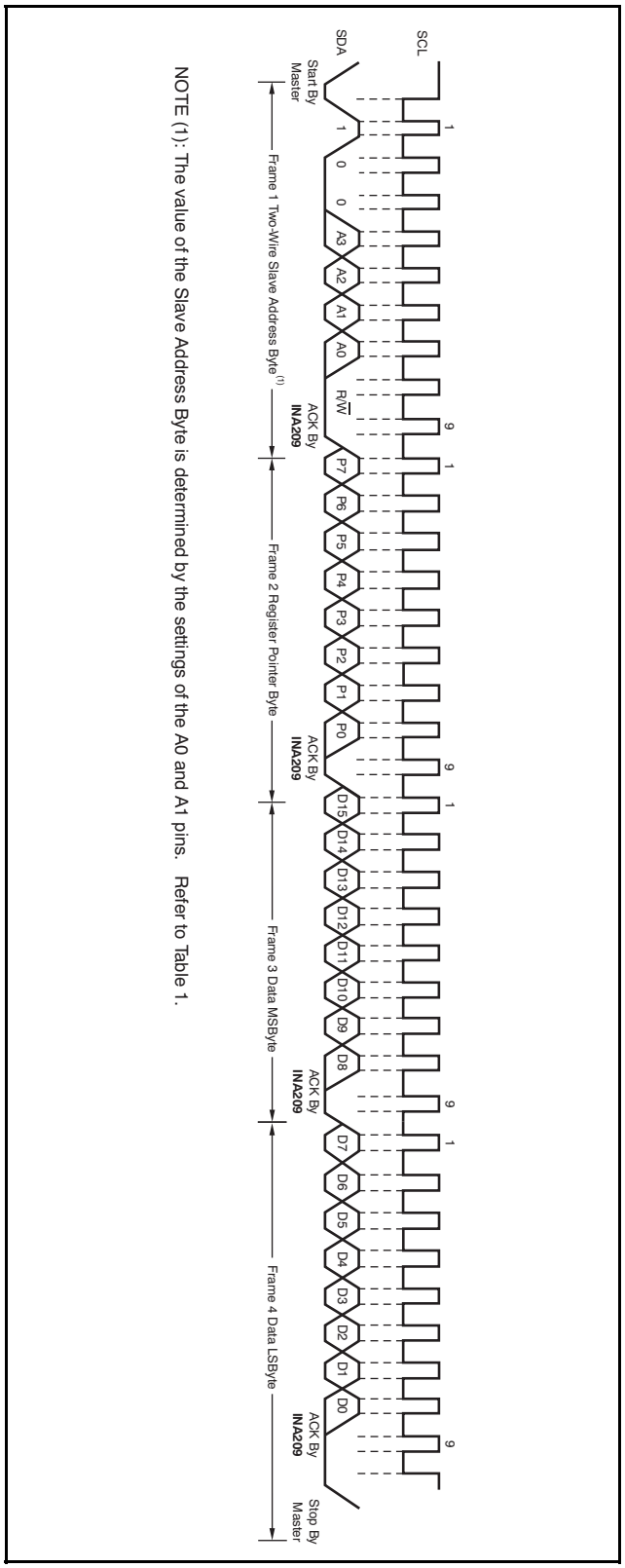
the R/$\overline{W}$ bit LOW. Every write operation to the

address, with the R/$\overline{W}$ bit LOW. The INA209 then



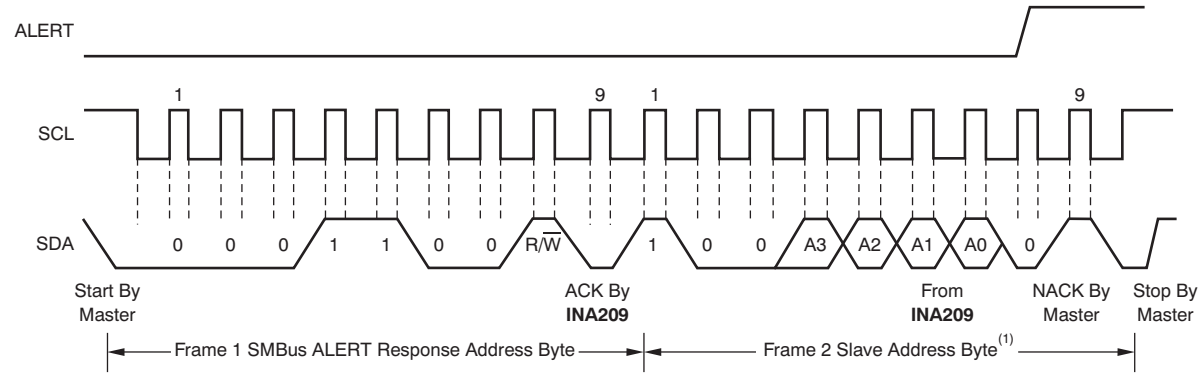
NOTES: (1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.
(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 19.
(3) ACK by Master can also be sent.

Figure 17. Timing Diagram for Read Word Format



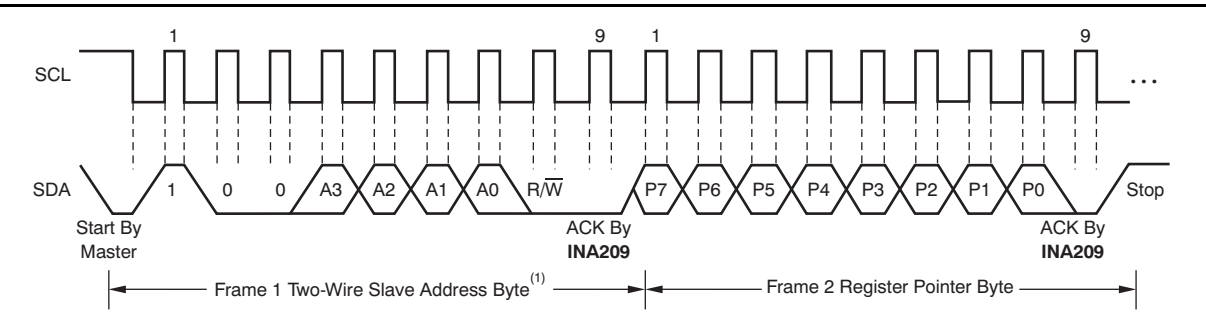
NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 16. Timing Diagram for Write Word Format



NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

ALERT SMBus Diagram Timing Figure



NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Set Pointer Register Type Figure

High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up devices. The master generates a start condition followed by a valid serial byte containing High-Speed (HS) master code 00001XXX. This transmission is made in fast (400kbps) or standard (100kbps) (F/S) mode at no more than 400kbps. The INA209 does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 3.4Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4Mbps are allowed. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the INA209 to support either F/S transmission mode.

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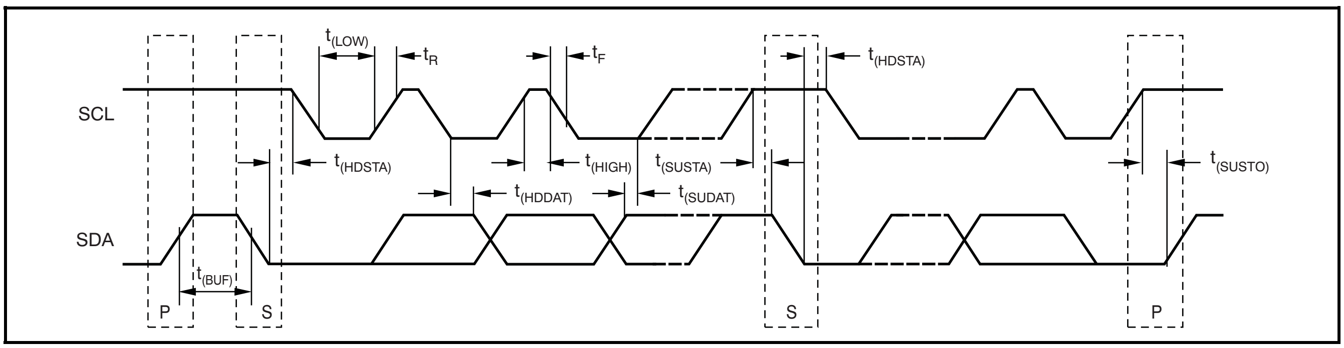


Figure 20. Bus Timing Diagram

Bus Timing Diagram Definitions

PARAMETER		FAST MODE MIN	FAST MODE MAX	HIGH-SPEED MODE MIN	HIGH-SPEED MODE MAX	UNITS
SCL Operating Frequency	$f_{(SCL)}$	0.001	0.4	0.001	3.4	MHz
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated	$t_{(HDSTA)}$	100		100		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	100		100		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	100		100		ns
Data Hold Time	$t_{(HDDAT)}$	0		0		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCL Clock LOW Period	$t_{(LOW)}$	1300		160		ns
SCL Clock HIGH Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time	t_R		300		160	ns
Clock/Data Rise Time for SCLK ≤ 100kHz	t_R		1000			ns

Power-Up Conditions

BASIC ADC FUNCTIONS

Measurements and Shunt

INA209 Configuration

When the INA209 is in the normal operating mode (that is, MODE bits of the Configuration Register are set to '111'), it continuously converts the shunt voltage up to the number set in the shunt voltage averaging function (Configuration Register, SADC bits). The device then converts the bus voltage up to the number set in the bus voltage averaging (Configuration Register, BADC bits). The Mode control in the Configuration Register also permits selecting modes to convert only voltage or current, either continuously or in response to an event (triggered).

All current and power calculations are performed in the background and do not contribute to conversion time; conversion times shown in the Electrical Characteristics table can be used to determine the actual conversion time.

Power-Down mode reduces the quiescent current and turns off current into the INA209 inputs, avoiding any supply drain. Full recovery from Power-Down requires 40 μs. ADC Off mode (set by the Configuration Register, MODE bits) stops all conversions.

In triggered mode, the external Convert line becomes active. Conversion is initiated by taking the Convert line low for a minimum of 4 μs. Any time the Convert line goes low while a conversion is underway, the Convert is disregarded and ignored, until the conversion ends. There are several triggered modes; however, all available conversions are repeatedly performed up to the number set in the Averaging function (Configuration Register, BADC and SADC bits).

If the Convert line is held low, writing any of the triggered convert modes into the Configuration Register (even if the desired mode is already programmed into the register) triggers a single-shot conversion.

Although the INA209 can be read at any time, and the data from the last conversion remain available, the Conversion Ready bit (Status Register, CNVR bit) is provided to help co-ordinate one-shot or triggered conversions. The Conversion Ready bit is set after all conversions, averaging, and multiplication operations are complete.

The Conversion Ready bit clears under these conditions:

- Writing to the Configuration Register, except when configuring the MODE bits for Power Down or ADC off (Disable) modes;
- Reading the Status Register; or
- Triggering a single-shot conversion with the Convert pin.

Power Measurement

Current and bus voltage are converted at different points in time, depending on the resolution and averaging mode settings. For instance, when configured for 12-bit and 128 sample averaging, up to 68ms in time between sampling these two values is possible. Again, these calculations are performed in the background and do not add to the overall conversion time.

Peak-Hold Registers

Shunt voltage peak registers hold the lowest and highest value read for the shunt. The converted shunt value may be either positive or negative; as a result, there is no need for a sign bit in the registers. For instance, the Shunt Voltage Positive Peak Register records the most positive voltage; in unidirectional current measurement systems, this is the common case. The Shunt Voltage Negative Peak Register also records positive voltage. However, certain conditions can occur normally in unidirectional systems that cause negative polarity events across the shunt; these events are recorded in their Shunt Voltage Negative Peak Register.

Peak-hold registers do not record conditions that trigger Critical shutdown. Comparator shutdown occurs within 5 μs of detecting a critical condition, while the ADC conversion requires 532 μs to record a peak. Therefore, the shutdown system removes the fault before the ADC can record it.

Critical Comparator

The Critical Comparator function is included to provide the fastest possible response to overload events. This function bypasses the digital circuitry, capturing the event in the analog domain.

The Critical Comparator responds only to shunt voltage, and can be programmed for a value from 0mV to 255mV in 1mV increments (Critical DAC+ and Critical DAC– Register). Two thresholds are provided, allowing users to set different thresholds for bi-directional current measurement systems. For example, a power supply may readily be sourcing 10A, but must alarm whenever sinking more than 1A. The SMBus Alert Mask/Enable Control Register allows the user to enable or disable the Critical output through the CREN bit. CREN affects only the Critical pin; it does not affect the CRIT flags within the Status Register.

The Critical DAC Comparator output filter is set by the GF bits of the Critical DAC– Register. This filter determines the duration of time that the CMP output must continuously be active (toggling) to propagate to the Critical output pin and set the CRIT+ or CRIT– flags within the Status Register.

While the Critical DAC Comparator output filter provides settings from 0ms to 0.96ms, the CMP is actually strobed every 4µs, providing multiple samples per delay period. For the Critical output to become active, the critical condition must be true for every sample during the specified delay period.

When using the Critical Comparator in unidirectional applications, where the Critical DAC– Register is unused, the input trip error for the Comparator could be near zero, because the comparator has an offset of up to ±1.5mV. Noise contributes to unintended tripping. To avoid tripping in unidirectional applications, the Critical DAC– should be programmed to a value beyond 2mV to account for the offset and an additional amount to provide noise immunity. Alternatively, the Critical DAC– can be programmed to full-scale negative range (–255mV), to eliminate tripping.

PGA Function

If larger full-scale shunt voltages are desired, the INA209 provides a PGA function that increases the full-scale range up to 2, 4, or 8 times (320mV). Additionally, the bus voltage measurement has two full-scale ranges: 16V or 32V.

Compatibility with TI Hot Swap Controllers

The INA209 is designed for compatibility with hot swap controllers such as the TPS2490. The TPS2490 uses a high-side shunt with a limit at 50mV; the INA209 full-scale range of 40mV enables the use of the same shunt for current sensing below this limit. When sensing is required at (or through) the 50mV sense point of the TPS2490, the PGA of the INA209 can be set to ÷2 to provide an 80mV full-scale range.

A typical application connects the Critical output pin to enable the TPS2490; in this configuration, the user-programmable Critical output provides a user-programmable current limit. Note that latched mode should be used for the Critical pin output to avoid oscillation at the trip level.

Filtering and Input Considerations

Measuring current is often noisy, and such noise can be difficult to define. The INA209 offers several options for filtering by choosing resolution and averaging in the Configuration Register. These filtering options can be set independently for either voltage or current measurement.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500kHz (±30%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1MHz and higher, they can be dealt with by incorporating filtering at the input of the INA209. The high frequency enables the use of low-value series resistors on the filter with negligible effects on measurement accuracy. Figure 22 shows the INA209 with an additional filter added at the input.

Figure 22. INA209 with Filtering Inputs

SMBus Responses

with Acquisition Multichannel Figure
Sampling Simultaneous

Multichannel Data Acquisition

Additional External Circuitry V$_{BUS}$ Input

External control can be used with the INA209 GPIO to switch the V$_{BUS}$ measurement circuit to an alternate location. Switching is most often done to perform measurements on the opposite side of the MOSFET series switch with the shunt resistor. Considerations must be given to the typical 11 μA current along the input, of the INA209 for the 320k impedance present at the V$_{IN–}$ input where the voltage is measured. These effects can create errors through the external resistance the switching method used. The easiest way to avoid these errors is to reduce the resistance to a minimum by selecting MOSFET switches with the lowest R$_{DS(on)}$ values possible.

The circuit shown in Figure 24 pairs MOSFETs back-to-back to reduce the package built-in body diode. Each pair must be used because of the source-to-drain diode back circuit in this shunt with the V$_{IN–}$ input for the normal connection that is for the optional voltage measurement output of the control FET.

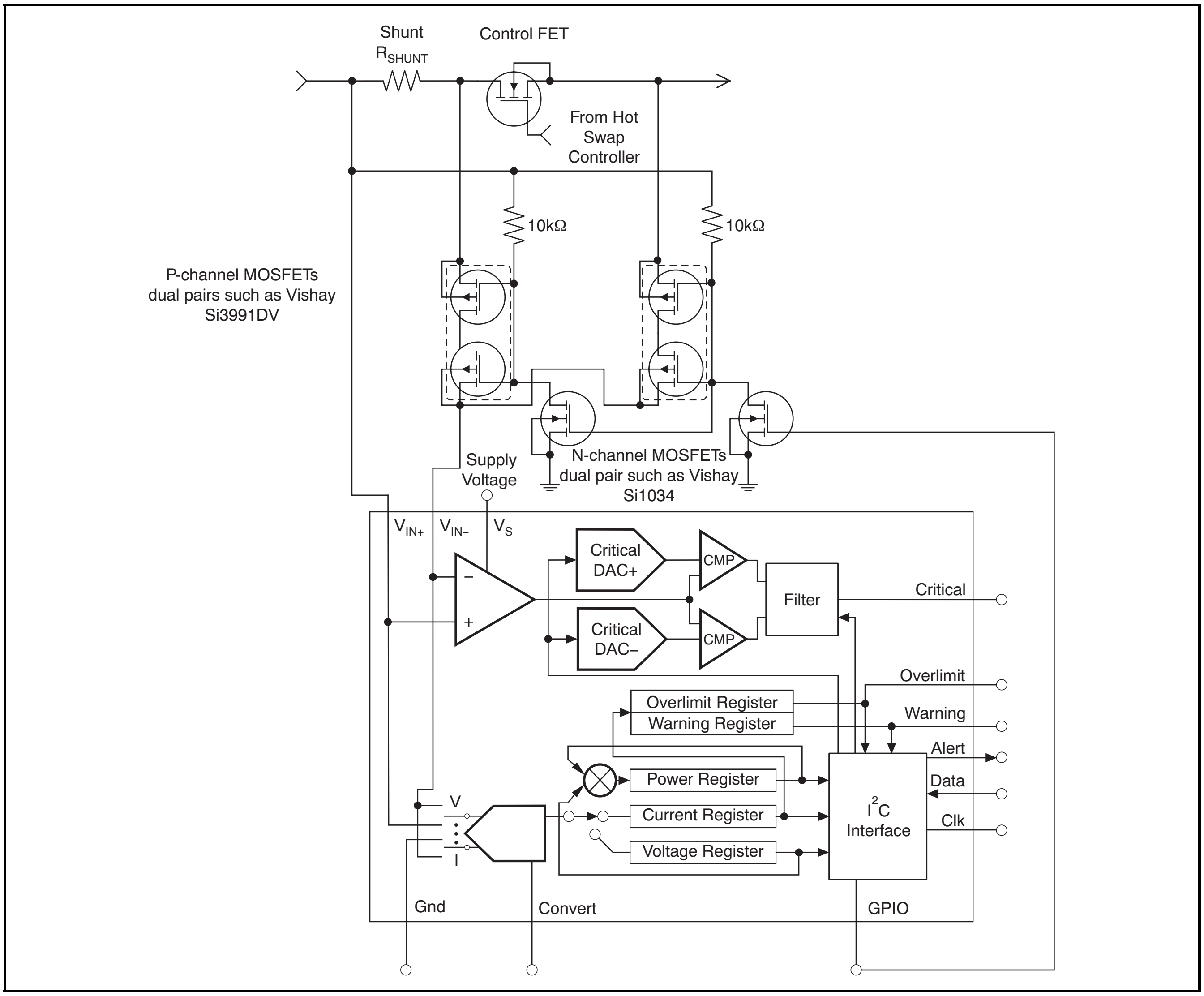


Figure 24. Additional External Circuitry V$_{BUS}$ Input

Calibration Register and Scaling

$$MaxI = \frac{V_{SHUNT}}{R_{SHUNT}} \quad (1)$$

$$Current\_LSB = \frac{Max\_Expected\_I}{CurrentRegisterh} \quad (2)$$

$$Current\_LSB = \frac{Max\_Expected\_I}{7FFFh} = \frac{Max\_Expected\_I}{32767} \quad (3)$$

$$Current\_LSB = \frac{Max\_Expected\_I}{1FFFh} = \frac{Max\_Expected\_I}{8191} \quad (4)$$

$$Current\_LSB = \frac{Max\_Expected\_I}{FA0h} = \frac{Max\_Expected\_I}{4000d} \quad (5)$$

$$Cal = trunc\left(\frac{0.04096}{Current\_LSB \times R_{SHUNT}}\right) \quad (6)$$

$$Power\_LSB = Volt\_LSB \times Current\_LSB \times 5000 = Power\_LSB = 20 \times Current\_LSB \quad (7)$$

Compute the maximum current and shunt voltage values (before overflow), as shown by Equation 8 and Equation 9:

$$Max\_Current = Current\_LSB \times 7FFFh = Current\_LSB \times 32767 \quad (8)$$

$$Max\_ShuntVoltage = Max\_Current \times R_{SHUNT} \quad (9)$$

Typical Design Example

This section presents a typical design example for using the INA209 as described in the previous section. For this example, we will assume a nominal 12V system.

1. Establish the following parameters:
   Maximum bus voltage: V_{BUS} = 16V
   Shunt resistor: R_{SHUNT} = 0.01 Ω
   Desired maximum drop across the shunt V_{SHUNT} (based on programming the INA209 for 40mV full-scale range)
2. Determine the maximum possible current using Equation 10:

$$MaxI = \frac{V_{SHUNT}}{R_{SHUNT}} = \frac{0.04}{0.01} = 4A \quad (10)$$

3. Choose the desired maximum current value, Max_Expected_I ≤ MaxI. For this example, we will use 2A.
4. Calculate the possible range of current LSBs. Calculate this from the general form given by Equation 2.

For this example, we will calculate three possible methods of Calibration Register current value using:

First, use Equation 11 to fill the Calibration Register to get the highest possible Max_Expected_I accuracy resolution:

$$Current\_LSB = \frac{Max\_Expected\_I}{7FFFh} = \frac{Max\_Expected\_I}{32767} = \frac{2}{32767} = 61.037^{-6} A \quad (11)$$

The second method, using Equation 12, generates LSB based on required 13-bit resolution:

$$Current\_LSB = \frac{Max\_Expected\_I}{1FFFh} = \frac{Max\_Expected\_I}{8191} = \frac{2}{8191} = 244.17^{-6} A \quad (12)$$

The third option: current LSB that must be less than specified by Equation 2; in this instance, chose to set the current LSB equal to:

100^{-6} A

This option provides a straightforward value for calculations, assuming that LSB value is within the ranges of resolution given by Equation 11 and Equation 12.

5. Now compute the Calibration Register according to Equation 13:

$$Cal = trunc\left[\frac{0.04096}{Current\_LSB \times R_{SHUNT}}\right] = trunc\left[\frac{0.04096}{100^{-6} \times 0.01}\right] = 20480d = 5000h \quad (13)$$

6. Then calculate the Power LSB, using Equation 14:

$$Power\_LSB = Volt\_LSB \times Current\_LSB \times 5000 = Power\_LSB = 20 \times Current\_LSB = 2^{-3} A \quad (14)$$

7. Finally, compute the maximum current and shunt voltage values (before overflow), as shown by Equation 15 and Equation 16:

$$Max\_Current = Current\_LSB \times 7FFFh = Current\_LSB \times 32767 = 2^{-3} \times 32767 = 3.2767A \quad (15)$$

$$Max\_ShuntVoltage = Max\_Current \times R_{SHUNT} = 3.2767 \times 0.01 = 32.767^{-3} \quad (16)$$

REGISTER INFORMATION

The INA209 uses a bank of registers for holding configuration settings, measurement results, maximum/minimum limits, and status information. Table 2 summarizes the INA209 registers; Figure 14 illustrates them. Register contents are updated 4µs after completion of the write command. Therefore, a 4µs delay is required between completion of a write to a given register and a subsequent read of that register (without changing the pointer) when using SCL frequencies in excess of 1MHz.

Table 2. Summary of Register Set

POINTER ADDRESS			POWER-ON RESET		
HEX	REGISTER NAME	FUNCTION	BINARY	HEX	TYPE (1)
00	Configuration Register	All-register reset, settings for bus voltage range, PGA Gain, ADC resolution/averaging.	00111001 10011111	399F	R/W
01	Status Register	Status flags for warnings, over-/under-limits, conversion ready, math overflow, and SMBus Alert.	00000000 00000000	0000	R
02	SMBus Alert Mask/Enable Control Register	Enables/disables flags in the Status Register	00000000 00000000	0000	R/$\overline{W}$
03	Shunt Voltage	Shunt voltage measurement data.	00000000 00000000	0000	R
04	Bus Voltage	Bus voltage measurement data.	00000000 00000000	0000	R
05	Power	Power measurement data.	00000000 00000000	0000	R
06	Current	Contains the value of the current flowing through the shunt resistor (2)	00000000 00000000	0000	R
07	Shunt Voltage Positive Peak	Contains most positive voltage reading of Shunt Voltage Register	10000000 00000000	8000	R/$\overline{W}$
08	Shunt Voltage Negative Peak	Contains most negative voltage reading of Shunt Voltage Register	01111111 11111111	7FFF	R/$\overline{W}$
09	Bus Voltage Maximum Peak	Contains highest voltage reading of Bus Voltage Register	00000000 00000000	0000	R/$\overline{W}$
0A	Bus Voltage Minimum Peak	Contains lowest voltage reading of Bus Voltage Register	11111111 11111000	FFF8	R/$\overline{W}$
0B	Power Peak	Contains highest power reading of Power Register	00000000 00000000	0000	R/$\overline{W}$
0C	Shunt Voltage Positive Warning	Sets positive shunt voltage limit that triggers a warning flag in the Status Register and activates Warning pin.	00000000 00000000	0000	R/$\overline{W}$
0D	Shunt Voltage Negative Warning	Sets negative shunt voltage limit that triggers a warning flag in the Status Register and activates Warning pin.	00000000 00000000	0000	R/$\overline{W}$
0E	Power Warning	Sets power limit that triggers a warning flag in the Status Register and activates Warning pin.	00000000 00000000	0000	R/$\overline{W}$
0F	Bus Over-Voltage Warning	Sets bus voltage limit that triggers a warning flag in the Status Register and activates Warning pin. Also contains bits to set Warning pin polarity and latch feature.	00000000 00000000	0000	R/$\overline{W}$

(1) Type: **R** = Read-Only, **R/$\overline{W}$** = Read/Write.
(2) Current Register defaults to '0' because Calibration Register defaults to '0', yielding a zero current value until the Calibration Register is programmed.

Table 2. Summary of Register Set (continued)

POINTER ADDRESS				POWER-ON RESET			
HEX	REGISTER NAME		FUNCTION	BINARY	HEX	TYPE[1]	
10	Bus Under-Voltage Warning		Bus Under-Voltage Warning watchdog register. Sets low voltage warning limit that triggers Status Register flag and activates Warning pin.	00000000 00000000	0000	R/W	—
11	Power Over-Limit		Power Over-limit watchdog register. Sets over-limit power limit that triggers Status Register flag and activates the Overlimit pin.	00000000 00000000	0000	R/W	—
12	Bus Over-Voltage Over-Limit		Bus Over-limit watchdog register. Sets an over-voltage limit that triggers Status Register over-limit flag and activates the Overlimit pin. Also contains Overlimit pin polarity bits and latch feature.	00000000 00000000	0000	R/W	—
13	Bus Under-Voltage Over-Limit		Bus Over-limit watchdog register. Sets an under-voltage over-limit that triggers Status Register flag and activates the Overlimit pin.	00000000 00000000	0000	R/W	—
14	Critical DAC+ Register (Critical Positive Shunt Voltage)		Sets positive Critical internal limit. Contains DAC+. GPIO bits status pin. Critical operation mode; Comparator latch feature and hysteresis.	00000000 00000000	0000	R/W	—
15	Critical DAC– Register (Critical Negative Shunt Voltage)		Sets negative Critical internal limit. Contains DAC–. Warning pin bits; Critical Comparator output delay, configuration.	00000000 00000000	0000	R/W	—
16	Calibration		Sets full-scale range and LSB current and power measurement. Overall system calibration.	00000000 00000000	0000	R/W	—

REGISTER DETAILS

All INA209 registers are 16-bit registers. 16-bit register data are sent in two 8-bit bytes via the I2C interface.

Configuration Register 00h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	BRNG	PG1	PG0	BADC4	BADC3	BADC2	BADC1	SADC4	SADC3	SADC2	SADC1	MODE3	MODE2	MODE1
POR VALUE	0	0	1	1	1	0	0	1	1	0	0	1	1	1	1	1

Bit Descriptions

RST: Reset Bit

Bit 15 Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values; this bit self-clears.

BRNG: Bus Voltage Range

Bit 13 0 = 16V FSR
1 = 32V FSR (default value)

PG: PGA (Shunt Voltage Only)

Bits 11, 12 Sets PGA gain and range. Note that the PGA defaults to ÷8 (320mV range). Table 3 shows the gain and range for the various PG settings.

Table 3. PG Bit Settings[1]

PG1	PG0	GAIN	RANGE
0	0	1	±40mV
0	1	÷2	±80mV
1	0	÷4	±160mV
1	1	÷8	±320mV

(1) Shaded values are default.

BADC: BADC Bus ADC Resolution/Averaging

Bits 7–10 These bits adjust the Bus ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Bus Voltage Register (04h).

SADC: Shunt ADC Resolution/Averaging

Bits 6–3 These bits adjust the Shunt ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Shunt Voltage Register (03h). BADC (Bus) and SADC (Shunt) ADC resolution/averaging and conversion time settings are shown in Table 4.

Table 4. ADC Settings[1]

ADC4	ADC3	ADC2	ADC1	MODE/SAMPLES	CONVERSION TIME
0	X[2]	0	0	9-bit	84 μs
0	X[2]	0	1	10-bit	148 μs
0	X[2]	1	0	11-bit	276 μs
0	X[2]	1	1	12-bit	532 μs
1	0	0	0	12-bit	532 μs
1	0	0	1	2	1.06ms
1	0	1	0	4	2.13ms
1	0	1	1	8	4.26ms
1	1	0	0	16	8.51ms
1	1	0	1	32	17.02ms
1	1	1	0	64	34.05ms
1	1	1	1	128	68.10ms

(1) Shaded values are default.
(2) X = Don't care.

MODE: Operating Mode

Bits 2–0 Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in Table 5.

Table 5. Mode Settings[1]

MODE3	MODE2	MODE1	MODE
0	0	0	Power-Down
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	ADC Off (disabled)
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

(1) Shaded values are default.

Status Register 01h (Read)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	WOV	WUV	WP	WS+	WS–	OLOV	OLUV	OLP	CRIT+	CRIT–	CNVR	SMBA	OVF	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Status Register flags are activated whenever any limit is violated and the corresponding latch bits are set. These flags are cleared when the Status Register is read (unless the limit is exceeded when the flag is set; in which case the flag immediately sets again).

After power-up and initial setup, the Status Register should be read once to clear any flags set as a result of power-up values prior to setup.

Bit Descriptions

WOV: Bus Over-Voltage Warning

Bit 15 This bit sets to '1' when the result of the Bus Voltage Register (04h) exceeds the level set in the Bus Over-Voltage Warning Register (0Fh).

WUV: Bus Under-Voltage Warning

Bit 14 This bit sets to '1' when the result of the Bus Voltage Register (04h) is less than the value set in the Bus Under-Voltage Warning Register (10h).

WP: Power Warning

Bit 13 This bit sets to '1' when the value of the Power Register (05h) exceeds the level set in the Power Warning Register (0Eh).

WS+: Shunt+ Voltage Warning

Bit 12 This bit sets to '1' when the value of the Shunt Voltage Register (03h) exceeds the level set in the Shunt Voltage Positive Warning Register (0Ch).

WS–: Shunt– Voltage Warning

Bit 11 This bit sets to '1' when the value of the Shunt Voltage Register (03h) exceeds the level set in the Shunt Voltage Negative Warning Register (0Dh).

OLOV: Bus Over-Voltage Over-Limit

Bit 10 This bit sets to '1' when the result of the Bus Voltage Register (04h) exceeds the level set in the Bus Over-Voltage Over-Limit Register (12h).

OLUV: Bus Under-Voltage Over-Limit

Bit 9 This bit sets to '1' when the result of the Bus Voltage Register (04h) is less than the level set in the Bus Under-Voltage Over-Limit Register (13h).

OLP: Power Over-Limit

Bit 8 This bit sets to '1' when the value of the Power Register (05h) exceeds the level set in the Power Over-Limit Register (11h).

Bit Descriptions (continued)

CRIT+: Critical Shunt Positive Voltage

Bit 7 This bit sets to '1' when the shunt voltage exceeds the positive limit set in the Critical DAC+ Register (14h).

CRIT–: Critical Shunt Negative Voltage

Bit 6 This bit sets to '1' when the shunt voltage exceeds the negative limit set in the Critical DAC– Register (15h).

CNVR: Conversion Ready

Bit 5 Although the data from the last conversion can be read at any time, the INA209 Conversion Ready bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready clears under the following conditions:

1.) Writing to the Configuration Register (except for Power-Down or Disable mode selections).

2.) Reading the Status Register

3.) Triggering a single-shot conversion with the Convert pin.

SMBA: SMBus Alert

Bit 4 Clears reading only Status Register when disabling SMBus Alert function

OVF: Math Overflow

Bit 3 This bit sets to '1' if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be meaningless. Watchdog does not affect outputs.

Mask/Enable SMBus Alert Control Register 02 (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	MWOV	MWUV	MWP	MWS+	MWS−	MOLOV	MOLUV	MOLP	MCRIT+	MCRIT−	MCNVR	—	SMAEN	CREN	OLEN	WREN
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits D15–D5 of the SMBus Alert Mask Register correspond to bits D15 to D5 of the Status Register. Writing a '0' to a bit prevents the Status Register bit from initiating an SMBus Alert. All default values are '0', which masks them from activating SMBus Alert.

Bit Descriptions

MWOV: Mask Over-Voltage Warning

Bit 15 When set to '0', this masks the WOV bit of the Status Register

MWUV: Mask Under-Voltage Warning

Bit 14 When set to '0', this masks the WUV bit of the Status Register

MWP: Mask Power Warning

Bit 13 When set to '0', this masks the WP bit of the Status Register

MWS+: Mask Voltage Positive Shunt Warning

Bit 12 When set to '0', this masks the WS+ bit of the Status Register

MWS−: Mask Voltage Negative Shunt Warning

Bit 11 When set to '0', this masks the WS− bit of the Status Register

MOLOV: Mask Over-Voltage Over-Limit

Bit 10 When set to '0', this masks the OLOV bit of the Status Register

MOLUV: Mask Under-Voltage Over-Limit

Bit 9 When set to '0', this masks the OLUV bit of the Status Register

MOLP: Mask Power Over-Limit

Bit 8 When set to '0', this masks the OLP bit of the Status Register

MCRIT+: Mask Voltage Positive Shunt Critical

Bit 7 When set to '0', this masks the CRIT+ bit of the Status Register

MCRIT−: Mask Voltage Negative Shunt Critical

Bit 6 When set to '0', this masks the CRIT− bit of the Status Register

MCNVR: Mask Conversion Ready

Bit 5 When set to '0', this masks the CNVR bit of the Status Register

SMAEN: SMBus Alert Enable

Bit 3 1 = SMBus Alert Enable
0 = SMBus Alert Disable (default)

CREN: Critical DAC Enable

Bit 2 Enables/disables operation of the Critical output
1 = Enabled
0 = Disabled (default)

OLEN: Over-Limit Enable

Bit 1 Enables/disables operation of the Over-limit output
1 = Enabled
0 = Disabled (default)

Bit Descriptions (continued)

WRNEN: Warning Enable

Bit 6 Enables/disables Warning output operation
1 = Enabled
0 = Disabled (default)

DATA OUTPUT REGISTERS

Shunt Voltage Register 03h (Read-Only)

The Shunt Voltage Register stores the current shunt voltage reading, V_{SHUNT}. Shunt Voltage Register bits are shifted according to the PGA setting selected in the Configuration Register (00h). When multiple sign bits are present, they will all be the same value. Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting the MSB = '1'. Extend the sign to any additional sign bits to form the 16-bit word.

At PGA = /8, full-scale range = ±320mV (decimal = 32000, positive value hex = 7D00, negative value hex = 8300), and LSB = 10μV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SD14_8	SD13_8	SD12_8	SD11_8	SD10_8	SD9_8	SD8_8	SD7_8	SD6_8	SD5_8	SD4_8	SD3_8	SD2_8	SD1_8	SD0_8
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = /4, full-scale range = ±160mV (decimal = 16000, positive value hex = 3E80, negative value hex = C180), and LSB = 10μV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SD13_4	SD12_4	SD11_4	SD10_4	SD9_4	SD8_4	SD7_4	SD6_4	SD5_4	SD4_4	SD3_4	SD2_4	SD1_4	SD0_4
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = /2, full-scale range = ±80mV (decimal = 8000, positive value hex = 1F40, negative value hex = E0C0), and LSB = 10μV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SIGN	SD12_2	SD11_2	SD10_2	SD9_2	SD8_2	SD7_2	SD6_2	SD5_2	SD4_2	SD3_2	SD2_2	SD1_2	SD0_2
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = /1, full-scale range = ±40mV (decimal = 4000, positive value hex = 0FA0, negative value hex = F060), and LSB = 10μV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SIGN	SIGN	SD11_1	SD10_1	SD9_1	SD8_1	SD7_1	SD6_1	SD5_1	SD4_1	SD3_1	SD2_1	SD1_1	SD0_1
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bus Voltage Register 04h (Read-Only)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	0	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Power Register 05h (Read-Only)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

$$\text{Power} = \frac{\text{Current} \times \text{BusVoltage}}{5000}$$

Current/PGA Register 06h (Read-Only)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

$$\text{Current} = \frac{\text{ShuntVoltage} \times \text{CALIBRATION}}{4096}$$

PEAK-HOLD REGISTERS

Note: All peak-hold registers are cleared and reset to POR values by writing a '1' to the respective bit D0.

Shunt Voltage Positive Peak Register 07h (Read/Write)

Mirrors highest voltage reading of the Shunt Voltage Register (03h).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SPP SIGN	SPP14	SPP13	SPP12	SPP11	SPP10	SPP9	SPP8	SPP7	SPP6	SPP5	SPP4	SPP3	SPP2	SPP1	SPP0/RS
POR VALUE	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Shunt Voltage Negative Peak Register 08h (Read/Write)

Mirrors lowest voltage reading (positive or negative) of the Shunt Voltage Register (03h).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SPN SIGN	SPN14	SPN13	SPN12	SPN11	SPN10	SPN9	SPN8	SPN7	SPN6	SPN5	SPN4	SPN3	SPN2	SPN1	SPN0/RS
POR VALUE	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bus Voltage Maximum Peak Register 09h (Read/Write)

Mirrors highest voltage reading of the Bus Voltage Register (04h).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BH12	BH11	BH10	BH9	BH8	BH7	BH6	BH5	BH4	BH3	BH2	BH1	BH0	—	—	BPK/RS
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bus Voltage Minimum Peak Register 0Ah (Read/Write)

Mirrors lowest voltage reading of the Bus Voltage Register (04h).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BL12	BL11	BL10	BL9	BL8	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	—	—	BL/RS
POR VALUE	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

Power Peak Register 0Bh (Read/Write)

Mirrors highest reading of the Power Register (05h).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PPK15	PPK14	PPK13	PPK12	PPK11	PPK10	PPK9	PPK8	PPK7	PPK6	PPK5	PPK4	PPK3	PPK2	PPK1	PPK0/RS
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WATCHDOG REGISTERS — WARNING

These registers set warning limits that trigger flags in the Status Register and activate the Warning pin. **Note:** Delayed output sets in Critical DAC Register (15h).

Shunt Voltage Positive Warning Register 0Ch (Read/Write)

Full-scale range = 320mV, 15-bit + sign, LSB = 10μV (decimal), positive value 32000, 7D00 hex, negative value 8300 hex.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SWP SIGN	SWP14	SWP13	SWP12	SWP11	SWP10	SWP9	SWP8	SWP7	SWP6	SWP5	SWP4	SWP3	SWP2	SWP1	SWP0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

SWP: **Sets positive shunt voltage warning limit.**

Bits 0–15 If the value of the Shunt Voltage Register (01h) exceeds this limit, the SWP bit of the Status Register (01h) is set to '1' and the Warning pin asserts.

Shunt Voltage Negative Warning Register 0Dh (Read/Write)

Full-scale range = 320mV (decimal), positive value 32000, 7D00 hex, negative value 8300 hex, LSB and sign bit 15 = 10 μV

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SWN SIGN	SWN14	SWN13	SWN12	SWN11	SWN10	SWN9	SWN8	SWN7	SWN6	SWN5	SWN4	SWN3	SWN2	SWN1	SWN0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

SWN: **Sets negative shunt voltage warning limit.**

Bits 0–15 If the value of the Shunt Voltage Register (03h) is below this limit, the SWN bit of the Status Register (01h) is set to '1' and the Warning pin asserts.

Power Warning Register 0Eh (Read/Write)

Full-scale range, same as the Power Register.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PW15	PW14	PW13	PW12	PW11	PW10	PW9	PW8	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

PW: **Sets power warning limit.**

Bits 0–15 If the value of the Power Register (05h) exceeds this limit, the PW bit of the Status Register (01h) is set to '1' and the Warning pin asserts.

Bus Over-Voltage Warning Register 0Fh (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BWO12	BWO11	BWO10	BWO9	BWO8	BWO7	BWO6	BWO5	BWO4	BWO3	BWO2	BWO1	BWO0	—	WPL	WNL
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

BWO: Bus Overvoltage Warning limit. Sets overvoltage warning limit.

Bits 15 – 3: If Bus Voltage Register (04h) value exceeds this limit, the WOV bit of Status Register (01h) sets to '1' and the WARNING pin asserts.

WPL: Warning Pin Polarity. Sets the Warning pin polarity.

Bit 1: 1 = Inverted (active-high open collector)
0 = Normal (active-low open collector) (default)

WNL: Warning Pin Latch. Configures the latching feature of the Warning pin.

Bit 0: 1 = Latch enabled
0 = Transparent (default)

Bus Under-Voltage Warning Register 10h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BWU12	BWU11	BWU10	BWU9	BWU8	BWU7	BWU6	BWU5	BWU4	BWU3	BWU2	BWU1	BWU0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

BWU: Sets overvoltage warning limit.

Bits 15 – 3: If Bus Voltage Register (04h) value below this limit, the WUV bit of Status Register (01h) sets to '1' and the WARNING pin asserts.

OVER-LIMIT/CRITICAL WATCHDOG REGISTERS

These registers set the over-limit and critical DAC limits that trigger flags to be set in the Status Register and activate the Overlimit pin or Critical pin.

Power Over-Limit Register 11h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PO15	PO14	PO13	PO12	PO11	PO10	PO9	PO8	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

PO: Sets the power over-limit value.

Bits 15 – 0 If the Power Register (03h) value exceeds this limit, the POL bit of the Status Register sets; if the OLENPOL bit is set in the Overlimit/Critical Register (01h), the Overlimit pin asserts.

Bus Over-Voltage Over-Limit Register 12h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BOO12	BOO11	BOO10	BOO9	BOO8	BOO7	BOO6	BOO5	BOO4	BOO3	BOO2	BOO1	BOO0	—	OLP	OLL
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

BOO: Sets the bus overvoltage over-limit value.

Bits 15 – 3 If the Bus Voltage Register (04h) value exceeds this limit, the BOL bit of the Status Register sets; if the OLENBOL bit is set in the Overlimit/Critical Register (01h), the Overlimit pin asserts.

OLP: Overlimit Polarity sets the Overlimit pin polarity.

Bit 1 1 = Inverted (asserts high)
0 = Normal (asserts low) (default)

OLL: Overlimit Latch configures the latching feature of the Overlimit pin.

Bit 0 1 = Latch enabled
0 = Transparent (default)

Bus Under-Voltage Over-Limit Register 13h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BUO12	BUO11	BUO10	BUO9	BUO8	BUO7	BUO6	BUO5	BUO4	BUO3	BUO2	BUO1	BUO0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

BUO: Sets the bus undervoltage over-limit value.

Bits 15 – 3 If the Bus Voltage Register (04h) value is below this limit, the BUL bit of the Status Register sets; if the OLENBUL bit is set in the Overlimit/Critical Register (01h), the Overlimit pin asserts.

Critical DAC+ Register (Critical Shunt Positive Voltage) 14h (Read/Write)

8-bit. 1mV LSB; 255mV range; full scale (positive only) limit; sign bit (sets positive) No

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CDP7	CDP6	CDP5	CDP4	CDP3	CDP2	CDP1	CDP0	GP	GPM1	GPM0	CP	CHYST2	CHYST1	CHYST0	CRL
POR VALUE	0	0	0	0	0	0	0	0	(1)	0	0	0	0	1	1	0

(1) POR value reflects the state of GPIO pin.

Bit Descriptions

CDP: Critical DAC+ limit setting

Bits 8–15

GP: GPIO readback

Bit 7 Shows state of GPIO pin.

GPM: GPIO mode bit.

Bits 5, 6 The GPIO mode settings are shown in Table 6.

Table 6. GPIO Mode Settings(1)

GPM1	GPM0	STATE	NOTES
0	0	Hi-Z	Use either of these modes as input.
0	1	Hi-Z	
1	0	0	
1	1	1	

(1) Shaded values are default.

CP: Configures Critical output polarity (open-drain output).

Bit 4 1 = Active high
0 = Active low (default)

CHYST: Configures Critical comparator hysteresis.

Bits 1–3 The CHYST settings are shown in Table 7.

Table 7. CHYST Settings(1)

CHYST2	CHYST1	CHYST0	HYSTERESIS
0	0	0	0mV
0	0	1	2mV
0	1	0	4mV
0	1	1	6mV
1	0	0	8mV
1	0	1	10mV
1	1	0	12mV
1	1	1	14mV

(1) Shaded values are default.

CRL: Configures Critical pin latch feature

Bit 0 1 = Latch enabled
0 = Transparent (default)

Critical DAC– Register (Critical Shunt Negative Voltage) 15h (Read/Write)

8-bit, 1mV/LSB; 255mV range; full-scale (negative only) limit; no sign bit

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CDP7	CDP6	CDP5	CDP4	CDP3	CDP2	CDP1	CDP0	CF3	CF2	CF1	CF0	WD3	WD2	WD1	WD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

CDP: Critical DAC- limit setting

Bits 8–15

CF: Configures Comparator output filter.

Bits 4–7 Ranges from 0 to 0.960ms; 64µs/LSB. CF settings are listed in Table 8.

WD: Configures Warning Output Delay from 0 to 1 second/LSB

Bits 0–3 Default setting = 0. WD settings are listed in Table 9.

Table 8. CF Settings

CF3	CF2	CF1	CF0	FILTER SETTING (ms)
0	0	0	0	0
0	0	0	1	0.064
0	0	1	0	0.128
0	0	1	1	0.192
0	1	0	0	0.256
0	1	0	1	0.320
0	1	1	0	0.384
0	1	1	1	0.448
1	0	0	0	0.512
1	0	0	1	0.576
1	0	1	0	0.640
1	0	1	1	0.704
1	1	0	0	0.768
1	1	0	1	0.832
1	1	1	0	0.896
1	1	1	1	0.960

Table 9. WD Settings

WD3	WD2	WD1	WD0	DELAY SETTING
0	0	0	0	0
0	0	0	1	0.1
0	0	1	0	0.2
0	0	1	1	0.3
0	1	0	0	0.4
0	1	0	1	0.5
0	1	1	0	0.6
0	1	1	1	0.7
1	0	0	0	0.8
1	0	0	1	0.9
1	0	1	0	1.0
1	0	1	1	1.1
1	1	0	0	1.2
1	1	0	1	1.3
1	1	1	0	1.4
1	1	1	1	1.5

Calibration Register 16h (Read/Write)

Current and power calibration are set by bits D15 to D1 of the Calibration Register. Note that bit D0 is not used in the calculation. This register sets the current that corresponds to a full-scale drop across the shunt. Full-scale range and the LSB of the current and power measurement depend on the value entered in this register. See the Programming the INA209 Power Measurement Engine section. This register is suitable for use in overall system calibration. Note that the POR values are all default.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (1)
BIT NAME	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0	FRB
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) D0 is a void bit and is always '0'. It is not possible to write a 1 to D0. CALIBRATION is the value stored in D15:D1.

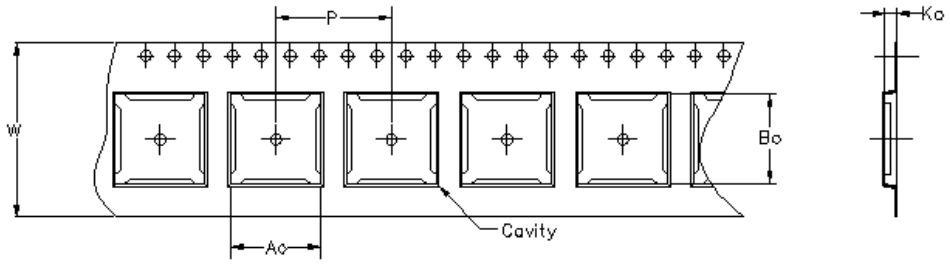
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
INA209AIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
INA209AIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

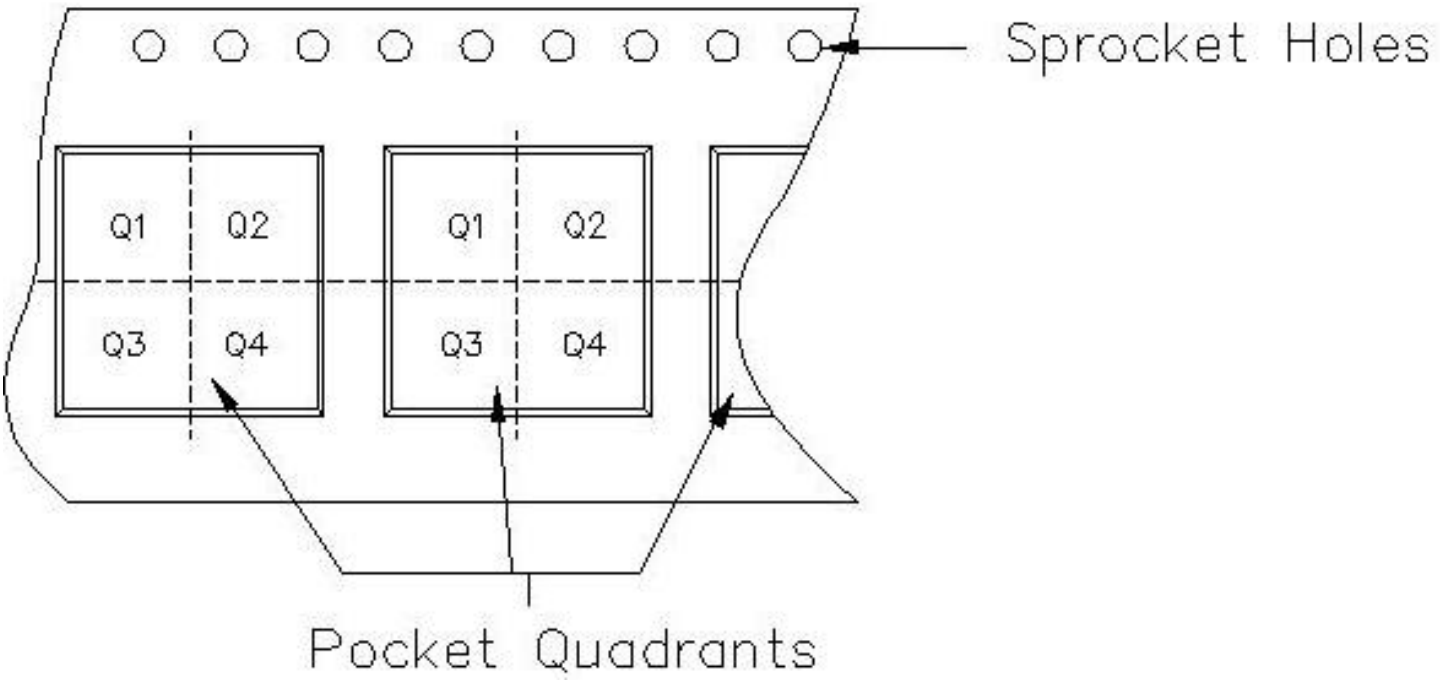
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



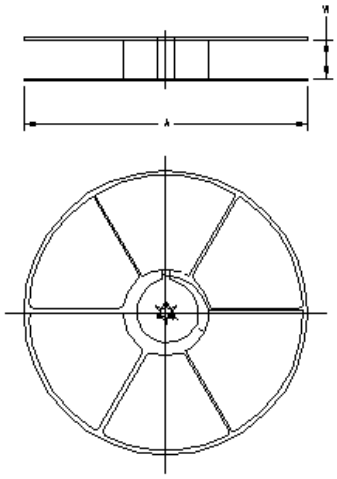
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



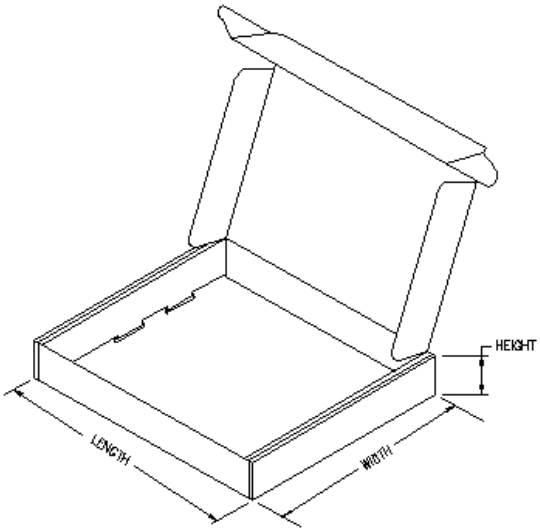
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA209AIPWR	PW	16	MLA	330	12	7.0	5.6	1.6	8	12	Q1



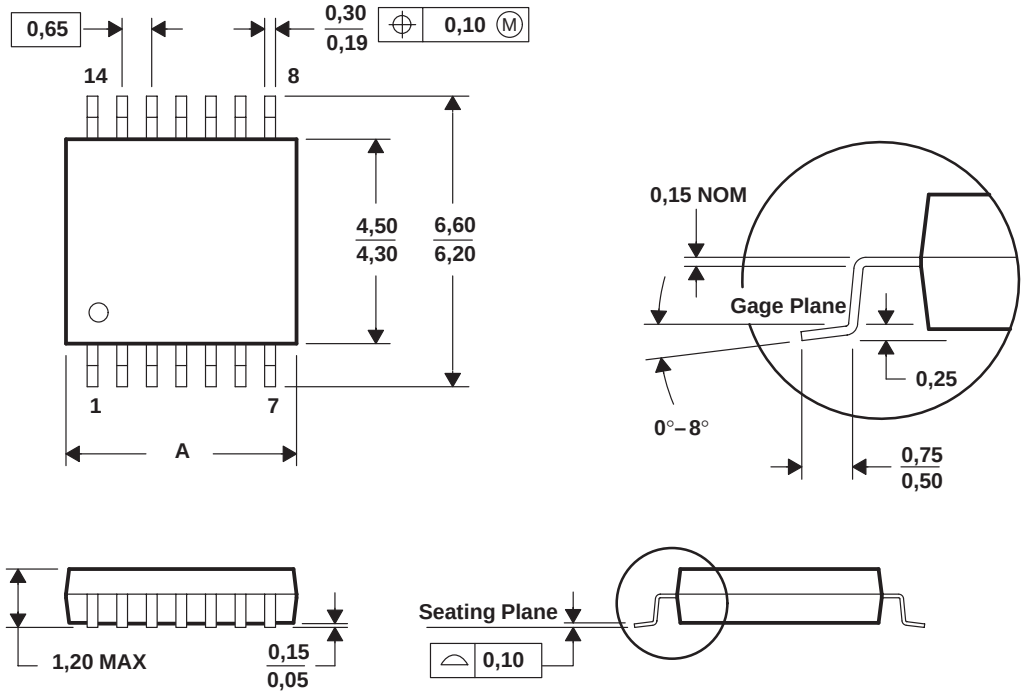
TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
INA209AIPWR	PW	16	MLA	346.0	346.0	29.0



PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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