



# **INA209**

**SBOS403** 2007 JUNE

with

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The

lower

delay.

system

monitorsINA209e

readoutsdirect

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# Monitor

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monfitoring useisul

assists

# Current/PowerBi-Directional Measuremetigh-Side Intel tace with

# FEATURE

# DESCRIPTION

VOLTENDESS SENISES FROM **VOLTAGE, CURRENT, REPORTS** PEAKS STORES POWER: WATCHDOBBLE LIMITS: Warningower Delawith Over-libhotoper Delato Critical Analogist :YISONRICCURRECTY:

**APPLICATIONS** 

V<sub>S</sub> (Supply Voltage)

Q

ç

Convert

Critical

Filte

DAC

Critical

Overlimit Register Warning Register

Power Register

Current Registe

Voltage Register

SERVERS EQUIPMENTELECOM **AUTOMOTIVE** MANAGEROGENER **CHARGERBATTERY** EQUIPMENWELDING SUPPLIESOWER EQUIPMEENT

V.

+26**V**O0V INA20Be poweamd shunt current high-isside intefacedtiw rotinom AND shunt both shunt and drop programmable calibration multiplier, internal amperes. multiplyingaddAtional features INA2008e waltts. power capabilities: watchdog onboard comparatorover-ainnit and comparator **TEMP OVERMAX%** comparatomarning user-defined incompatients warning comparatoover-IIThit immediatequirecouldthat limits upper

shutdown. INA2099he anal compto-digital includes so proagramamelble converter compar (Add) C) digital-to-analog converter (DAC) comb**iha**t ot responsespossiblefastekte provide curtent conditionsoverload

enables

INA2079ae togethesede can swaphot with controllers alreatolwat resistorsense cuarentuse full-scaleNA208e selettedcan range be to controller hot-shareap within either limits, sense າດ enouowhide them. indude

shunts across senses INA2019e can that buseers +3V sinagle uses devicTehe 26th 0V from vary -O Critical maaximum drawing supply,+5.560V 1.5 of A of speisifiled current. supply operfabilion from +850 C 25 .D

application and use and Please warranty, standard availability, concerniotige awaboee impeontathat Teøfas semiconductorstructors products appearsthereto disclainders endthæt sheetdatathis f SemitAbXotelluctors. trasdeismat/LC

-O Overlimi

-O Warning

-O Aler

-O Data

-O CLK

1<sup>2</sup>C

Interface

GPIO

tradero tar texts prophet/vare respetibitisti owners.



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han**ble**d

proceduresinstaallation handlingroper obtoerve Failure precautions.appropriate damageausean degradation performantatter from rangean dama**£6**2 susceptible controplete integrated Precisiofailure. device because dantage parametriall very changes cause could devi**th**e

circuits be may publtshed meto not

circuits

intealitatetdat

specifications.

#### ORDERING INFORMATION

	EAD PRODUCT	PACKAGE-LI	KAGE	DESIGNAT <b>OR</b> C	RKING PACKAGE	MAF
	INA209	TSSOP-16		PW	INA209A	
(1)	packagecurremtosthe For	informatiom de ain g	Packhaegesee	Addend <b>0pt</b> ion	docu <b>thie</b> fnt, endthæt	TI the seer

wwatv.tissitemweb

# **ABSOLUTE MAXIMUM RATING®**

circuit

temperafteteeair opera@wger otherwis(enlessange noted).

	INA209	τινυ
<sub>S</sub> V Voltage\$upply	6	V
<sup>(3)</sup> _ <sub>IN</sub> (V–) <sub>IN∔</sub> (V Differential Inputs, Analog	+260 26	V
Common-Modely, INY	+260 0:3	V
Output&igital Open-Drain	+6to 0.3 GND	V
Pins ConvertBPIO,	0.3 <sub>S</sub> V to 0.3 GND	V
Pin Any Into Currefriput	5	Am
CurrentOutputDigital Open-Drain	10	Am
Temperatu®perating	+1255 40	ಲ
Tempera	+1500 40	ಲ
Temperaturection	+150	ಲ
ModeBody Human	2000	V
Model Charged-Devideatin	1000	V
(MM) Model Machine	150	V

Stres(ste)s Exposuredamage. permaroautsenay ratingsthese above conditions maximumab tool ute periods exteorded may These reliabilityevice degrade ratingsstressee operation functional only, devitoreeof theaste condition hean or beyond specifitendose implineatits

differentialvemay<sub>N</sub>V and<sub>N</sub> $\chi$  (2) voltage however260V; 26Vof voltabgee excened mustpins theate 0<del>.</del>3V ran**gb**e to +26V.

SBOS403 2007 JUNE

#### CHARACTERISTEDSTRIC.

#### +3<del>,</del>3₩ temperatu**spectific**edover apply limits ا - سرز V = ديلارد 124 سري 3 + 25 T tA **C. +85oC 25 = <sub>A</sub>T** range, <sup>1)</sup> BRNa®nd,÷ = PGA 32an≬V<sub>M</sub>V-Boldface

				e	INA209		
	PARAMETER		CONDITIENIS	МІМ	ЧҮТ	ХАМ	тиυ
тирит							
Full-Scale	ange Voltage(Input) Sense Current	Я	1 ÷ = PGA	0		4⊕	M
			2 ÷ = PGA	0		⊕8	Vm
			4 ÷ = PGA	0		160	M
			8 ÷ = PGA	0		3 <b>≇</b> 0	Vm
ta Boos	(2) Range Voltage()put Vol		1 = BRNG	0		32	V
			0 = BRNG	0		16	V
Common-Mo	Rejection	CMRR	26¥o6 0\≟ IN¥	100	120		dB
geoffset	<sup>(3)</sup> RTI Volta	Véo	1 ÷ = PGA		1⊕	1⊕0	Vµ
			2 ÷ = PGA		2⊕	1 <del>2</del> 5	Vμ
			4 ÷ = PGA		3⊕	150	Vµ
			8 ÷ = PGA		4 <del>0</del>	2⊕0	Vμ
ature	Ter <b>n</b> per				0.1		∆v ⊃
	SupplyPowser	РЗКК	5.51oV 3V⊭ <sub>S</sub> V		10		VAV
Current	Error Gain Sense				4⊕		%m
ature	Termaper				10		s ppm/
edapote	Impe		Mode Active				
	γ <sub>INN</sub>				20		Αμ
	Pininy				3 <b>2</b> p 20		k∥Aμ
a <b>lge</b> ut		wn	Mode Power-Do				
	Pin <sub>IN</sub> Y				0.1	0±5	Ąц
	Pin <sub>IN</sub> V				0.1	0±5	Aµ
YOARD	A						
CADC	Resolution				12		Bits
88.	Size Step1						
	Voltagehun				10		Vμ
	VoltaBojes				4		Vm
reChuereint	Error Measu				0±2	0±5	%
	Tempævet					1±	%
	Error Measure <b>vin</b> et				0±2	0±5	%
ราเ	Tempævet					1±	%
tyDifferential	•				1±0		LSB
-	Range Full-SDAIG				255		Vm
Critical	Accuration				0#2	1±	%
Critical	Resolution				8		Bits
Critical	Size Step LSB DAC				1		Vm
	Offset Comp <b>a</b> Actor				0 <u>±</u> 3	1±6	Vm
	<sup>(4)</sup> Hysteresis Comp <b>BA</b> C				(4) See		
	Delay Comp <b>a</b> Actor				5		sμ

s BRNQI) parar**fibite**r(2) Refer(@)d-to-input User (ali)ogrammable.

expresses full-stoale .(ІТЯ) Comparation See

sections. Regiater

scalingb@heof

range

appliced 26V than more should eventual In

devi**teis**o



#### CHARACTERISTEDSTRIC.

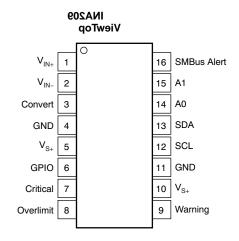
# (contin**u3e3W**

**C.** +850C 25 =  $_{A}T$  range, temperatuspectificedover apply limits Boldface noted. otherwiselts BRN kend,  $\dot{e} = PGA 32$  moted.  $S_{R}$  (V=  $_{SE}V_{SE} 12V$ ,  $_{IN}V$  C, +25 $_{A}T$  At

			60	INA2		
	PARAMETER	CONDITIENS	ИІМ	ΤΥΡ	ХАМ	тиυ
COC	ИІМІТ					
<b>ArBiG</b> n	Time Conve	12-Bit		532	586	sμ
		11-Bit		276	304	sµ
		10-Bit		148	163	sμ
		9-Bit		84	93	sμ
Minimum	TimeLow Input Convert I		4			sµ
SMBus	2					
SMBus	<sup>(5)</sup> Timeout			28	35	ms
DIGITAL (Convert,	INPUTS I A1)A0,SCL, Inpases, SDAand GPIO					
bitpate	Leakage Capad			3		ΡF
<b>ht</b> put	Currel	$V \leq IN > 0$		0.1	1	Aµ
Input	Levelstogic					
	V <sub>HI</sub>		) <sub>S</sub> (V 0.7		9	V
	V_II		<del>0.3</del>		) <sub>S</sub> (V 0.3	V
Hysteresis	1			500		M
DIGITAL	OUTPUT					
GPIO	Low OutpRint (	ЗпеА ынк		0.15	0.4	V
GPIO	High OutpRint (	3mA JOURCE	0.4 <sub>S</sub> V	0.45 V		V
OPEN-DRAIN (Critical,	OUTPUTSDIGITAL ( SDA) Alert, Warning, Over-Lim					
Logic	Level Outpout	3m=A JINK		0.15	0.4	V
High-Level	1 0	s V = OH		0.1	1	Aμ
РОМЕК	SUPPLYI					
Operating	Range Supply 0		+3		+5.5	V
Quiescent	Current (			1	1.5	Am
Quiescent	Mode Power-D <b>©wrr</b> ent, (			9	15	Αμ
Power-On	Thresholdestet			2		V
ТЕМРЕКАТИ	RANGE					
<b>Spe</b> cified	Range Temperat		25		+85	ວ
Corperating	Range Temperatu		40		+125	ວ
denermal	Resistand	Qu				
P-16	TSSOF			+150		C/W

28msoveftor lovics SCL timeany intertrace resets INA21049 timeout SMB(63)

# **PIN CONFIGURATIONS**

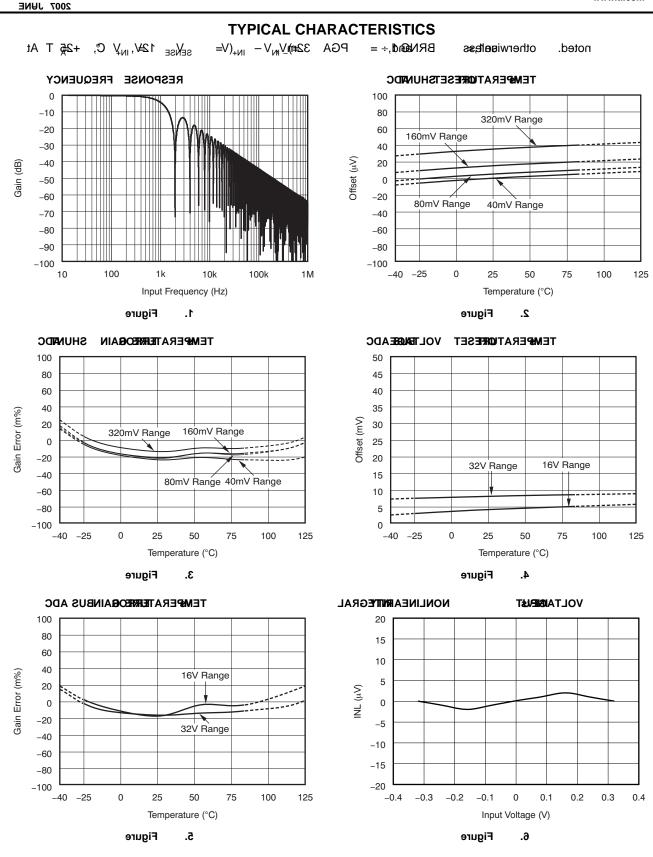


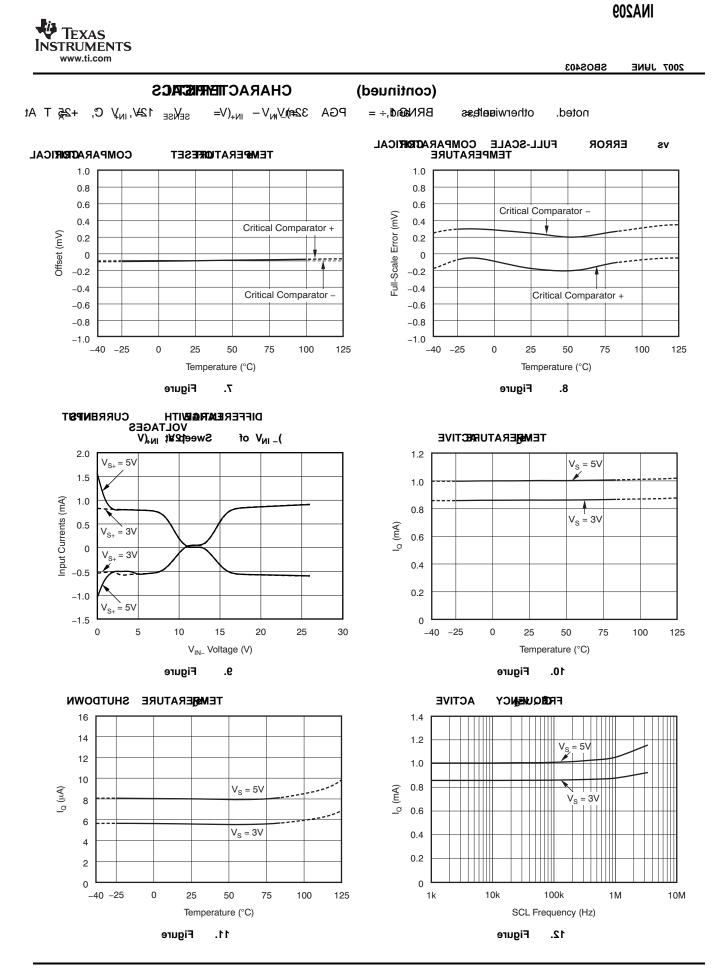
# DESCRIPTIONS

NO. PIN	3	DESCRIPTIONAME
1		resisto <b>shon</b> ft side po <b>tsit</b> ive Connectvoltagehunt differenti®bsitive <sub>IN</sub> ¥
2		is volta <b>Be</b> s resisto <b>shou</b> ht side netgative Connectvoltagehunt differentiaNegative_INV grotounophin this from measured
3	ert	and higbbe normallshopld this mode, triggered mode. triggered conversitigger Used Conve each convexto?Che low, helfdsµ4 after high retubreedmeby conversitionatelow taken hightiedbe shoulide this usedudt buo81 the via writsten commannade triggerename
4		ground:1 pin with together Connect GND
5		5.5tW. 3V suppoly1,0 pin with together Connect <sub>S4</sub> V
9		if supply ground Connecbutput. Totem-pole input/output. user-programmableeneral-purpeBebQ input/output asis conditioDefaultseendot
7	le	di <b>sa</b> bled; conditioDefault Regist <b>@)</b> AC Criticastet (filter output watchdogitical Open-drain Critica (non-latched)ansparentactive-low;
8	limit	transparentactive-low <b>disa</b> bled; conditio <b>D</b> efault output. watchdogover-limit Open-drain Over (non-latched).
6	ing	is conditioDefault Registውእር Criticaset (delay output watchdogvarning open-drain Warr (non-latched)ansparentactive-lowdisabled;
10		5.5tol. 3V supposed, pin with together Connect <sub>S4</sub> V
11		grda#d. pin with together Connect GND
12		line. cloclbus Serial SCL
13		line. databus Serial SDA
14		addresses. correaspubndingsettipigs shows Tablpin. Address A0
15		addresses. correaspubndingsettipigs shows Tablpin. Address A1
16	lBus	disiabled. Default RegistikalaskAlert SNinBus Controllectipuatert SMBus Open-drakinert SN

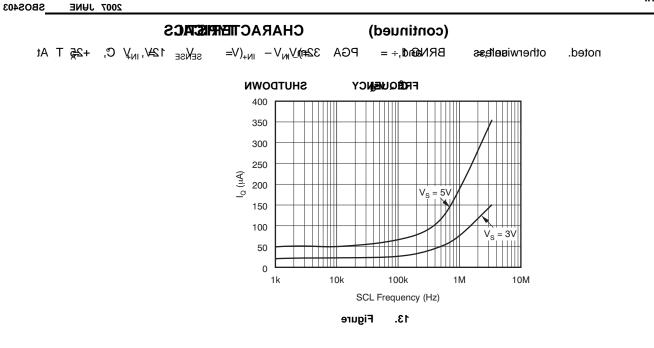
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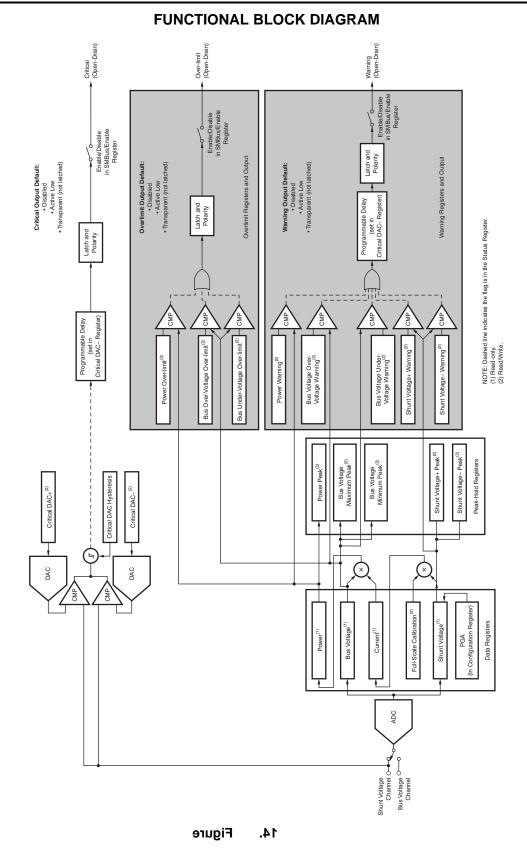












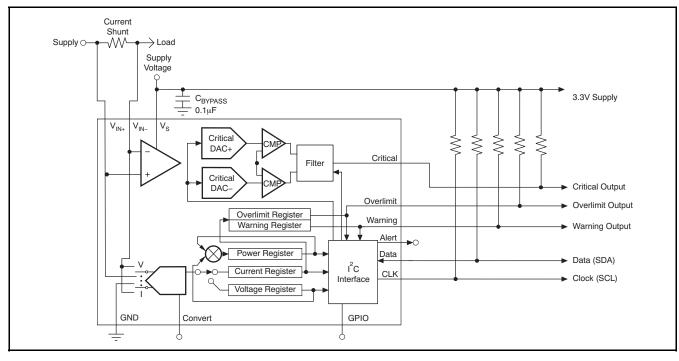
#### INFORMATIONAPPLICATION

INA270199e curren telszani tatelt monitor an with additess device, spacific initiates masthe 6 SMBuandom patible interface. prolytides conditionSTART gdilluq signaldata the line voltage, current, digital readings power and HI&H from (SDA) SCL while level logic LOWto necessary decision-makirgurater HIGH. slavAB shift bus the on slavehein in precisely-cor Programmablesystems. address edge risintelyeon byte last the with SColf, registers configuratiexible allow settinfgr whether indibiatting reaad operativonitoer si resolution, During warning measurehimeitts, intended. and pulse, clock ninththe slavehe operation. continuous-v Detailed address**bee**ing responds mastehe to by informaticentister appears Ackenowledge generatingdatathisof end theat LOW.SDA pullinagend beginnisgeet, Tablewith FundhenaSe@ transf@ata initiat etetebas dataf bits eightand **Diagrathock** diagraboha ckfor INA 27029f followedent.are Ackanowbadge Duribog. The INA209 offers compatability with Deug MZ transfebata SCL while stable remaimust SDA si

protocols SMBuandCl HIGH. interfaces. The chang <del>ke</del>ny SCL while SDiA Hadih si are interpretetet will other. each with SPARES condition TOP compatible essentially through set SMBweith docu**thnie**nt, being Once transfebreegh have dataall mastelle generates lines between differencewhenonly specified indicated conditio6,TDP pullibng addresseistig lines, systems bi-dir**€otio**nal HIGH. SCL while HIGH LOW from SDA The conneStDAand SCL eons and Both bus.theto includes INA209 timeou 28 ans inteitfacen to connectionsopeandrais DAand SCL Figure 15 locking prevent SManusup applicativenical shows circuit.

### **BUS OVERVIEW**

device the initiatersat transtiteet calli**s**d а controlledevittees and master mastiteetby are contbelled mustbus The massterby slaves genetrates device controls(SCL)clock seriathe STOBnd accebsis the geneaanteles START conditions.



Circuit ApplicatTyptcal Figure

next The

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The byte.data eaolh

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#### **SBOS403** 2007 JUNE

WRITING TO/READING FROM THE INA209

addressabid of

pointer registiteer

register. The next two bytes are written to

gentesyrating transferenta

by

pointer registher

pointer. register by

duringreats

condition START

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HIGHH WR/ the with byte

significazostheis

pointer. registreerby

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add**teas** 

#### Serial Bus Address

event.

com mounicate INA 21009. with masthe Accessing must register paralicular INA 2009 on si addreiesset devicesslave addressave via accomplisheede. app**tbp**riatewritinyg value theto addressaaveThe consistate addressevenfin Refer pointer. register Tabbe coanplicete list directionand bits, indicating intenthe correspondingregoisters of addresses. valueThe pointer registherfor executing read operativoitoe shoawan Figare theis 19 trans bevotes for the states of the states o addressavtene after with byte The INA209 has two address pins, A0 and A1. the R/W bit LOW. Every write operation to the requiresINA209 theof describestable levelstogippin the eactor vaalue pointer. regitterfor addressepos\$60le stateThe A1 and A0 pinsf shoutedhd Writing byte first the with saimspled combausaicaeticeevy begins regesteto befoset be activitation transmitted occurs. interfaeon mastelene by byte This slaveheis The address pins are read at the start of each address, with the R/W bit LOW. The INA209 then

acknowledges

transbritted

receipt

Ackanovbledge follisswedbyte This

acknowlerdageesine byte.

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followeldOW/twit WR/ the with byte

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communicati

Table	AddressNA209	and Pins	æn.will data wh <b>ich</b> register
	Addre Stare		jis <b>titee</b> updatessalue address
A1	0A	ADDRESS	register. The next
GND	GND	100000	teerby addresseretgistteer receipt acknowletde <u>β</u> a€9
GND	V <sub>+8</sub>	1000001	ansfeteata termi <b>nate</b> maste <u>r</u>
GND	SDA	1000010	conditionTOP START
GND	SCL	1000011	INA21029, from reading/vhen
V <sub>48</sub>	GND	1000100	y pointer registere in
V48	V <sub>48</sub>	1000101	registerwhich determines
V <sub>+2</sub>	SDA	1000110	regishter chantge operation.
V <sub>+2</sub>	SCL	1000111	an must valueneaw opera <del>tion,</del> coincreatiente≣bie coincter
SDA	GND	1001000	acisomp <b>listte</b> dThis pointe <mark>r.                                    </mark>
SDA	V <sub>+2</sub>	1001001	add <b>kto</b> nabyte. pointer register
SDA	SDA	1001010	.RT genertantens masterhe
SDA	SCL	1001011	n byte addresskavtene sends
SCL	GND	1001100	commensed the initiate
SCL	V <sub>+2</sub>	1001101	and slaveneby transmitted indicated egishteof byte
SCL	SDA	1001110	kanovbryedge follisswedbyte This
SCL	SCL	1001111	transmalavene then master;

#### Serial Interface

terminatev masterne byte. transf**e**ata by Noat-Acknowledgeenerating receiviation any operatesINA20Be deviceslaave as only theon genemating byte, data START STOR Connection Manual busel condition are bus theto repteated registessamtene from reads opethelivaian The SCLand SDA lines/O made desizere. necensatarit conttinually send SDA SCL and integratedeaturpins spike bytes; pointer registiteer retains INA2109 the mintiomize triggers Schmaittd filters suppression chashinged until value pointer register nexttheby spikesinputf noisebus and The effectbe operativoite transhession supportsINA209

protocol fastfor Figure Figurand 16 write and read show 7 4000kHz) (1kHz high-**ape**led 3.44601Hz) (1kHz operation most bytes registhat Note diagrantisming transmitted bytes data All modes. most-segntialiteant followferest, byte the by significant first. byte significeanst Figurebyte. showis timintope diagram SMBtbs for operat Adean: Figure 19 illustrates configuration ter registerty paical

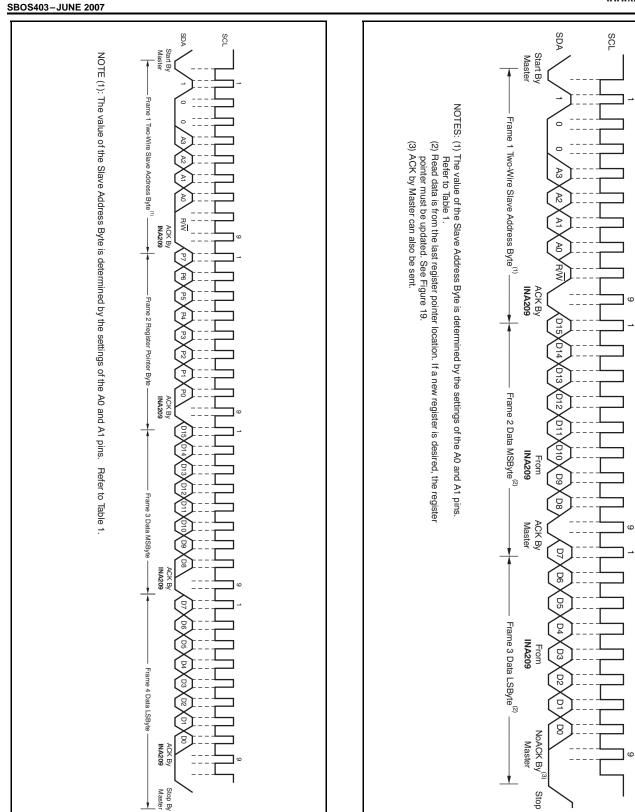
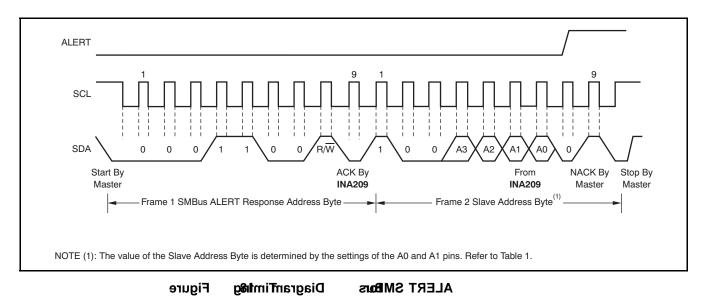
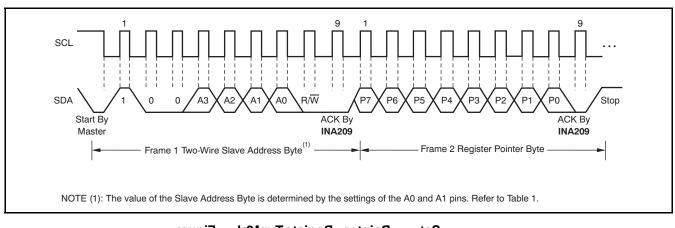


Figure 16. Timing Diagram for Write Word Format

Figure 17. Timing Diagram for Read Word Format



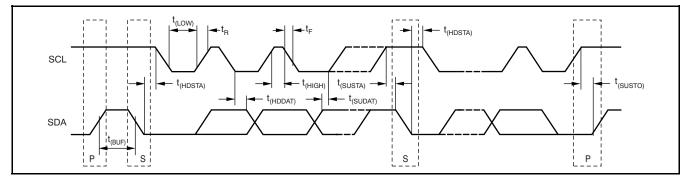




Set Pointer RegisterTypleal Figure

High-Speed I<sup>2</sup>C Mode Instead allowed. usiot repeated condisticant condisitants should sectoure uselode bus the in HS-mode. lines SCL and SDAthe both idles When bus the condistor HS-threade ends and devices pull-the by high pulleatre mast**e**he switches intertdrade all filters INA 20092 of to followed condistant serialvaalid by generates either transmisseiten/S support High-Speed contain bity tep master(HS) code

00001XXX transmītsteison made fastin mastelne genethers reaeated condistant (400kbps) (100kbps)standard mode (F/S) no at condititant rep(eaated timing samthe has as more 400kbptshan INA209The does not conditiettart the After repeat bits start acknowledge masterIS the code, does but condition, protobel sametheis mod€;/Sas recognize switcelmetes support filters inteitsnal transtmistsionexcept speeds 3.44104 bps are operation3.4Mbps Instead allowed. repeated condisticant usiot mastēhe genetheens reaeted condistant condistants should sectorre uselode bus the in rep(eaated condititant timing samthe has HS-modes condititon HS-threade ends and repeat**bits** conditiettant the After switches start interthate all filters INA 20092 of to mod€;/Sas mode/S the condition, protobel sametheis support transtmistsionexcept speeds 3.44104 bps are



DiagranTimitBgu20. Figure

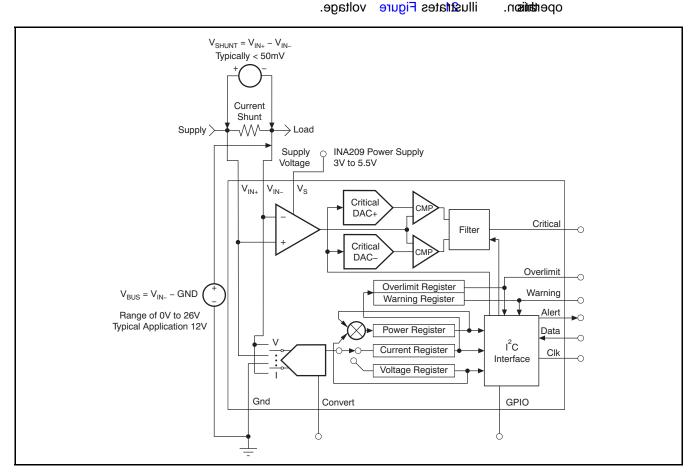
		DEFAST	EED MOI	нен-зр	MODE HIGI		
PARAMETER		ΜΑΧ ΜΙΝ		ИІМ	ХАМ	υΝΙΤS	
FrequencyOper <b>\$</b> @lg	(ŚCL)	0.001	0.4	0.001	3.4	MHz	
STARATId STOP Betwensime FreeBus Condition	(ヨリ <b></b> 雄)	600		160		ns	
condition&TART repeadatedrtimeHold geiaserateddockirstthe periolodicaAfter	( <b>H</b> DSTA)	100		100		ns	
Time Setup Conditio8TART Repeated	(SUSTA)	100		100		ns	
Time Setup Conditi <b>8</b> nTOP	(SUSTO)	100		100		ns	
Time Hold Data	( <b>H</b> DDAT)	0		0		ns	
Time SetupData	(BUDAT)	100		10		ns	
Period_OW ClockSCL	( <b>t</b> ow)	1300		160		ns	
PeriodHIGH ClockSCL	( <b>H</b> IIGH)	600		60		ns	
TimeFall Clock/Date	ц		300		160	ns	
TimeRise Clock/Date	я		300		160	ns	
1000kHz SC <b>tok</b> TimeRise Clock/Dat	<b></b> 与		1000			ns	

#### DefinitionBaiagramTiminBogus

#### **Power-Up Conditions**

## BASIC ADC FUNCTIONS

conditions Power-up software apply reset the via inputs analtogo The O BO B ANI and V V<sub>NI -</sub>, Configuration) (bitbit RST Register, connect theor resistosrhauntto interfestbus thein The Genebrate Resectall power devAde INA209 all up, powered typisally separatity supply Status Over-Limit/Varning, mastured bits Critical, +5.15V. +3V from sensedbeindous The vary can disableatet conside satisfations are SMBuand function Adert IΙΑ There26to 0V from watchdog outputs default active powfear-supply and low sequencing exam(fole, Bng (non-latched) ansparent modes. voltage pressent can voltage supplice with off, vice-aetaa). senses INA2009e drop smathe across shunthe voltages,hufter sensead the voltage respeweitth gratond bus the for  $I_{N}V$ from





Configulted 209 Figure



SBOS403 2007 JUNE

> When INA 2600 operatingornthadein is mode Conve**rbie**n Ready these under clearbait MOSE (that Register Confirentation conditionscre

shunthe set conttinuoush/1to, converts numbreato up voltage voltageshurthein set Register, (Configuration averaging SADC convelntesn devictene bits). voltaboges the to up numt**te**e set averagingvoltagetus the in Register, (Configuratio ModeThe bits). BADC control Confibreination Register permittalso selecting contoert modes voltagoenly curcent. continue utbler respinonscer evenatin to (triggered).

currelint calculation was md perfamme backtgeound conversion continibute and conversione; shown times Electthmain detterminerseble can table Characteristi the time. converaittaal

Power-Down reducesnode quiestorent current avoiding nputs, INA 2009 into curcefnt turnsand drain. suppleyny Powefr Down recoverty ADGu 40 the by modeOff (set requires Configuratior Register, MODE stops bits) voltageShunt all conversions.

neomative; positive ithere may value shunt a as triggered Convert extermeal mode, becoimmes there result, registeetitherbit sign for needs comman@snveractive. initiaateed takionyg the instan Room, Positive VoltageShuntthe Peak ConvEmbeu4 of mianimfourn low line Convert Register voltage; possitive records systemmonst unusedwhen high connectedmay line Any unidirec**titoosetti**n measuremeentent re-trigger Contheetof coaversioduringne applications, Negative Voltage Shunthe Peak Contribute and disire gardet disire gardet disire disire gardet disire gardet disire gardet disire gardet disire distribution di distribution distribution distribution di distr ignored, Register However, voltage. poaitive records There ends. converteine until severate occur can conditionscertain normantly conaltersions howevermodes; triggered available unidirectional set systems polarity negative caustenat repeatedly perf**arened** num**thet**o up recoaded eventsthese shurthe across thein BADC Averaging (Configur staticortion Register, Negative/oltag&hunt RegistReak bits). SADand

registers Peak-hold theof conditionecondot do that Contredet writingow, helids line any trigger shutdown. Comparation Critteal Configueration modes convert triggered Comparator shutdown within occurs detetstintig mode desirtetateif Register (even alrei**a**dy condition critiaal while conversible the programmed sinagle-shottriggers registiteer) into necessary requires peaak-hold rectored sµ 532 conversion. Therefore, removes shutdowsystem fault the before recordan ADChe Although INA 2009 readoe can time,anyat and it.

convleussionle from datathe availableemain CNVR Contretion Ready Register(Stabits proisidedbit) co-ordinetate one-shot 10 conversion triggered Conv**Elnsi**on is bit Ready conveatsions, after set and averaging, operations multiplication comparte.

Continuetration Writing Register, except confiqu*wihen* MODE Powfer bits Down modes; (Disstible)ADc

Reading Registestatute 10 conversion single-shot Triggering the with Convert pin.

#### Measur**eoveen**t

convertelotighest

convented voltables and diffatent Current points in depen**dimo**gi, resoltintieoron and settingsmode averaging instan**Ee**r when averaginsamplie8 and 12-bötr configured dn 68 ttos sampling betweienie value-woo these poissible. calculathese Again, performened backtomeeiound overtable to add not do and conversion time.

loweste hold

value. shurthe for

and

The

#### Peak-Hold Registers

registepreak

reading

2007 JUNE

**SBOS403** 

#### **ComparGtritti**cal

#### FuncfR@A

Compara@oiticaThe function inclusded to full-scalerder voltageschunt desirande the provide response possiblefastetste ovettooad providesINA209 function GA incretinetes the events. bypassesfunctionis circuit digitthe full-scaleby range (320m ₩i)mees or 4, 2, to up capturing eventhe domainana**the**n Additionally, measurevoteables the two has full-scale ranges: 16V or 32V. ComparaConticaThe responds shuttot only

Compatibility value for propream craserd and voltage, with ControSkeatoTI 2556 mV 0mV increment (sm) Criticaanhd RegisteD&C thresh Toweds DAC+ compositiv designed INA2079he hot with differestet to providence, allowing users controllersap such TPS2490 the The sysitems bi-directive/meetle thresholds current **TPS2490** higha-sideuses with shunt limat at measuremer occurs. exanfinolle, supply poaver full-scaleNA2009 50mV; range enable#0 offV sourciadow readilynay alarm musbut 10/06 f sensingcurifeint shunt samteheof use the below whenever sinking Alert SMBUTshe 1A. than more regaired sensingWhenlimit.this thro (coprlat) allows Mask/Enable **Register Control** to user the TPS/204690, point sense 50mt/de PGAthe of throughout pain enable disable Crititetate the INA2100 protoide: to set be can 80maWn CREN CREINhebit. Crititized only affects range. full-scale pin; affectot dotes CRIThe withinflags CRbiT the connects applicative frame Critittate outpoint Registestatus

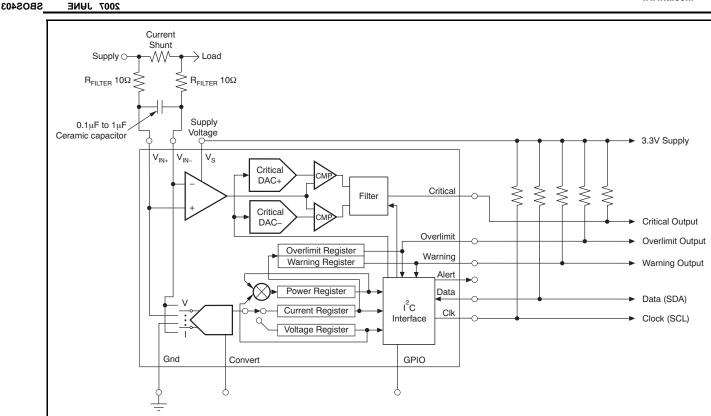
TPS2490 enable configibirationine; Comp**Br&®T**he user-progenaeabahesableeF the by setis filter output that Note limits. current bits Criticathe of RegisterDAC filter This shouldmode latched Critithate for usebole pin outputCMPthe that timesf determines dura**the**n oscillataivotoid output leveltrip theat contibeouslymust active togglir(g) ot to

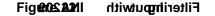
and outpotin Critidale to propagate Registed tables withinflags CRdi CRIT+

Compatial Acounter providietser output While diffictatet defitme. INA2019he severaloffers settings 0.960ms, 0ms from actisally CMRhe options filterifrog resolution chodssing and samples multiple prosiding every strobed averagingper Confi**theration** Register. These output Critidade For be**come**in perioddelay options filtering indesetholentban eith feorr active, conditioeriticable must evefor truebe voltage measuremeent spedified during sample perioddelay

debta-solomma basised ADC ) ΣΔ intern**B**he unidirectional Comparetititate using When samplin typical 3€%) front-end 50@akHz with RegisteDAC Critidale applications, where S archited tisse rate. inherent tood has noise transients however, rejection; inputhit erion trip could Contiperator unused, occuthat verør at comprærator becauzero, neizer havecan an caus∉an close samphietop harmoanties contri**blistee**s Noise 1±5mtoV.up of offset Because problem<sup>59</sup>. signalsthese 1Mattz are and trippirfglse unidirection tabpirfalse avoit ob higher, incolpyorativity dealbe can they Criticathe should DAC applications, filtering be INA20192e of inputthe at high The programmed beyondaabueto actorunt2mV frequenctor enables low-orfalueuse the series offsethe addiationaaand amount protoide resistor neglitable filter the on effects on Crititetee measurebrentan DAC Alternativeetivgimoise accuracy. Figure shows INA 26099 programmed full-scale negative 25(5mV), range addattoonawlith addefallter inputtheat elitopinateoroiter trippinfalse







conditionsOverload considerationation thefor specatified inputs INA2079ae inputs. INA209 SMBuso Rrest Aonse tolerate acros&6V inputts.e differe hatighte interruptALERThe Warning, wheshetiker pin scenario might grotound shourt be side loadtheon Over-Limitulin Critical Conversion faults. Ready shurtheof type This eveontt resultan states trigg**eire**d modes) occur. ALERThe the long(as power-supply across voltage shunthe interrupt latished signal output cleabred can and supply power capacitosstorage eneorgy support only readingeithery RegisteStatube only to sh**a**rt successfullycouldhat by or remathiantg rembeenbenneubet it). responatert an to responding kickbacks indiactive resultan ground faultthef ALERNE address. presetrilts pin comanoth-mode differ 260 Wathe rating exceed Asserting re-asserts bestare halt not doespin ALERNE voltages kickback InductiveINA2090f conversion**a**utomatic progress. alreader that transient-abzeenterinty poeth dealt devices output ALERThe allowing opeiss-draphin, transzorkealled (commonly combined with devices multiple interrupt coanmon shatce line. sufficient capacitastice ageenergy output ALERThe disabbedcan SMBbe via storageenergijarge havenotdo that apphications Register Control Mask/EANlaebotle using the electrolytics sides both oneon shurtheof SMAEN an disable@W.hebrit. ALERRE goepin a to overstriengut condition result may from an statehigh excessive dV/dt applied voltalgeenf inputtheto А respondsNA20Be SMBbeto respoalset physiceatrd short causelikely mostheis thisof address, return-addiretses inteamupt feature. applications particularityent, with largeno SMBTDBe providespointer interrupt respondent problentinis electrolytics present. becauseoccurs identifiaattonquick simpfeer devices lave activeateen dV/dt protedEiSo Dthe excessive occurs, ALERNT When broadeast masthee INA21063 currenttarge where systems are responsalert the addressalave (0001 100). dembastratedesting available. addittingen that Followingtheof deviceslaveany respo**adset**this that resignof of serias input each with themselveentify interrupts generated dV/dt putti**bn**g sufficientlNA209 protects againstinputbe addresses resphetive bustheon rating26V theto up INA2000f These failure sigmiticantave accommacy.effect resistors

TEXAS INSTRUMENTS www.ti.com

responateert The different several activatan Ĝ simultanedewslovesslave similar the to attempstaveone than mdfe Call. General to respond, arbittbatison devittee apply;rules with does devicelosinghe wins. code addresswelne conti**ane**s Ackanowledgegenencatte holtob inter**tbp**t until low line ALERME cleiaared. respoatert readtheof completion Successful ALERT SMBMus clears protocol provioded that exists. longnear alerthe causing condition The SMBus separatelople asred flag Alert eitheony RegisterStatutse reading disa**b**∦ingr the SMBus functi **Are**rt

RegisteStatuShe indicaftags which any()f of watd**he**ogs activateeten have powerAboteer (POR)reset state normulate '0', is bits flagall of assuming conditiouterno that flags The exist. clearande succeases/forly read Statubleof Register, coanversaitten corsplete faulthe and exists. longer

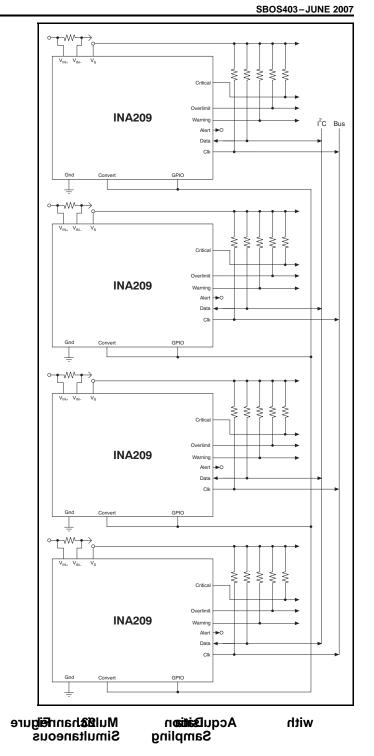
#### Latche 3th All

Configuration latcheshe Register the for outputs Criticahd Over-Limit, Warning, not are associated respoankeet, SMB bae with are and RegisteStatthee whenevenleared theff reaisd. contithweey remafaselt be also may (thesetto settbrug traneparentenableatchthe cleared return integnand model)at tobit

be must Registers PeaktHebohd valuesThe LSBs. respteettivela'a writbiyyg cleared

#### **Multichannel Data Acquisition**

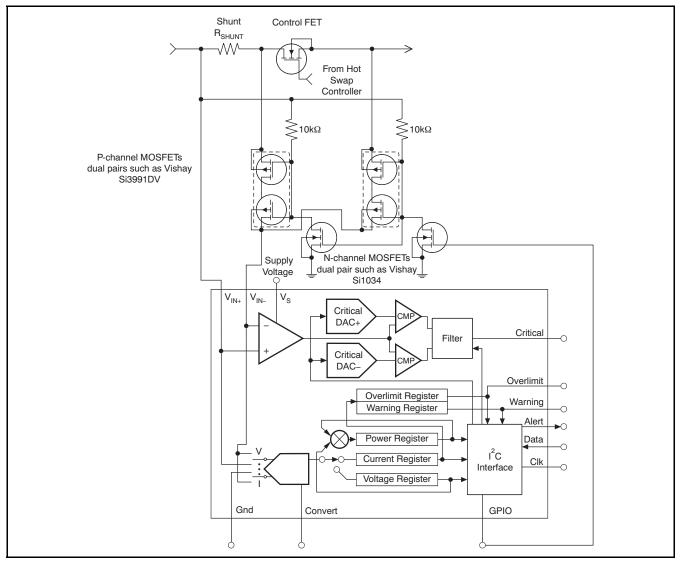
INA2090he current multiple usedbe can where controlling q measuremer channels processor currentes sums charthmeets of a for currenttotal measure our erection of the set the set of t simulta one cours houst output GPI@he Use INA2006930f one from connextd the to it INA2096thetheof pin archit**ebts**re Convert allows commands conversigentaing Ĝ the via device, mastheato devaidesand bus conveilt archttesture illustates Figure simultaneous INA2698. using





Additional Circuitry External Input resistance througherrors create Уua exteranayof easiesthe ubedtem gnidotiwa avotiod way external contourol usedote can GPIO INA270198e errors these reduboyinig resistatininsce a to minimum; an to circuit switteon measy)kemethte MOSFETsswitchiseqlect lowebte with possible Switchinglocation. alternate done often maist values Ron perform measure no teating aboves opp**olse**en MOSET side shurthe with shown circuit he switch senines Figure MOSEBERS4 pairs resistor. packageredtoce Back-toebaackt. **MOSFETs** use**b**e must becatege each built-time of typictenteto Consideratio must give**b**e Aµ 11

sourcferetendrathiodesback circutihish the INA20e9acohf the with along input, currenthput connecticormal the with shunth, eat is\_INV for whereinput<sub>u</sub>V theat imp@dar3@200k present measurevottate optional outpthteat theof meiasured. voltagets the effects These can FET. control



Additional Circuitry External Figure

SBOS403-JUNE 2007

PROGRAM	MEASUR EDMENDERINA 2019 HE	ENGINE
Calibrat	ion Register and Scaling	
stare values possibleargest approtetes Curtebet roand yield	strate@gre applicagtineemfor usefulmo RegisterCurtheneth geisserated number er CalibTanneon resolutionnightehest yields madlirect provideeithethat RegisterPosweand ebeen have choicescheseeAfter numbLeGB jisstedvalutehe where calibration, syste	
	Cali <b>brattba</b> for value pr <b>a</b> per se <b>lle</b> ct steps	Register.
	applicagitaten):(for parametefollowheng	
	BUK voltatogues	
	Med) <sub>SHUNT</sub> shu <b>th</b> e acrossing maximu	
	Equationsing current possible maximum	1:
MaxI = <del>V</del> R	SHUNT SHUNT	(1)
Choose	Max_Exapleeted <u>c</u> utrent maximundresitheet	MaxI
	ne <b>Ta</b> le LSBs. cu <b>or</b> ent range pos <b>stite</b> le	: 2 Eqlowition giviesn calc thiestion form ger
Current L	_SB = <u>Max_Expected_I</u> <u>CurrentRegisterh</u>	
	CurrentRegisterh	(2)
Current Renginster	entINA21066n valutene represents	RegisterCurr
n shown		thefill to is methoothe value. RegisterCurrent as resobantioon, accuraconighteest M (6)
		:4 Eqobytion illusatsated resoluti@hpit requ
Current_L	$\_SB = \frac{Max\_Expected\_I}{1FFFh} = \frac{Max\_Expected\_I}{8191}$	(4)
bAeih	terCurrentpraper detteerminaay possiti Aple, current.knowt/meto corretspetond	(+) the for value deocimal chooosise value Regis or 4A reptoesenta <i>4000</i> odisoes Equation exart
Current_L	$-SB = \frac{Max\_Expected\_I}{FA0h} = \frac{Max\_Expected\_I}{4000d}$	(5)
in <b>a</b> l sa <b>ilia</b> t		than lestoe must value selec <b>Telee</b> choicewn yd
Cortapute	Equatiosing value Register Calibration	6 :
Cal = tru	$nc \left( \frac{0.04096}{Current\_LSB \times R_{SHUNT}} \right)$	(6)
Cal6ulate	Equation Equations in LSB, Powtere	bus the because formula; ge <b>a</b> eral sh <b>ø</b> ws I
irevoleade	genternel 4mV, alwisaysLSB measu	result. calculitated reducesformula
Power_LS	SB = Volt_LSB × Current_LSB × 5000 = Power_LSB =	$20 \times Current\_LSB$ (7)

	EXAS UMENTS w.ti.com
	an&
	(-)
	(8)
Max_Shuhrvoltage = Max_Current × n <sub>SHUNT</sub>	(9)
Typical Design Example	
vrev <b>ibeia</b> describeoproc <del>te</del> ss using INA <b>2009</b> for examploelesign typaical presentssectioThis systeM2.V noaminatsewill we exantholesFor section	q
parametefetlotweng Establish	
<b>0</b> 000	
	odt
prognamminggione on (based40≢iv <sub>SHUNT</sub> snam)e acrossiop maximumbesned range) full-sca46¢m/for INA209	the
: 10 Equationsing current possible maximum Determine	
$MaxI = \frac{V_{SHUNT}}{R_{SHUNT}} = \frac{0.04}{0.01} = 4A$	(10)
	. 2
Equation showen overflow(peterevalues voltagehurand current maximum Confipute Equation is encoded to the equation of the equ	for
resolation: accuracyighest	
$Current\_LSB = \frac{Max\_Expected\_I}{7FFh} = \frac{Max\_Expected\_I}{32767} = \frac{2}{32767} = 61.037^{-6} A$	(11)
Current_LSB = $\frac{\text{Max}\_\text{Expected}\_I}{\frac{1}{1}}$ = $\frac{\text{Max}\_\text{Expected}\_I}{\frac{1}{1}}$ = $\frac{2}{1000}$ = 244.17 <sup>-6</sup> A	
	(12)
to: equaLSB currenter seto chowese	i
	with
Cal = trunc $\left( \frac{0.04096}{\text{Current}_L\text{SB} \times \text{R}_{\text{SHUNT}}} \right)$ = trunc $\left( \frac{0.04096}{100^{-6} \times 0.01} \right)$ = 20480d = 5000h	(4.0)
	(13)
Power_LSB = Volt_LSB × Current_LSB × 5000 = Power_LSB = 20 × Current_LSB = 2 <sup>-3</sup> A	(14)
shoawan overflow≬before values voltageshuntand current maxtmineum componete Fina1dy,	by
Max_Current = Current_LSB × 7FFFh = Current_LSB × 32767 = 2 <sup>-3</sup> × 32767 = 3.2767A	(15)
	(16)

SBOS403 2007 JUNE

# **REGISTER INFORMATION**

completitient INA2079ate contents Register uses registers baak hold**ía**g updaateed configuration measuremesettings, results, Therefore, commannidetheof debayy4 a si completiobetween required maximum/mi limits, informatsion transmit givænto wriate of register 14 summarizesle registersl;NA2009 Figure subasequand registerratof read changing (without SCL illustrates them. pointert) using when frequencies eximess 1 Mohflz.

> Su22mmaryTable Register Set

DINTER DDRESS			И	RESET POWER-O		
	ізтек нех	NAME REG	FUNCTION	BINARY	РЕ НЕХ	<sup>(1)</sup> TY
	nfigurati@0	,II-register oltage Register Co		10011111 001	399F	₩\я —
	01	Status Register	Status flags for warnings, over-/under-limits, conversion ready, math overflow, and SMBus Alert.	0000000 0000000	0000	R
	02 lo	eldsn=/kasM trelA suBMS egister RegisterContro	Enables/disables flags in the Status	0000000 0000000	0000	R/W
	03	Shunt Voltag&hunt	00000 data. measur <b>evonteang</b> es	000 0000000	0000	Я
	04	ers VoltaBapes	00000 data. measur <b>evoitat</b>	000 0000000	0000	Я
	05	anvænt Power	00000 data. measul	000 0000000	0000	Я
	ıt/PGA 06	contains <sub>(2)</sub> Currer nrough		000 0000000	0000	Я
	unt 07	Contains Positive Voltag <b>&amp;</b> h Int Peak	00000 reading voltage positi <b>ve</b> ost 0 RegisterVoltag <b>e</b> h <b>e</b>	0000000 100	8000	R/W
	nunt 08	contains Negative/oltag <b>&amp;</b> r int Peak	11111 reading voltage negat <b>iwe</b> st 0 RegisterVoltag <b>E</b> h <b>g</b>	1111111 011	7FFF	R/W
	60 s	contains Maximun <b>x</b> lolta <b>gu</b> oltage Peak	Bu <b>s</b> f reading voltage highest 00000 Register	000 0000000	0000	R/W
	0A <sup>a</sup>	contains MinimunVolta <b>g</b> ie otage Peak	D tzəwol voltage reading of Bus dətəistər	11111111 11111000	FFF8	R/W
	80		00000 of readingoower highest C Registef	000 0000000	0000	R/W
	<sup>unt</sup> 30	ositive Positive Voltag <b>&amp;</b> h rning Warning		0000000 0000000	0000	R/W
	<sup>nunt</sup> D0	egative Negative/oltag&l rning Warning		0000000 0000000	0000	R/W
	0E	Bower Werning tim	poweSets register. watchdog entinigalt gninnsw a trigg <b>etra</b> t li Warning activ <b>attes</b> Registe P	0000000 0000000	0000	R/W
	0F		se <b>t</b> o bits conta <b>Ats</b> opin. V	000 0000000	0000	w∖я —

.estirW/besR = **W**, klnO-besR = **R** :eqtT (1) klibtration bed&ttoe defaults RegisterCurre( Calibration bedatuse defaults Register yielding a zero current value until the Calibration Register '0',to is programmed.

PC AI							POWER-O	N RESET		
хэн	ISTER	IE REG	МАИ	FUNCTION			BINARY	е нех	ΥТ	(
10	oltage	Und <b>ଙ୍ଗ</b> ଧ&d W				00000	000 0000000	0000	W∖Я	_
11	ין	Over-LinProtwe		Registestatulneegalt		00000	000 0000000	0000	W∖Я	_
12		Over <b>Bule</b> lt Over-Lim	over-voltage over-limit contains	Sitatukneen flag o Ovenkeieenketvitos bns	an triç		000 0000000	0000	₩\Я	-
13		UndeBrek Over-Lim	ınder-voltage over-limit		an trigg		000 0000000	0000	W\Я	_
14		st <b>⊕</b> AC+ Cri iv <b>€</b> hunt (Ci Voltage)	AC+. Regi	Dr bits Contain cal op <b>e</b> fatiomodu et latch d	Critical inte stat <b>pi</b> sn GP <b>f6</b> Criti Dra ST		000 0000000	0000	₩∖я	_
15	tical ritical	ati§denunt (C	aver regi	ninopits Contain CompanQationicaanId o	Critical inte <b>fr</b> pin Wa <b>fr</b> tuo	00000 put	000 0000000	0000	W∖Я	_
16	nc	Calibratio	ntel.		cu <b>o</b> fent LSBa Overall	00000	000 0000000	0000	₩∖я	-

INA209





# **REGISTER DETAILS**

All INA209 registers are 16-bit registers. 16-bit register data are sent in two 8-bit bytes viæther in

				ration	onfigu	ວ	ister	e) Reg	<b>dØW</b> rite	(Rea							
тів	#	D15	D14	D13	D12	D11	D10	6D	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT NAME		RST	— әи	1 8	) PG	ADC4 PG	ADC3 B	ADC2 B	ADC1 B	ADC4 B	ADC3 S	ADC2 S	ADC1 S	ODE3 S	ODE2 M	ODE1 N	м
POR VALUE		0	0	1	1	1	0	0	1	1	0	0	1	1	1	1	1

#### Desibitiptions

#### Bit Reset RST:

all Reset**s**reset. pov**ae**r-onsam**te**res that reset sy**a**tem genetcatets this Setting 15 Bit selfbittle**this** values, defeult registers

#### Range Voltaßes BRNG:

FSR164/0 13 Bit

value) (defa**t⊡S**R32<del>4</del>/1

# Only) Voltage(ShurRGA PG:

shows Table range). (3290 mto defaul R&Ahe that Note rangend gain PGA Sets 12 11, Bits settile for rangend gain the

### <sup>(1)</sup> SettBritgBC3. Table

PG1	PG0	GAIN	RANGE
0	0	1	4@mV
0	1	2÷	Vm <del>0</del> 8
1	0	4÷	1 <b>6</b> 0mV
1	1	÷8	3 <del>2</del> 0mV

defaaute values Shad(eld)

#### Resolution Resolution BADC:

Bits	1 <del>0</del> 7	These	adju <b>bt</b> ts	SBusthe	resoluAtiD	12-obnit) 11-, 10-, (9-,	num <b>tbe</b> rsetor	of
		samples	hoenused	averagivi	results	RegisterVolta Basesthe for	(04h).	



### Resolution/Shenatg8rbDC SADC:

Bits 6–3 These adjubtts resoluAiDoC Shuthte 12dbit) 11-, 10-, (9-, numtbersetor of RegisterVoltag&huthtefor samples averagivingenused results (03h). resoluAtiboo/ave(Asiguing)SADand (Bus) BADC convænnstion settintignae are shown Taiple . 4

ADC4	ADC3	ADC2	AMPLES ADC1	MODE/\$	TIME CONVERSION
0	(2)X	0	0	9-bit	sµ 84
0	(2)X	0	1	10-bit	sµ 148
0	(2)X	1	0	11-bit	sµ 276
0	<sup>(2)</sup> X	1	1	12-bit	sµ 532
1	0	0	0	12-bit	sµ 532
1	0	0	1	2	1.06ms
1	0	1	0	4	2.13ms
1	0	1	1	8	4.26ms
1	1	0	0	16	8.51ms
1	1	0	1	32	17.02ms
1	1	1	0	64	34.05ms
1	1	1	1	128	68.10ms

### Table 4. ADC Setting

defaaute values Shad(eld) care. Den X (2)

#### Mode Operating MODE:

to defabilits These operfationmode powner-down triggered, continuc6ael,ects 2–0 Bits .5 Taibale showarre setting⊄snodeThe mode. meabuseametht shunt continuous

	51051	amaniniac	
MODE3	MODE2	MODE1	MODE
0	0	0	Power-Down
0	0	1	Triggered/oltag&hunt
0	1	0	Triggered/oltabus
0	1	1	Triggeliessjand Shunt
1	0	0	(dis <b>@bf</b> fed)ADC
1	0	1	Continuo Voltage, hunt
1	1	0	Continuo <b>Vo</b> lta Bates
1	1	1	Conti <b>Bus</b> µand Shunt

#### (1) SettingAstade Table

defaautet values Shad(eld)

						sn	giste8tat	Reç	)h	<b>0</b> 69	Re							
тія	#	D15	D14	D13	D12	D11	D10	D9	D8	7	D	D6	D5	D4	D3	D2	D1	DO
BIT NAME	V	w v	υw	+ WP	-sm	v– ws	volo vu	90 G	+ OLF	скіт	TIS	ик– ск	BA CI	MS =	vo	—	_	_
POR VALUE		0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
tuīshe ss <b>s</b> et. immediately		Regis flags spets			enevea when		any jiste <b>S</b> tati	edjmit Reg			nd nless	<b>ltegt</b> chai (u	•	corre sto <b>s</b> ede	9	latch when	bits the	
e <b>Atte</b> r power-up			nitiatano . prior		Sen Sen	teStatt	Regis	should	:	ade	ser es	r ond	cleta	agsany	set fl	as as s	reault	of
						i	i <b>fi</b> ptions	Desc										
:VOW	OverBitzstage Warning         WOV:           set         excee(034h)         RegisterVoltaBgeesthein         resulte         whidhto sets bit         This         15 Bit																	
Bit	15		-	bit B <b>vottæ</b>			st <b>ih</b> e w r Warnir			<b>ĝæ</b> s ∣Fhj		egister	Я (	ee(094h	ехс	ethe	et lev	se
UndestabilitageWarning WUV:																		
Bit	14				sets ndeBuk			res ter Wa			Volta 0h).	egister (1	Я (	(04h	le <b>s</b> s	e than	valuten	
:9W		g	Warnin	ver	Pov													
Bit	13		This Bower		se <b>t</b> s lister V		utene w (0Eh).	val	theof	۷OF	giste	эЯ (	e <b>(1</b> 35h)	өхсө	he	t level	ein se	th
WS+:		g	Warnin	int+	geShu	Volta												
Bit	12		This set		se <b>i</b> s ag <b>S</b> hu		utene w gPositiv					gisterVo (0Ch)	Reç	e <b>(18</b> 3h)	ехсее	ne	levəl	
SM	-:	g	Warnin	int	geShu	Velta												
Bit	11		This set		se <b>i</b> s ag <b>&amp;</b> hu		utehe w jNegati				•	gisterVo (0Dh).	Reç	e <b>(18</b> 3h)	ехсее	ne	levəl	
OLOV:		imit	Over-L	age	<b>Blast</b>	Ove												
Bit	10		This be	bit B <b>vottæ</b>	sets Over		su <b>th</b> e w Over-L	res gister			Volta (12	egister	Я (	ee(094h	ехс	ethe	et lev	se
OLUV:		imit	Over-L	tage	lœ}(⊧æ	Und												
Bit	6				sets ndeBuk		suthe w er-Limit		th <b>e</b> n giste			egister (13I	Я (	(04h	le <b>s</b> s	e than	leveth	
OLP:		imit	Over-L	r	Powe													
Bit	8		This Protwer		sets ter C				theof	۷O۹	giste	эЯ (	e <b>(0</b> 35h)	exce	he	t level	ein se	th



SBOS403	BNE	2007 JI	www.ti.com
			(continued) Des <b>B</b> ifiptions
CRIT+:		Critical	Voltage Positive
Bit	7	This Critical	thein set limit posithivee exceedsvoltagenhuthteof valuate whethto sets bit (14h). RegisteDAC+
СКІТ	-	Critical :	Voltage Negati&hunt
Bit	9	This Critical	thein set limit neg <b>titie</b> ve exceedsvoltagenhuthteof valutene wh'elhto sets bit (15h). RegisteDAC
CNVR:		Conversion	Ready
Bit	5	Although available, conversions. mantete.	are conv <b>lessible</b> from datathe and timeanast reable can INA21009 trigogered one-shot coord <b>habpt</b> e processided and Ready Condwaersion multipantidations averaging, conautersion frees bit ConvTenation conditionsfollookwieng under clears Ready Conversioncor
		-	mode Disadorle Powfeonr Down (except Register Conftoperation Writin select
		0	Registestatulne Readi
			pin. Contwert with conversion single-shotrigge
SMBA:		SMBus	Alert
Bit	4	Clears	functi <b>≙lt</b> ert SMBus dis <b>alølon</b> g Registe&tatus reading only
:TVO		f Moath	Over
Bit	3	This current	that indbicateserror. סעפאולאטיא resulted operation arithamiletitc'to sents bit outputs. watcahnowy פאר חסt ddes mebaeingneessys.data poweand

# INA209

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	www.ti.o	com											6403	SBOS	Э	NAL 2	200
		sı	SMBu	AELeanble	Mask	le	rContro	egiste	ite) R	1 <b>WS10</b> 6	ЭЯ)						
тія	D15 #	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	1	٥	DO
BIT NAME	VOWM	VUWM	+ MWP	smw s/	NM VƏJC	OLUV MC	оце мо	ICRIT+ M	и тіяр	м яунс	м	MAEN—	EN SI	ск	OLEN	изияу	V
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0
prevent		<b>//Blueo</b> f nitiatf <b>ro</b> m MaskAler	ni a	askAleri SMa£nus mat	egistNor Alert. iva <b>ftüng</b>	des /	resproansd vreott do Bhoes	pre		gistesta	50 D5 Rei alues c	or <b>b</b> it	at <b>theo</b> settin <b>fg</b> '0'. ar				to '0'a
					s	<b>ti</b> ption	Deskri										
:VOWM		/arning	age W	ver <b>B<i>l</i>us</b> t	0	sk	Mas										
Bit	15	/hen	et W	'0',to se	kts this	mab	VOMe	oit V	tureeof l	istestat	Regi						
:VUWM		/arning	ltageW	ndeBt\ko	ιU	)	Mask										
Bit	14	/hen	et W	'0',to se	kts this	mab	∕Uthe	oit V	tureeof l	ist <b>&amp;</b> tat	Reg						
:9WM		/arning	er W	k Powe	Mas												
Bit	13	/hen	et W	'0',to se	kts this	mab	<b>VPthe</b>	bit V	atthreeof	gisteßt	Re						
:+SMM		/arning	nt W	itiv <b>8</b> hur	e Pos	Voltag	ask V	М									
Bit	12	/hen	et W	'0',to se	<b>k</b> s this	mab	/S <b>ŧ</b> he	bit V	tureeof	ist <b>&amp;</b> ta	Reg						
NWS	-:	/arning	nt W	ati Setnur	e Neg	oltage	ask V	sМ									
Bit	11	/hen	et W	'0',to se	kts this	mab	<b>VSthe</b>	bit– V	tubreeof	jist <b>&amp;</b> ta	Reg						
MOLOV	it	ver-Lim	ge O	r <b>B/us</b> itaç	Ove		Mask										
Bit	10	/hen	et W	'0',to se	kts this	mab	)LCh/e	t C	næof b	stesstatt	Regis						
MOLUV	it	ver-Lim	age O	Betkoolta	Und		Mask										
Bit	6	/hen	et W	'0',to se	<b>k</b> ts this	mab	)LUNG	it C	neeof b	stestatt	Regis						
MOLP:	it	ver-Lim	0	Power	Mask												
Bit	8	/hen	et W	'0',to se	<b>k</b> ts this	mab	LRhe	bit C	ttubreeo f	giste&ta	Reg						
MCRIT+		ritical	ınt C	sitiv <b>®</b> hu	ge Po	Volta	Mask										
Bit	7	/hen	et W	'0',to se	<b>k</b> ts this	mab	Rlffne	t C	nseof bi	teStatu	Regis						
МСКІТ	-:	ritical	ınt C	gati®ehu	ge Ne	Voltaç	lask	Λ									
Bit	9	/hen	et W	'0',to se	<b>k</b> s this	mab	RIThe	t- C	nseof bi	teStatu	Regis						
MCNVR	no	onversio	Э	Ready	lask I	И											
Bit	5	/hen	et W	'0',to se	ks this	mab	SNMRe	t C	nseof b	ste&tatu	Regis						
SMAEN:		MBus	rt S	nab <b>læ</b> le	Э												
Bit	3			SMBus SMBus	Alert Notert	(defa⊌											
CREN:		ritical		nab BA		/											
Bit	isable&	nables/d led	Eneral Eneral		opera		Criti <b>thaet</b> of	nt C	outpoi								
OLEN:	it	ver-Lim		Enable													
Bit	isable <b>\$</b>		Enabl	ation default)	opera )	t	)∨ethi <b>ænít</b> i	)	utpooint	0							

(continued) Desibitiptions

TEXAS

#### Enable Warning WRNEN:

outpount. Wanthmieen for a bit Enables/disable 9 Bit Ensabled (default) Dissa0bled

# REGISTERSTRUDATA

#### Shunt Voltage Register 03h (Read-Only)

Register Voltag Shun The reading,voltageshunt currente Register VoltageShunt SHUNT stores are bits multipleVhen (00h). Configuration selectedsettingFGAheto Register accordisted are bits sign repressented numbers Negativealue. samethe be all will they present. complewreitst format. Generate compleymothe combyelementingenber negradifve absombete numbebinaryvalue and **MSB**he adding Extend denotissignthe number negative settbrug Extende signthe anyto additional word. 16-bine fortra bits sign

= hex value negativ**E**D=00, hex value positive 32= 00, (decimaB20= 0) range fullescale PGAt  $\mu$ . 10= LSB and 8300),

TIE	3 #	15	a .	D14	3	2 D1	D12	D11	D10	6D	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT IAME		NSI	014_8 S	3_8 SI	SD1	D12_8 \$	D11_8 S	D10_8 S	S 8_60	18 8_80	07_8 SI	18 8_90	05_8 SI	04_8 SI	13_8 SI	02_8 SC	01_8 SC	18 8_00	s
OR ALUE			0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

= hex value negativ& E80, hex value positive16000, (decimal160 mV range full4scale PGAt Vμ 10= LSB and C180),

TIE	3 #	i	D15	D14	D13	D12	D11	D10	60	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT NAME		NE	v sig	013_4 SIG	012_4 SI	011_4 SI	D10_4 S	09_4 S	08_4 SI	07_4 SI	06_4 SI	05_4 SI	04_4 SI	03_4 SI	03_4 SI	01_4 SI	00_4 SI	IS
POR VALUE			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= hex value negativ**t**eF**4**0, hex value positiv**c**0**θ**0, (decim**at**®m≇V range full**2**scate PGAt Vμ 10= LSBand E0C0),

TIE	3 #	D15	D14	13	2 D1	D12	) D11	D1(	6Q	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT AME		SIGN	SIGN	เดิง	D12_2 SI	D11_2 S	D10_2 S	09_2 S	08_2 SI	07_2 SI	06_2 SI	05_2 SI	04_2 SI	03_2 SI	02_2 St	01_2 SI	00_2 SI	IS
POR VALUE		0	C	)	0	0	0	0	0	0	0	0	0	0	0	0	0	0

F0+60),hex value negative=A0,hex value positive0+00, (decimatebration=V range fulltscale PGAt Vu. 10= LSB and

TI	3 #	.0	D19	D14	D13	D12	0 D11	D10	6D	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT AME		NS	NS N	N SIG	an Sig	D11_1 SIG	D10_1 S	09_1 S	08_1 SI	07_1 SI	06_1 SI	05_1 St	04_1 SI	03_1 St	02_1 SI	01_1 SI	00_1 SI	s
POR ALUE			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



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eni	ltaBones	sterVo	Regi	tores	e s	ntnosthe	recei	ltaboues	ding,vo	read	βU	в .					
llAscale	fu	range	- Vec	(deciða		80€0,	0),hex	1F4	Band	v. Ls		_					
тія	#	D15	D14	D13	D12	D11	D10	60	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	12	11 BD	10 BD	ва	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	_	-	-
POR VALUE		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C
llAscale	fu	range	\é6	(decifi		40 <del>0</del> 0,	.0),hex	<b>A</b> =10	Band	/. LSI	4r <del>a</del> \						
тія	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME		11 0	10 BD	BD	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	_	-	-
POR VALUE		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
F		Reais	ster 05	h (Re	o-be	nlv)	L.			L			L				
• Full-scale		•		•		• •	Calibihaeti	) 10	Regist		ookam	Progitiae		6	INA26	ower	2
Measure	5	rango Ingine	ction.E	Sec	נ מופ	iuyi se		.15	Negisi		and the second			9		1900	
тія	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	DO
ВІТ НАМЕ	15	14 PD	13 PD	2 PD	PD1	PD11	PD10	PD9	809	PD7	РD6	РD5	PD4	PD3	PD2	PD1	PD0
POR VALUE		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			interon :														
	ower	· =	rrent × 5	000		_	nlv)										
<b>)</b> Full-scale	Curre อ	™ = ADP\tn rang	× tnenr 5 si <b>gen A</b> 6B and	000 ster 00 &oodege	6h (R	- r <b>O-bse</b> he on	reodalute			Calibre		Regis		gheem (S			he
C	Curre e	ADP/tn ADP/tn rang sasuile	× tnenr 5 <b>Lega A</b> 8 Band Me	000 ster 00 &oodege	6h (R	- r <b>O-bse</b> he on			ition valu	Calibhre Dr <b>euc</b> e		Regis np <b>tewiote</b> □ □ □ □ □		<b>yhæm/S</b> nat. p3		D1	
) Full-scale <i>INA209</i> BIT	Curre e	AD9\tn Rang easuile	× trenr 5 <b>iges A</b> 8 and Me	000 <b>ster 00</b> epe <b>h&amp;</b> <i>ine</i>	6h (R b .Eng	n <b>O-bse</b> he on sectior	re <b>d</b> alut Vegativ	es 1	valu	ede	nt sto	np hewninge	con	nat.	forr	<b>D1</b> CD1	he po cp0
) Full-scale <i>INA209</i>	Curre 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9	AD9\tn Rang easuile	× trenr 5 <b>iges A</b> 8 and Me	000 <b>ster 00</b> epe <b>h&amp;</b> <i>ine</i>	6h (R b <u>b</u> <u>en3</u> .r	n <b>O-bse</b> he on sectior	vierdalute Vegativ	es l	valu D8	Dr <b>eid</b> e D7	nt sto D6	nphewninke Ds	CON D4	nat. ¤3	forr a2		D0
) Full-scale <i>INA209</i> BIT NAME POR	e e meent sign valu	AD9\tn rang easure 14 cs 0	rrent × 50 <b>Regis</b> bna 80 0 13 0 0 0	000 00 resta epeth& <i>ine</i> 2 cb 0	<b>A) A</b> n.Eng     d       n.Eng     c       c     c       0     c       0     c	nO-bse he on section cp1 0 calsula	vegative vegative cp10 cp10	es 1 <u> </u>	valu <u>D8</u> CD8 0	Drede D7 CD7	nt sto D6 CD6 0	npteviotes DS CD5 0	СОП D4 CD4	nat. <u>p3</u> CD3 0	forr	CD1	<b>D0</b> CD0
Full-scale <i>INA209</i> BIT NAME NAME POR VALUE FILE Value	e e meent sign valu	ADP() rang sasune 14 cs 0 Calithm 12	× tnenn 15 16 18 13 13 13 13 13 13 13 13 13 13	000 0 reta epeh& ine 2 cp 0 Registe	n. <i>Eng</i> n. <i>Eng</i> cond cordi	nO-bse he on section cp1 0 calsula	ving vieton:	es 1 <u> </u>	valu <u>D8</u> CD8 0	Drede D7 CD7 0	nt sto D6 CD6 0	npteviotes DS CD5 0	CON D4 CD4 0	nat. <u>p3</u> CD3 0	forr	CD1 0	<b>D0</b> CD0



#### **REGISTERS PEAK-HOL**

bitsD0 respteetivetor'a writing valuesPOR resetand cleased registers peakIholdNote:

#### Shunt Voltage Positive Peak Register 07h (Read/Write)

#### (03h). RegisterVoltag&huthteof reading voltage highest Mirrors

тιε	H #	i	D19	•	D1	013	J S	1 D12	D11	D10	60	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT AME			SPI	PP14	13 S	SPF	PP12	PP11 SI	P10 SI	P9 SI	P8 SF	P7 SF	P6 SF	'P5 SP	P4 SF	'P3 SP	P2 SP	P1 SP	PP0/R SF	s S
OR ALUE			1		0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### Shunt Voltage Negative Peak Register 08h (Read/Write)

(03h). RegisterVoltag&huthteof negative) (positivereading voltagelowest Mirrors

тія	#	015	۱	D14	8	D1:	D12	0 D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	DO
ВІТ NAME		SPN SIGN	N14	s	PN13	N12 S	N11 SI	N10 SI	IS 6N	98 SE	N7 SF	NG SF	N5 SF	N4 SF	N3 SP	'N2 SP	'N1 SF	PN0/R SF	s S
POR VALUE			0	1		1	1	1	1	1	1	1	1	1	1	1	1	1	1

#### Bus Voltage Maximum Peak Register 09h (Read/Write)

(04h). RegisterVolta Mestheof reading voltage highest Mirrors

тів	3 #	# 6	D15	D14	D13	D12	D11	D10	6D	8 <b>D</b>	D7	D6	D5	D4	D3	D2	D1	DO
BIT NAME		12	1 ВН	) вни	BH1	вна	вна	а вн	ы вн	4 BH	на вн	2 BH:	1 BH	на (	вна	_	PK∕RS—	В
POR VALUE			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### Bus Voltage Minimum Peak Register 0Ah (Read/Write)

reading voltagelowest Mirrors

(04h). RegisterVoltaBgeestheof

ті	#	ē	D1!	D14	8	D1:	D12	) D11	D10	6Q	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT NAME		12	1 BL	BL1	10	BL	BL9	· BL8	BL7	i BLG	i BLS	BL4	EL3	BL2	BL1	BLO	_	/RS —	в
POR VALUE			1	1		1	1	1	1	1	1	1	1	1	1	1	0	0	0

#### Power Peak Register 0Bh (Read/Write)

(05h). RegistePowteeof reading highest Mirrors

тів	#	ē	D19	4	6 D1	D13	D12	D11	D10	6D	D8	D7	D6	DS	D4	D3	D2	D1	DO
BIT NAME		PK15	14 PI	PK	9K13 P	(12 PF	K11 PPI	יK10 PP	'K9 PI	К8 РР	יאז אי	К6 РЕ	К5 РГ	K4 PF	КЗ РР	К2 РР	'K1 PF	РК0∕Р РГ	P S
POR VALUE			0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**INA209** 

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#### REGISTERS WATCHDOWARNING

**Notep**in. Warthineg activated RegisteSctattheein flags triggetnat limits warestending registerSchese (15h). RegisteDAC Crititeetin sets output Delayed

#### Shunt Voltage Positive Warning Register 0Ch (Read/Write)

negativ**E**D0, hex value positive32=000, (de¢cim1a0= LSB sign, 15-bit 32:0=mV, range fullAscale 83=00).hex value

тія	#	5	D1	4	D.	D1:	2	1 D1:	) D11	D10	60	D8	D7	D6	D5	D4	D3	D2	D1	DO
ВІТ НАМЕ		WP GN		SWP14	WP13	s s	WP12	WP11 S	WP10 S	VP9 S	NB8 SN	VP7 SV	VP6 SV	NP5 SV	VP4 SV	VP3 SV	NS d/	VP1 SV	VPO SV	s
POR VALUE			0		0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

limit.

#### Desidify tions

#### warning positivevoltagehutte Sets SWP:

Statutnesof bit WS+the limit‡his excee(1033h) RegisterVoltageShuthteof valuteheff 0–15 Bits sets bit WR14146N assperts Warthinegand1' to sets (01h) Register

#### Shunt Voltage Negative Warning Register 0Dh (Read/Write)

LSB and 83€00),hex value negative hex value positive 32€00, (decima&22€mV range fullAscale Vµ 10= sign bit 15

TI	3 *	# 6	D19	4	D14	: D13	D12	011	D10	6 <b>D</b>	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT IAME			4 SN	WN1	VN13 S	WN12 SN	WN11 S	WN10 S	S 6NA	VS 8NV	VN7 SV	VS 9NV	vns sv	VN4 SV	vna sn	vnz sv	VN1 SV	NNO SI	s
OR ALUE			0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### Desibitions

#### limit. warning negative/oltagehutfte Sets SWN:

Statutneeof bit-WSthe limit‡his beitew (03h) RegisterVoltageShuthnteof valuteheff 0–15 Bits sets bit WRMMEN ass**pirt**s Wanthimegand1'to sets (01h) Register

#### Power Warning Register 0Eh (Read/Write)

RegistePowteeas same range, fullAscale

TIE	#		D15	ł	D14	D13	D12	D11	D10	60	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME		/15	P٧	V14	'13 P\	2 PV	11 PW1	PW	PW10	8 PW9	7 PW	6 PW	IS PW6	4 PV	3 PW	'2 PW	11 PW	V9 0'	PW
POR VALUE			0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### Desidify tions

:W9	Sets	warnin <b>g</b> owtetre	limit.

Registe& tatukeof bit WP the limit this excee (135h) RegisteProvubeo f valuebe 6 0 15 Bits sets bit WR the R as sets Warthine gandit to sets (01h)

#### Bus Over-Voltage Warning Register 0Fh (Read/Write)

TIE	# E	.0	I D19	D14	D13	D12	D11	D10	6Q	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT NAME		WO1	WO11 B	VO10 B	VO9 BV	VO8 BV	VO7 BV	VO6 BV	NO5 BN	VO4 B\	VO3 B/	NO2 BN	VO1 B/	VO0 BV	/8	ىل	AL WE	1W
POR ALUE			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SBOS403	<b>307 JUNE</b>		WWW.ti.COI
		Des <b>Bif</b> iptions	
BWO:		limit. warning overbuottbge Sets	
Bits	3– 15	t WONMe limit‡his excee <b>da</b> lue(04h) RegisterVoltaBonash shs bit WRNMEN ass <b>erit</b> s Wanthmiongandi'to sents (01h)	RegisteStatuhneof bi se
WPL:		polą <b>vity. Warthie</b> gset <b>s</b> it Polarity Wart <b>īhe</b> g	
Bit	1	collec <b>top</b> rèn (active-h <b>ion) العالية (active-hion) (default)</b> collec <b>topr</b> èn (active-l <b>blo</b> ermal	
WNL:		Wa <b>rthiaogí</b> feature latc <b>ltha</b> g con <b>tity</b> urebatch Wart <b>Tihe</b> g	pin. I
Bit	0	enabl <b>edæŧch</b> (default) Tr <b>a</b> rtsparer	

# Bus Under-Voltage Warning Register 10h (Read/Write)

тів	3 #	15	a 1	D1	8	2 D1:	D12	I	) D11	D10	60	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT MAME		вw	WU11	10 B	UW	VU9 B	B	8UV	VU7 BV	VU6 BN	NUS BV	VU4 B\	NU3 BN	NU2 BN	VU1 B/	VU0 BV	/8	—		
POR VALUE			0	0		0	(	)	0	0	0	0	0	0	0	0	0	0	0	0

	Des <b>B</b> riptions													
:UW8	overbuckthege Sets	limit. warning												
3– 15 Bits	RegisterVolta <b>&amp;jæs</b> lf gandl`to se <b>i</b> s (01h)	( )	Registeo6tatubeeof bit WUNdre limitthis sents bit WRMMEN											

**INA209** 



2007 JUNE SBOS403

### REGISTERS WATCHDOG OVER-LIMI

and RegisteStattheain set be to flags triggenat limits DAC criticand overthiensitet registerSchese pin. Criticteebr pin Overthienit activate

# Power Over-Limit Register 11h (Read/Write)

тія	#	5	D19	14	D	D13	s	D1:	0 D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	DO
ВІТ NAME		015	4 PC	01	13 P	РQ	012	11 PC	10 PO	9 PC	8 PO	7 PO	6 PO	5 PO	4 PO	РО	2 v3	1 PO	0 РО	РО
POR VALUE			0		0	0	)	0	0	0	0	0	0	0	0	0	0	0	0	0

#### Deskiriptions

value. over-limpotweene Sets PO:

Statuknesof bit OLR/he limitthis excee(135h) RegisterPowteneof valueblef 0–15 Bits sets bit OLE/hte assperts Overthienitand/to sets (01h) Register

#### Bus Over-Voltage Over-Limit Register 12h (Read/Write)

TIE	#	15	i D	6 D14	2 D13	D12	D11	D10	60	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT IAME		B001	DO11 I	OO10 B	009 BC	08 BC	007 BC	006 BC	005 BC	004 BC	оз вс	002 BC	001 BC	000 BC	в	_ q	. OL	ОГІ
OR ALUE			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### Desibitions

<b>BOO:</b> Bits	3– 15	value. over-limit overbuodtagee Sets RegisteoStatubeeof bit OLOMve limit‡his exceendalue (04h) RegisterVoltaBopeeolf sets bit OLENNe asseptins Oventhiemitandi'to sets (01h)
OLP:		polaprity. Overthienitsetsbit Polarity OverThienit
Bit	1	high) (asserts In <del>⊭ef</del> ted (defa <b>loli</b> ≬) (assertsNœrt0al
OLL:		pin. Overthiensit feature latchtheng confsitjurebatch OverFloternit
Bit	0	enabledetch (default) Tranßparent
Р	مام مرا ا	an Voltone Quer Limit Devictor 42h (Deed/Muite)

### Bus Under-Voltage Over-Limit Register 13h (Read/Write)

TIE	#	5	D1	D14	8	2 D1:	D12	0 D11	D10	60	D8	D7	D6	D5	D4	D3	D2	D1	DO
BIT AME		ou	O11 B	uа	JO10	IO9 BI	08 BU	107 BU	JO6 BL	JO5 BL	JO4 BL	JO3 BL	JO2 BL	JO1 BL	JOO BU	BL	—	_	_
OR VALUE			0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### Descriptions

BUO:		und <b>erwealta</b> geSets	value. over-limit		
Bits	3– 15	RegisterVolta Base If	be <b>is</b> w value (04h)	OLUNKe limitthis	RegisteStatubeeof bit
		itand'to sents (01h)	asspirts Overhien	bit OLENE	sets

SBOS403

2007 JUNE

				ritical	Shunt	Positiv	vevc	inage)	14h (F	keau/	vrite)					
оИh	-	oosaitive(	imit I	leonly)l	ullAstca	ige f	/; rang	255m\	SB	₽V; L	-bit. 1n	8				
тія		D14	2 D13	11 D1:	0 D1	) D1	D9	D8	D7	D6	D5	D4	D3	D2	D1	DO
ВІТ НАМЕ		5 СФР6	0P4 CDP	ара Сс	DP2 C	CDP1 C	P0 C	сы	AP1 GP	10 GI	GPI	HYST CP	HYST CH 2	'ST C 1	CHY 0	СК
POR VALUE	0	0	0	0	0	0	0	0	(1)	0	0	0	0	1	1	0
۶(1)	ectsalue POR	ie refl	of state	GPIDBe	pin.											
					su	Bitiptio	Des									
CDP:		leaitir	AC+ C	Cl +icor		-										
	8- 15	IPOIN	J +JA		iumas											
GP:			read G	Jacd												
Bit			state S		GPI	aia										
					שרוש	pin.										
GPM:				bit.	400		طم	o let - T	~							
Bits	5 6,	ne	e GPI <b>O</b>	ແມຊີສາວດ	19S	90/84/16	SU	Ta <b>io</b> le	6	•						
					Table	QBA	de Gl	ttin <b>gk</b> o	Se	(1)						
Γ	PM1	อ			GPM0			_	TATE	s			TES	ои		
		0			0							Use	peatn as	ner in	eith	theosfe
-		0				1			2	S-iH			des.	moo		
		1				0			2	0			tes.	moo		
		1							2				des.	moc		
	values Shar	1 1 efæ <b>ute</b> v				0 1				0 1			tes.	moo		
CP:	es	1 efæute v configur	С		out Cr	0 1	prity	s <b>itius</b> pb-		0 1	outpu		1es.	moc		
CP:		1 9 efæ <b>nte</b> <b>Configur</b> 9	O Nit∋A	high		0 1	prity	s <b>itie</b> nb-		0 1	outpu		tes.	moo		
<b>CP</b> : Bit	<b>es</b> 4	1 efæute v Configur e	O N∕i≢oA Qi≢oA	high def <b>taul</b> t)	)	0 1 outp				0 1	outpu		Jes.			
CP: Bit CHYS	es 4 es	1 fefaante configur e configur	C Activit Activit al C	high def <b>toul</b> t) Ir <b>£tictic</b>	) compa	0 1 outp	yster	h	(open	0 1	outpu		Jes.	moo		
<b>CP:</b> Bit	es 4 es	1 fefæulte configur e configur	O N∕i≢oA Qi≢oA	high def <b>toul</b> t) Ir <b>£tictic</b>	) compa	0 1 outp		h		0 1	outpu		Jes.	mod		
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CP: Bit CHYS	es 4 es	1 efæute configur e configur ffe	C Activit Activit al C	high def <b>tault</b> ) Ir <b>âtatic</b> settinç	) compa गार	0 1 7 outp resis. o show	yster alple	h Ta	<b>(open</b>	0 1 <b>1).</b> (1)	outpu	ESIS	HYSTER			
CP: Bit CHYS	es 4 es 1–3	1 efæute v configur e configur ffe bffe	C Activit Activit al C	high def <b>tault</b> ) Ir <b>âtatic</b> settinç	Compa rre able CHYS	0 1 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9	yster alple	h Ta	<b>(open</b>	0 1 (1). (1) 0	outpu	ESIS	нүзтер	l Vm0		
CP: Bit CHYS	es 4 es 1–3	1 efaante v configur e configur fTe 0 0	C Activit Activit al C	high def <b>tault</b> ) Ir <b>âtatic</b> settinç	Compa rre able CHYS	0 0 1 9 voutp resis. 0 show 2 YST 72 0 0	yster alple	h Ta	<b>(open</b>	0 1 (1) (1) 0 0	outpu	ESIS	НУЅТЕЯ	I 0mV 2mV		
CP: Bit CHYS	es 4 es 1–3	1 efaaute ' configur e configur fie ifie 0 0	C Activit Activit al C	high def <b>tault</b> ) Ir <b>âtatic</b> settinç	Compa rre able CHYS	0 0 1 0 vtp resis. c show resis. c 1 0 0	yster alple	h Ta	<b>(open</b>	0 1 (1) (1) (1) (2) (1) (2) (2) (2) (2) (2) (2) (2) (2) (2) (2	outpu	ESIS	НУЗТЕЯ	0mV 2mV		
CP: Bit CHYS	es 4 es 1–3	1         1           efaante         1           configur         0           configur         0           configur         0           configur         0	C Activit Activit al C	high def <b>tault</b> ) Ir <b>âtatic</b> settinç	Compa rre able CHYS	0 0 1 9 <b>outp</b> show show 2 7 7 1 1 1 1	yster alple	h Ta	<b>(open</b>	0 1 (1) (1) 0 0 1	outpu	ESIS	нүзтек	0mV 2mV 4mV 6mV		
CP: Bit CHYS	es 4 es 1–3	1 efaaute ' configur e configur fie ifie 0 0	C Activit Activit al C	high def <b>tault</b> ) Ir <b>âtatic</b> settinç	Compa rre able CHYS	0 0 1 0 vutp resis. 0 show 2 7 7 1 0 0 1 1 1	yster alple	h Ta	<b>(open</b>	0 1 (1) (1) 0 0 1 0 0 0	outpu	ESIS	HYSTER	0mV 2mV 6mV 6mV 8mV		
CP: Bit CHYS	es 4 es 1–3	1         1           i         1           i         1           i         i           i         i           i         i           i         i           i         i           i         i           i         i           i         i           i         i           i         i           i         i           i         i           i         i           i         i	C Activit Activit al C	high def <b>tault</b> ) Ir <b>âtatic</b> settinç	Compa rre able CHYS	0 0 1 9 <b>outp</b> show show 2 7 7 1 1 1 1	yster alple	h Ta	<b>(open</b>	0 1 (1) (1) 0 0 1	outpu	ESIS	HYSTER	0mV 2mV 4mV 6mV		

defauntet values Shad(eld)

# featur**ta**tc**p**in Critical Configures CRL:

enabledætch 0 Bit

(default) Trantsparent

8.

# Critical DAC- Register (Critical Shunt Negative Voltage) 15h (Read/Write)

sianNo	negat( <b>sets</b> it	fullAstcaleonly)limit	255mV; range	8-bit. 1m+V: LSB
				(

тія	#	5	D1	D14	8	2 D1:	D12	D11	D10	6 <b>D</b>	8 <b>D</b>	D7	D6	D5	D4	D3	D2	D1	DO
BIT NAME		DP7	s c	CDP	P5	P4 CI	≥3 CE	P2 CDI	P1 CD	90 CE	ci	CF3	CF2	) CFI	з сға	22 WD	01 WE	o we	w
POR VALUE			0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### Desibitiptions

CDP:	Critical	settinigmit DAC-		
Bits	8– 15			
CF:	Configures	ut Comp <b>BA</b> stor	filter. outp	
Bits	Ranges 4–7	∰. 0.960ns; from	) listeadre settiΩl§s s√L	Ta <b>io</b> le
WD:	Configures	Out <b>piıt</b> Warning	0rfd/LSBscq0 from Delay	sec
Bits	Default 0–3	teadre settitvog 60.=	.9 Ta <b>im</b> le lis	

# Set@Host Table

CF3	CF2	CF1	СЕО	FILTER SETTING (2m)
0	0	0	0	0
0	0	0	1	0.064
0	0	1	0	0.128
0	0	1	1	0.192
0	1	0	0	0.256
0	1	0	1	0.320
0	1	1	0	0.384
0	1	1	1	0.448
1	0	0	0	0.512
1	0	0	1	0.576
1	0	1	0	0.640
1	0	1	1	0.704
1	1	0	0	0.768
1	1	0	1	0.832
1	1	1	0	0.896
1	1	1	1	0.960



Table 9. WD Settings						
WD3	WD2	WD1	WD0	SETTIN <b>G</b> ELAY		
0	0	0	0	0		
0	0	0	1	0.1		
0	0	1	0	0.2		
0	0	1	1	0.3		
0	1	0	0	0.4		
0	1	0	1	0.5		
0	1	1	0	0.6		
0	1	1	1	0.7		
1	0	0	0	8.0		
1	0	0	1	0.9		
1	0	1	0	1.0		
1	0	1	1	1.1		
1	1	0	0	1.2		
1	1	0	1	1.3		
1	1	1	0	1.4		
1	1	1	1	1.5		

### Calibration Register 16h (Read/Write)

Register. CalibretiforD1to D15bitsby set are Current calibratioonweemd usedioits D0 bit that Note corretaptondscurretime sets acros**s**rop calc**uldeiti**on. registentis fubh-stocale Full-scaleuthte currement LSB the and measuppermeentd range depend enterevaluteneon registesn the See Programming Measured INA 2009 section.*Engine* suitsable registernis system over all usefor calibration. valuesPOR the that Note def**all**ultare

тія	#	5	D1	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	(1) <b>D0</b>
BIT NAME		514	13 FS	2 FS	1 FS1	10 FS	i FS	FS	r FS8	i FS	5 FSG	FS:	s FS4	FS:	I FS2	) FS	s fsi	гя
POR VALUE			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D1ib5:D1.storedvalubenies CALDENBRATIK£0N writete possiolebelt '0'.be alwawyikal andbit *voaid*is D0 (1)

# PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
INA209AIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
INA209AIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

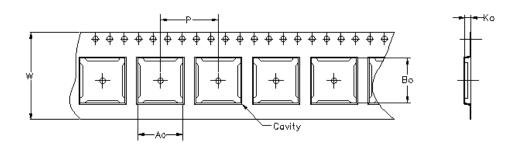
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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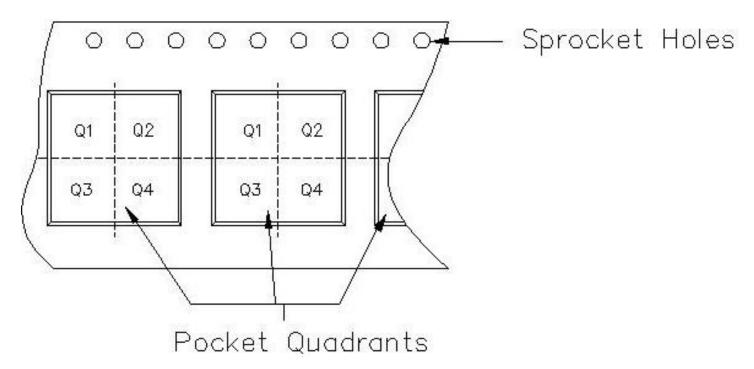


13-Jun-2007



Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



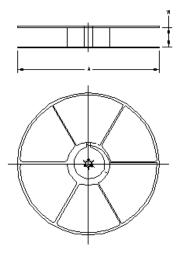
TAPE AND REEL INFORMATION

# PACKAGE MATERIALS INFORMATION



13-Jun-2007

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA209AIPWR	PW	16	MLA	330	12	7.0	5.6	1.6	8	12	Q1



# TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
INA209AIPWR	PW	16	MLA	346.0	346.0	29.0
					HEXAT	r

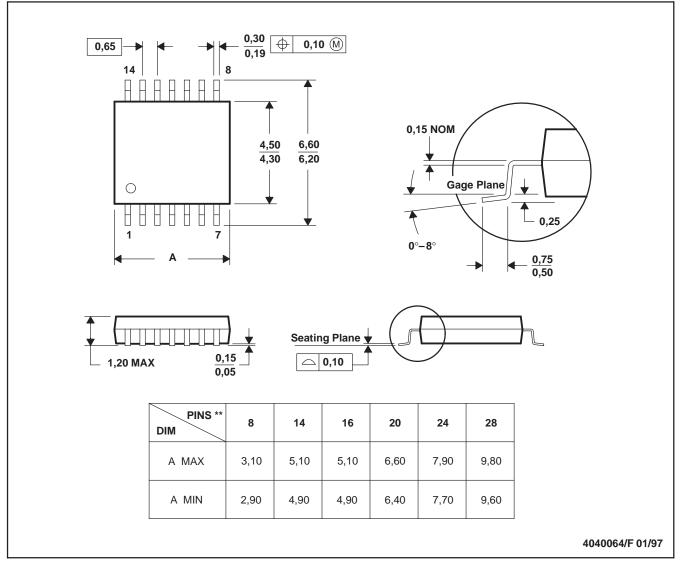
# **MECHANICAL DATA**

MTSS001C - JANUARY 1995 - REVISED FEBRUARY 1999

# PW (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



#### ΝΟΤΙCE ΙΜΡΟRΤΑΝΤ

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