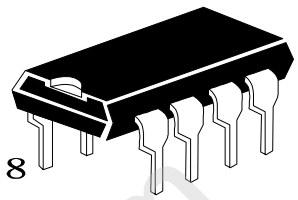
CMOS timer with RAM and I²C-bus control.

INA8583N

INA8583N is a timer with RAM and I²C-bus control. Designed for use in appliances having I²C-bus as clock/calendar/timer/alarm/events counter for turning on functions of the appliance at preset time or upon completion of an event. To be used in audio and appliances.



T_A = -20° To 70° C

Features:

- I²C- bus interface operating supply voltage: 2.5 V to 6 V;
- Clock operating supply voltage (0÷70°C): 1.0 V to 6 V;
- Operating current (at f_{SCL} = 0Hz): 50 µA;
- Clock function with four year calendar;
- 24 or 12 hour format;
- 32.768 kHz or 50Hz time base;
- Serial bus (I²C);
- Automatic word address in crementation;
- Programmable alarm, timer and interrupt function;
- Operating temperature range: -20 to +70 °C.
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Table1 – PIN ASSIGNMENT

	Pin	
OSCI	1	Generator input, 50Hz or occurrences
OSCO	2	Generator output
A0	3	Address input
GND	4	GND
SDA	5	Data for I²C-bus
SCL	6	Clock pulses for I²C-bus
INT	7	Open-drain interrupt output
Vcc	8	Supply voltage

Pinning diagram

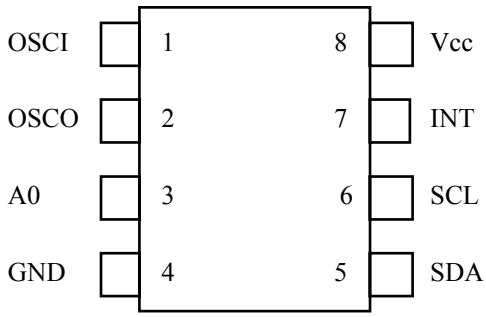

Fig.1

Block diagram INA8583N

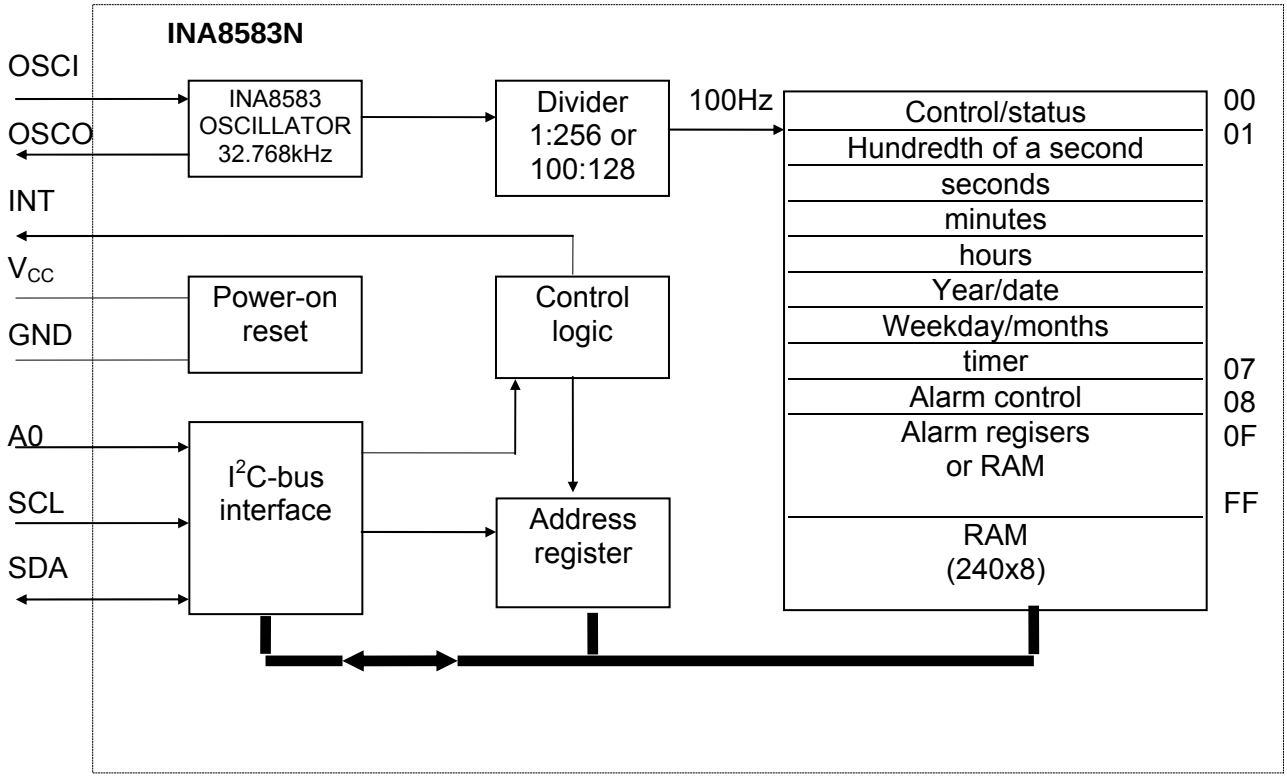

Fig. 2.

Table 2 – Recommend-operating conditions

Parameter Symbol Unit	Limits		Note
	Not more	Not less	
Supply voltage, Vcc, V			
■ operating	2.5	6.0	
■ clock	1.0	6.0	T_{amb}=0÷+70°C
Low input voltage, Vil, V	0	0.3*Vcc	
High input voltage, Vih, V	0.7*Vcc	Vcc	
Operating ambient temperature, Tamb, °C	-20	+70	
Input frequency, f_I, MHz		1	Only for event mode

Table3 – Absolute maximum rating

Parameter Symbol Unit	Limits		Note
	Not more	Not less	
Supply voltage, Vcc, V	-0.8	7,0	
Input voltage for all inputs, V_I, V	-0.8	Vcc+0.8	Note1
Max output current, Io, mA		10	
Max input current, I_I, mA		10	
Current through inputs 04 or 08, I_{DD}, I_{SS}, mA		50	
Power dissipation on package, P_{TOT}, mW		300	
Power dissipation on output , P_O, mW		50	
Storage temperature, Tstg, °C	-65	+150	

Notes:

1. If voltage on diode is higher than V_{CC} or lower than GND, the current will flow, the current should be not more than ±0.5mA.

Table 4 – Electrical parameters.

Parameter, Symbol unit	Limit Not less	 Not more	Testing conditions	Temperature, °C
Supply				
Supply current ,Icc, µA		200	Vcc=6V F_{SCL}= 100kHz	T=-20 +25 +70
Supply current for clock, I_{CC0}, µA		50	Vcc=5V	
		10	Vcc=1V	
Data storage supply current, I_{CCR}, µA		5	Note 1 V_{CC}= 1V	
		2	V_{CC}= 1V	
I^2C-bus enable level, V_{POR}, V	1.5	2.3	Note 2	
Input/output SDA				
Low output current, I_{OL}, mA	3		Vcc= 6 V Vol= 0.4 V	
Input leakage current, $\|I_I\|$, µA		1	Vcc= 6 V V_{IL}= 0 V V_{IH}= 6 V	
SCL, SDA				
Input capacity, C_I,pF		7	V_I=0 V	
Inputs A0, OSCI				
Input leakage current, $\|I_I\|$, nA		250	Vcc= 6 V V_{IL}= 0 V V_{IH}= 6 V	
Output INT				
Output low current, I_{OL}, mA	3		Vcc=6.0 V V_{OL}=0,4 V	
Input leakage current, $\|I_I\|$, µA		1	Vcc= 6 V V_{IL}= 0 V V_{IH}= 6 V	

Notes:
1. For event mode or 50Hz only.
2. The I^2C-bus logic is disabled if $V_{CC} < V_{POR}$.

INA8583N contains 256x8 RAM 8-bit. The word address register which is incremented automatically, built-in 32.768 kHz oscillator circuit, frequency divider, interface of two line bi-directional serial I^2C-bus and power-on reset circuit.

The first 8 bits of the RAM (addresses 00÷07) are designated ass addressable 8-bit parallel registers. The first register (address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory address 08÷0F may be used as free RAM locations or may be programmed as alarm registers.

The following modes can be selected by setting the control/status register:

- Clock mode from 32.768 kHz;
- Clock mode from 50 Hz;
- Event counter mode.

In the clock mode hundredths of a second, seconds, minutes, hours, date, month (four-year calendar) and a weekday are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used for counting pulses applied to the oscillator input (OSCO left open-circuit). In BCD format the event counter stores up to 6 digits.

By setting the alarm enabling bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register the following may be programmed:

- Dated alarm;
- Weekday alarm;
- Daily alarm;
- Timer alarm.

In the clock mode the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set, and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set. The flags remain set until directly reset by a write operation to register (00 address).

When the alarm is disabled the remaining alarm registers (addresses 09÷0F) may be used as free RAM.

In the clock modes 24hr or 12hr format can be selected by setting the most significant bit of the hours counter register.

Register arrangement.

Control/status
Hundredth of second
seconds
minutes
hours
Year/date
Weekday/month
timer
Alarm control
Hundredth of second
Alarm seconds
Alarm minutes
Alarm hours
Alarm date
Alarm month
Alarm timer
Free RAM

Clock modes

Control/status		
D1	D0	01
D3	D2	02
D5	D4	03
free		04
free		05
free		06
timer T1	timer T0	07
Alarm control		08
alarm D1	alarm D0	09
D3	D2	0A
D5	D4	0B
free		0C
free		0D
free		0E
Alarm timer		0F
Free RAM		

Event counter

Fig. 3.

Table 5. – Cycle length of the time counters, clock modes.

Unit	Counting cycle	Carry to next unit	Contents of the month counter
Hundredths of a second	00 ÷ 99	99 to 00	
Seconds	00 ÷ 59	59 to 00	
Minutes	00 ÷ 59	59 to 00	
Hours (24 h)	00 ÷ 23	23 to 00	
Hours (12 h)	12AM, 01AM÷11AM, 12PM, 01PM÷11PM	11PM to 12AM	
Date	01÷31 01÷30 01÷29 01÷28	31 to 01 30 to 01 29 to 01 28 to 01	1, 3, 5, 7, 8, 10, 12 4, 6, 9, 11 2, year = 0 2, year = 1, 2, 3
Months	01÷21	12 to 01	
Year	0÷3	3 to 0	
Weekdays	0÷6	6 to 0	
Timer	00÷99	No carry	

The year and date are packed into memory location 05. The weekdays and months are packed into memory location 06. When reading these memory locations the year and weekdays may be masked out when the mask flag of the control/status register is set. This allows the user to read the date and month counters only.

In the event counter mode data are stored in BCD format. D5 is the most significant and do the least significant digit. In this mode the internal divider is by-passed.

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated. All functions of the alarm, timer and interrupt output are controlled by the contents of the alarm control register.

All alarm registers are arranged starting from 08 address.

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignored the month and date bits. When a weekday alarm is selected, for comparison a bit will be selected from the alarm register per the weekday (address OE) corresponding to the weekday on which the alarm is activated.

Interrupt output (with open drain) is programmed by setting the alarm control register. It enables (active LOW) when the alarm flag or timer flag are set. The voltage level in ON state (HIGH) on the interrupt output may be more than the supply voltage.

A 32.768 kHz quartz crystal may be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and supply is used for tuning the oscillator. A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50Hz reference frequency or an external high speed event signal into the input OSCI.

When power-up occurs the I^2C-bus interface, the control/status register and all clock counters are reset. After the device starts time-keeping in the 32.768kHz clock mode with the 24hr format on the square wave appears at the interrupt output pin (starts HIGH). This may be abolished by setting the alarm enable bit in the control/status register.

The 2^{nd} signal of interface of I^2C-bus is generated as soon as the supply voltage below the reset level of I^2C-bus interface. This reset signal does not affect the registers of hour counter and control/status register.

It the recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.

I^2C-bus is a bi-directional, two-line communication between different ICs and modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines shall be connected to a positive supply via a resistor since in IC these outputs have “open drain”. Data transfer may be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

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Bit transfer

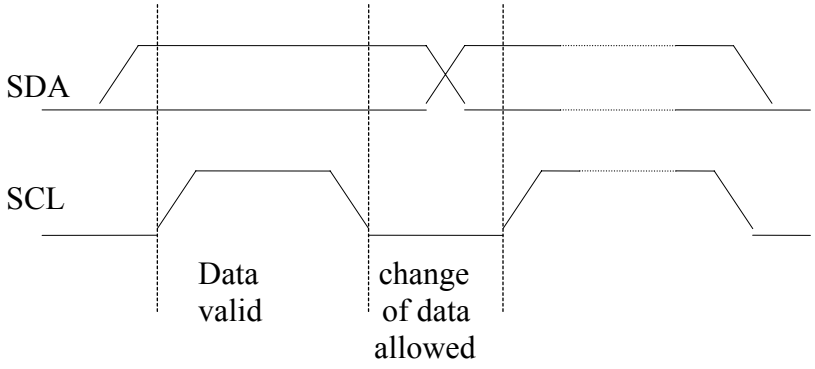


Fig. 4.

Both SDA and SCL lines remain HIGH when the bus is not busy. The HIGH-to-LOW transition of the data line, while the clock is High is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

Definition of start and stop conditions.

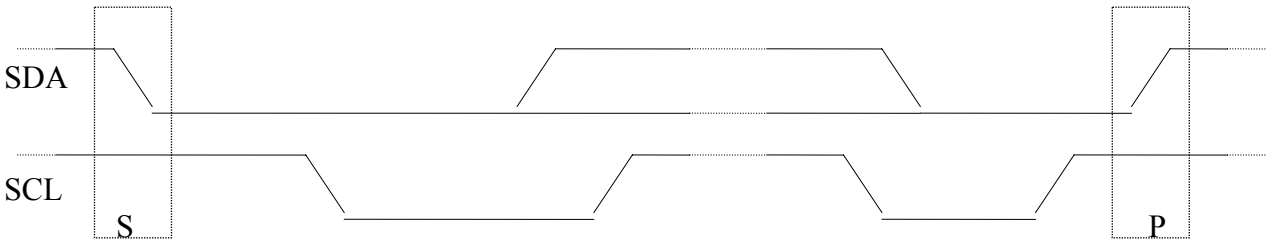


Fig. 5.

A device generating a message is a “transmitter” a device receiving a message is a “receiver”. The device that controls the message is the “master”, and the devices which are controlled by the master are “slaves”.

The number of data bytes transferred between the start and stop conditions from the transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit.

Acknowledgment on the I^2C-bus.

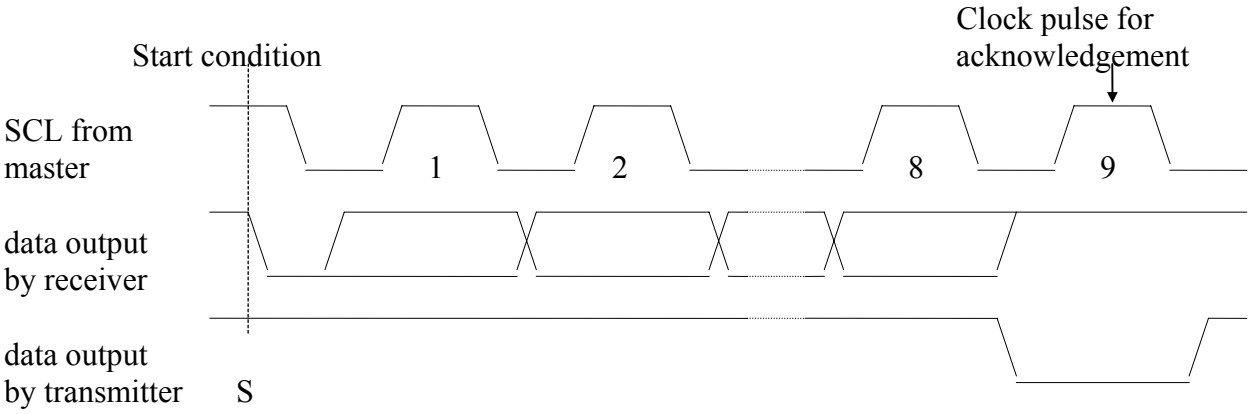


Fig. 6.

The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception oa each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse. A master receiver must signal an end of date to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

Before any date is transmitted on the I^2C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

Master transmits to slave receiver (WRITE) mode.

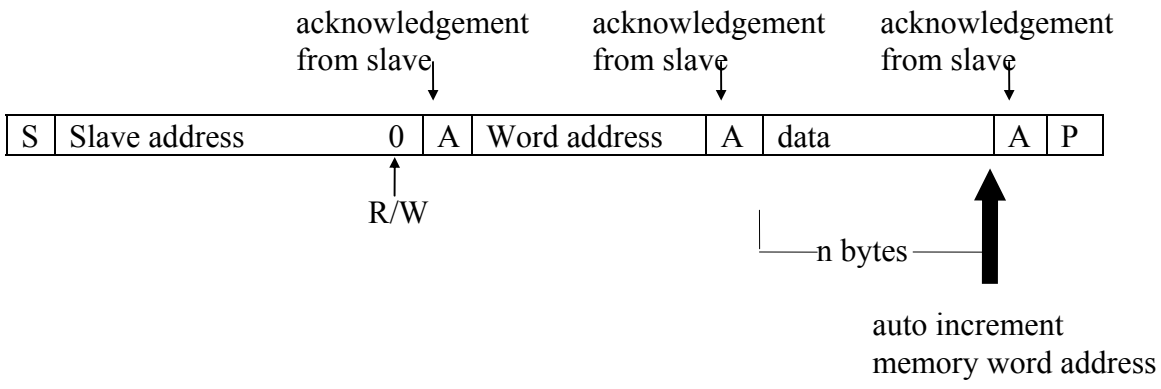


Fig. 7.

Master reads after setting word address (write word address; READ data).

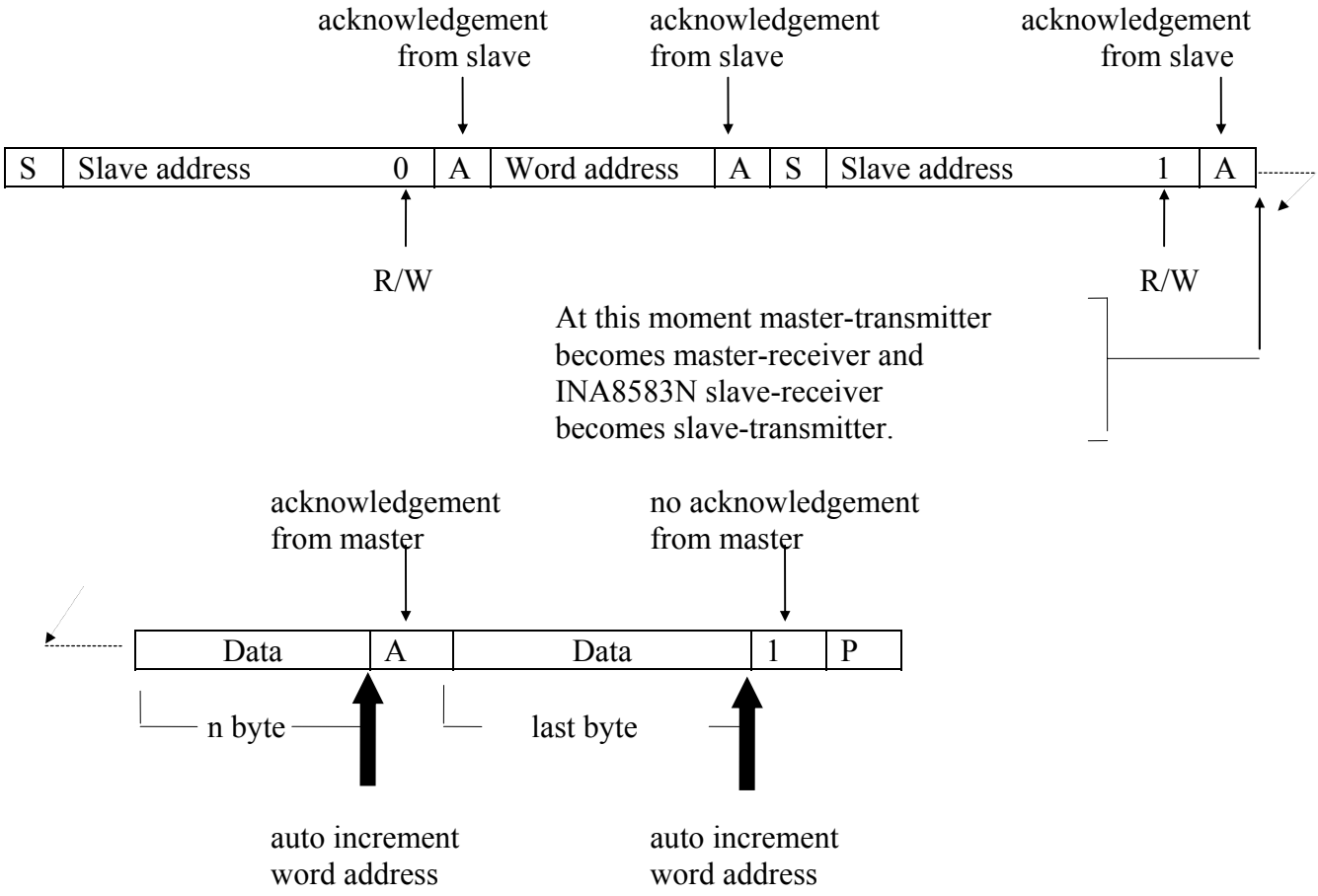


Fig. 8.

Master reads slave immediately after first byte (READ mode).

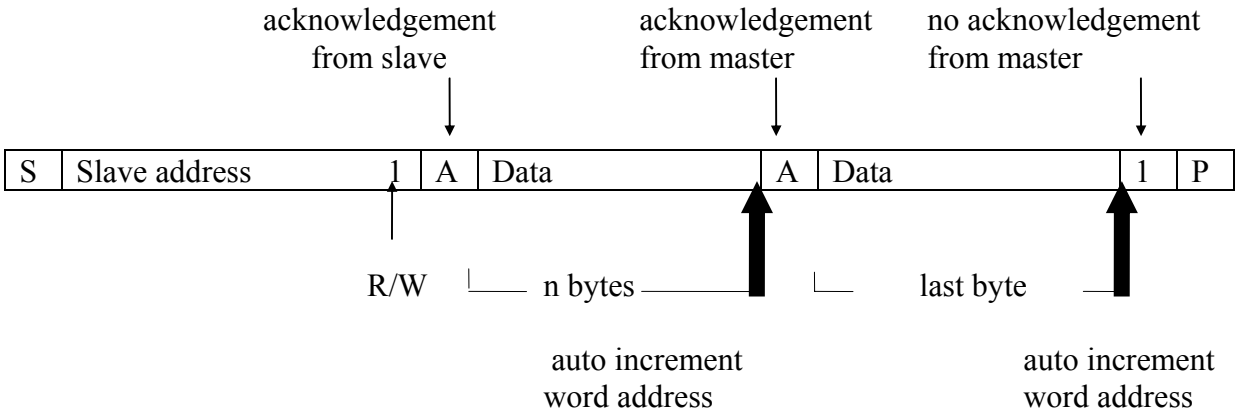


Fig. 9.

Application circuit

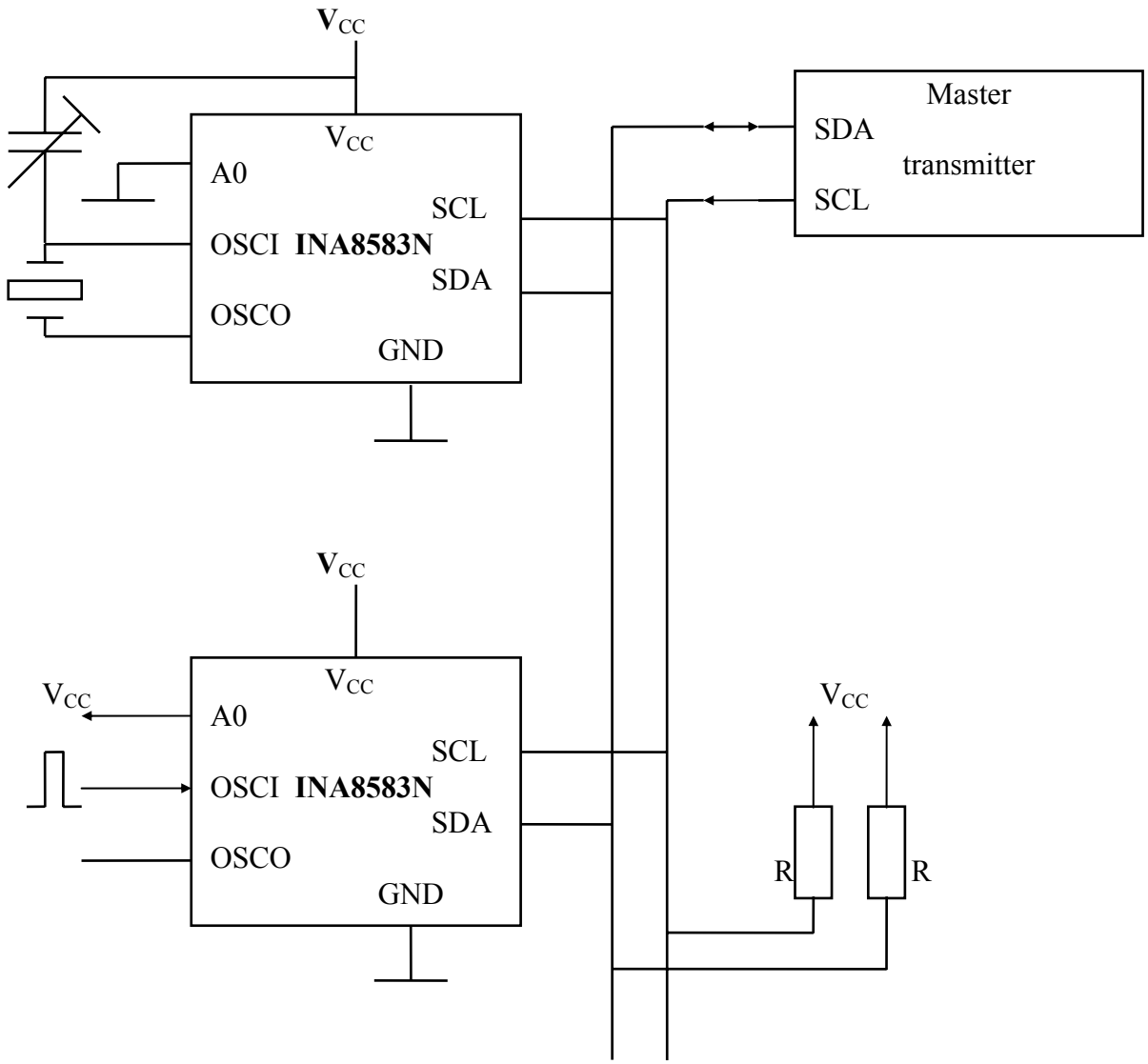


Fig.10

Table 6 – Symbols

Symbol	Description
S	START condition
P	STOP condition
A	Bit acknowledge

INA8583N address

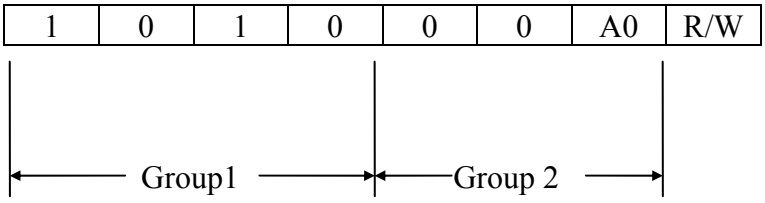
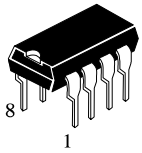
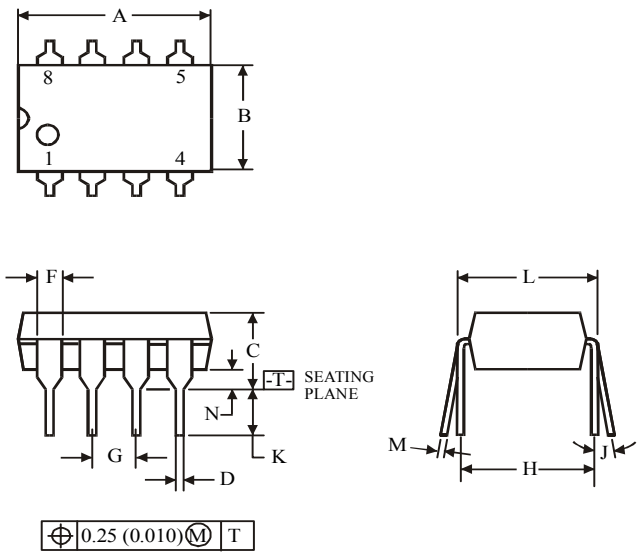


Fig. 11.

N SUFFIX PLASTIC DIP
(MS – 001BA)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.