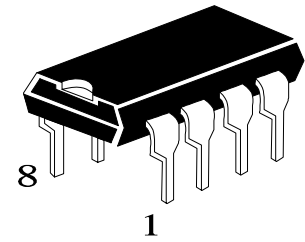


INF85116

2048 x 8 -Bit CMOS EEPROM with I²C-bus interface

The INF85116N is an 16-Kbits (2048 x 8-bit) floating gate Electrically Erasable Programmable Read Only Memory (EEPROM). Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier. As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Only one INF85116N device is required to support all eight blocks of 256 x 8-bit each.



FEATURES

- Low power CMOS
 - maximum active current 1.0 mA
 - maximum standby current 10 μ A (at 5.5 V), typical 4 μ A
- Non-volatile storage of 16-Kbits organized as eight blocks of 256x8-bits during 20 years (at 55°C)
- Single supply ($U_{cc}=2,7 \div 5,5$ V);
- Automatically increased word's address
- On-chip voltage multiplier
- Serial input/output I²C-bus
- 1000000 ERASE/WRITE cycles per byte
- Internal timer for writing (no external components)
- Write operations: multi byte write mode to 32 bytes
- Write - protection input
- Power-on-reset

Temperature range: -40°C \div +85°C

PIN DESCRIPTION

| Symbol | Pin | Description |
|-----------------|-----|--|
| n. c. | 1 | not connected |
| n. c. | 2 | not connected |
| n. c. | 3 | not connected |
| U _{ss} | 4 | negative supply voltage |
| SDA | 5 | serial data input/output (I ² C-bus) |
| SCL | 6 | serial clock input (I ² C-bus) |
| WP | 7 | write - protection input |
| U _{cc} | 8 | positive supply voltage |

PIN CONFIGURATION

| | | | |
|-----------------|---|---|-----------------|
| n. c. | 1 | 8 | U _{cc} |
| n. c. | 2 | 7 | WP |
| n. c. | 3 | 6 | SCL |
| U _{ss} | 4 | 5 | SDA |

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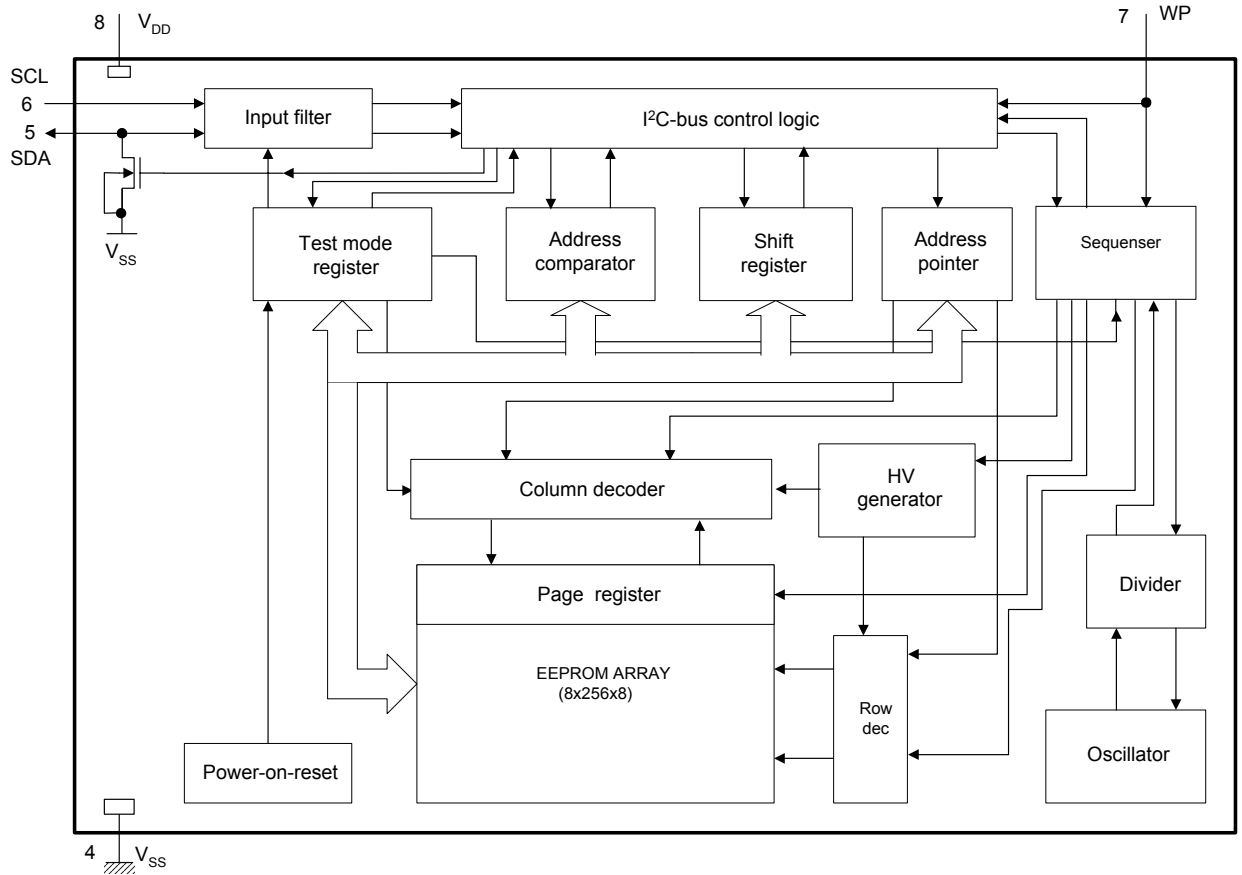
Table 1. Quick reference data

| Symbol | Parameter | min | max | Unit |
|--------|-----------|-----|-----|------|
|--------|-----------|-----|-----|------|



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| | | | | |
|-----------|-------------------------------|-----|-----|----|
| U_{DD} | Supply voltage | 2.7 | 5.5 | V |
| I_{OL} | LOW level output current | - | 6 | mA |
| T_{amb} | Operating ambient temperature | -40 | +85 | °C |

BLOCK DIAGRAM**Table 2. Limiting values**

| Symbol | Parameter | min | max | Unit |
|-----------|--|------|------|------|
| U_{DD} | Supply voltage | -0.3 | 6.5 | V |
| U_i | Input voltage on any pin $ Z_i > 500 \Omega$ | -0.8 | 6.5 | V |
| i_i | Input current on any pin | - | 1 | mA |
| i_o | Output current | - | 10 | mA |
| T_{stg} | Storage temperature | -65 | +150 | °C |



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Table 3. Characteristics

| Symbol | Parameter | Conditions | min | max | Unit |
|---------------------------------|--|--|----------------|--------------|---------|
| $I_{DD(stb)}$ | Standby supply current | $U_{DD} = 2.7V$ | - | 6 | μA |
| | | $U_{DD} = 5.5V$ | | 10 | μA |
| I_{CCR} | Supply current READ | $f_{SCL}=400kHz,$ $U_{DD} = 5.5V$ | - | 1 | mA |
| I_{CCW} | Supply current E / W | $f_{SCL}=400kHz,$ $U_{DD} = 5.5V$ | - | 1 | mA |
| WP input (pin 7) | | | | | |
| U_{IL} | LOW level input voltage | | -0.8 | $+0.1U_{DD}$ | V |
| U_{IH} | HIGH level input voltage | | $0.9U_{DD}$ | $U_{DD}+0.8$ | V |
| SCL input (pin 6) | | | | | |
| U_{IL} | LOW level input voltage | | -0.8 | $+0.3U_{DD}$ | V |
| U_{IH} | HIGH level input voltage | | $0.7U_{DD}$ | 6.5 | V |
| I_{LI} | Input leakage current | $U_i=U_{DD}$ or U_{SS} | - | ± 1 | μA |
| f_{SCL} | Clock input frequency | | 0 | 400 | kHz |
| t_{sp} | Pulse width of spikes suppressed by filter | | 0 | 100 | ns |
| C_1 | Input capacitance | $U_i= U_{SS}$ | - | 7 | pF |
| SDA input/output (pin 5) | | | | | |
| U_{IL} | LOW level input voltage | | -0.8 | $0.3U_{DD}$ | V |
| U_{IH} | HIGH level input voltage | | $0.7U_{DD}$ | 6.5 | V |
| U_{OL1} U_{OL2} | LOW level output voltage | $I_{OL}=3mA,$ $U_{DD} = U_{DD (min)}$ $I_{OL}=6mA,$ $U_{DD} = U_{DD (min)}$ | - | 0.4 0.6 | V |
| I_{LO} | Output leakage current | $U_{OH}=U_{DD}$ | - | 1 | μA |
| $t_{O(F)}$ | Output fall time from U_{IHmin} to U_{ILmax} | with up to 3mA sink current at U_{OL1} | $20+0.1 C_B^*$ | 250 | ns |
| | | with up to 6mA sink current at U_{OL2} | $20+0.1 C_B$ | 250 | ns |
| t_{SP} | Pulse width of spikes suppressed by filter | | 0 | 100 | ns |
| C_1 | Input capacitance | $U_i=0V$ | - | 10 | pF |
| $t_{E/W}$ | E/W cycle time | | - | 10 | ms |
| $N_{E/W}$ | E/W cycle per byte | $T_{amb} = (-40+85) ^\circ C,$ | 100000 | - | |
| | | $T_{amb} = 22^\circ C$ | 1000000 | | |
| t_S | Data retention time | $T_{amb} = 55^\circ C$ | 20 | - | years |

* - The bus capacitance ranges from 10 to 400pF (C_B = total capacitance of one bus line in pF)



INF85116**Table 4. I²C-bus characteristics**

| Symbol | Parameter | Condi- tions | Standard mode | | Fast mode | | Unit |
|----------------------|--|-----------------|------------------|------|--------------------------------------|-----|------|
| | | | min | max | min | max | |
| f _{SCL} | Clock frequency | | 0 | 100 | 0 | 400 | kHz |
| t _{BUF} | Time the bus must be free before | - | 4.7 | - | 1.3 | - | μs |
| t _{HD, STA} | START condition hold time after which first clock pulse is generated | - | 4.0 | - | 0.6 | - | μs |
| t _{LOW} | LOW level clock period | - | 4.7 | - | 1.3 | - | μs |
| t _{HIGH} | HIGH level clock period | - | 4.0 | - | 0.6 | - | μs |
| t _{SU, STA} | Set-up time for START condition | repeated start | 4.7 | - | 0.6 | - | μs |
| t _{HD, DAT} | Data hold time for CBUS compatible masters | - | 5 | - | - | - | μs |
| t _{HD, DAT} | Data hold time for I ² C - bus devices | note 1 | 0 | - | 0 | - | ns |
| t _{SU, DAT} | Data set-up time | - | 250 | - | 100 | - | ns |
| t _R | SDA and SCL rise time | - | - | 1000 | 20+0.1 C _b ⁽²⁾ | 300 | ns |
| t _F | SDA and SCL fall time | - | - | 300 | 20+0.1 C _b ⁽²⁾ | 300 | ns |
| t _{SU, STO} | Set-up time for STOP condition | - | 4.0 | - | 0.6 | - | μs |

Notes:

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.
2. C_b = total capacitance of one bus line in pF.

