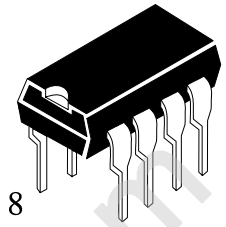
INF8594E

512 x 8-bit CMOS EEPROMS with I²C-bus Interface



INF8594E Plastic DIP
T_A = -40° to 85°C

The INF8594E is a 4-Kbit (512 x 8-bit) floating gate electrically erasable programmable read only memory (EEPPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage 1s generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to four INF8594E devices may be connected to the I²C-bus. Chip select is accomplished by two address inputs.

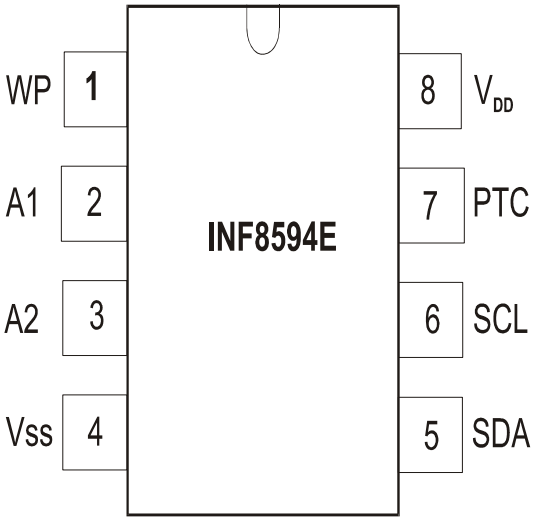
Timing of the Erase/Write cycle is done internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock or timing the length of an Erase/Write cycle.

A write protection input (pin 1) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 256 EEPROM cells is addressed, then the data bytes will not be acknowledged by the INF8594E and the EEPROM contents are not changed.

PIN ASSIGNMENT

- Low Power CMOS
  maximum active current 2.5 mA
- maximum standby current 10 µA
- Non-volatile storage of 4-Kbits organized as two pages each 256 x 8-bits
- Only one power supply required
- On-chip voltage multiplier
- Serial input/output bus (I²C)
- Write operations
  byte write mode
  8.byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  sequential read
  random read
- .Extended supply voltage range (2,5 to 6.0 V).
- Internal timer for writing (no external components)
- .Power-on reset
- .High reliability by using a redundant storage code (single bit error correction)
- .Endurance
  100 k. Tamb = 85 °C
- 10 years non-volatile data retention time
- Pin and Address compatible to
  INF8594E Family and PCx8598X2 Family



ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
INF8594E	8	DIP	plastic	SOT97

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Positive supply voltage		2.5	6.0	V
I_{DDR}	Supply current READ	f_{SCL}= 100 kHz V_{DD}= 3V V_{DD}= 6V	 - -	 60 200	 µA µA
I_{DDW}	Supply current ERASE/WRITE	f_{SCL}= 100 kHz V_{DD}= 3V V_{DD}= 6V	 - -	 0.8 2.5	 mA mA
I_{DDO}	Supply current STANDBY	V_{DD}= 3V V_{DD}= 6V	- -	3.5 10	µA µA

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	positive supply voltage		-0.3	+7.0	V
V_I	voltage on any input pin	$IZ_II > 500\ \Omega$	V_{SS}-0.8	V_{DD}+0.8	V
I_I	current on any input pin	-	-	1	mA
I_O	output current	-	-	10	mA
T_{stg}	storage temperature range		-65	+150	°C
T_{amb}	ambient operating temperature range INF8594E		-40	+40	°C

CHARACTERISTICS

INF8594E: V_{DD} =4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 to +85°C

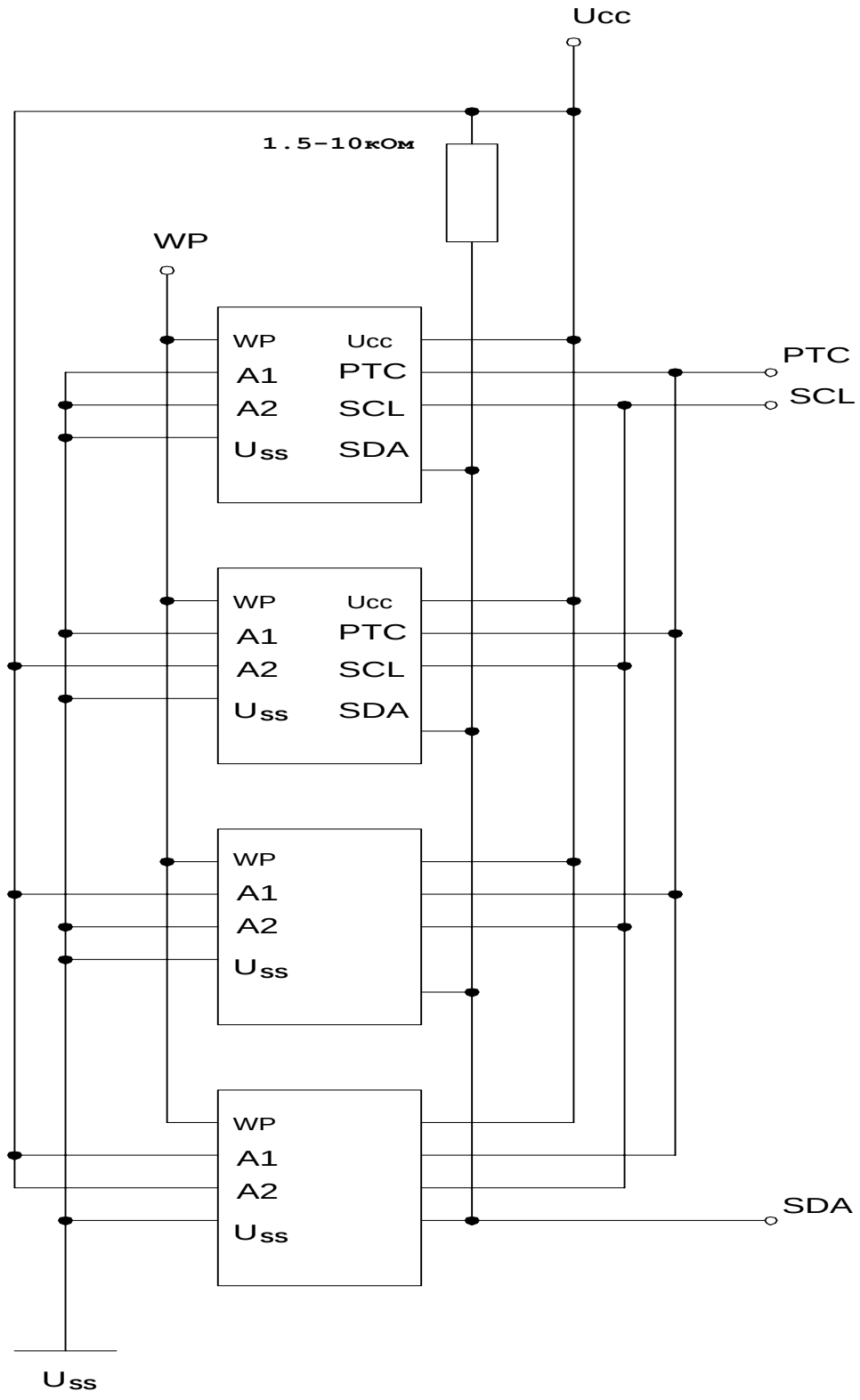
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Supply					
V_{DD}	positive supply voltage PCF8594E		 4.5	 5.5	 V
I_{DDR}	supply current READ INF8594E	f_{SCL} = 100 kHz $V_{DD(max)}$	 -	 200	 µA
I_{DDW}	supply current ERASE/WRITE INF8594E	f_{SCL} = 100 kHz $V_{DD(max)}$	 -	 2.5	 mA
I_{DDO}	supply current STANDY INF8594E	 $V_{DD(max)}$	 -	 10	 µA
PTC Input					
V_{IL} V_{IH}	LOW level input voltage HIGH level input voltage		-0.8 $0.9V_{DD}$	$0.1V_{DD}$ V_{DD}+0.8	V V
SCL Input					
V_{IL} V_{IH} I_{LI} f_{SCL} C_I	LOW level input voltage HIGH level input voltage input leakage current clock frequency input capacitance	 $V_I = V_{DD}$ or V_{SS} $V_I = V_{SS}$	-0.8 $0.7V_{DD}$ - 0 -	$0.3V_{DD}$ V_{DD}+0.8 ±1 100 7	V V µA kHz pF
SDA Input/Output					
V_{IL} V_{IH} I_{LI} f_{SCL} C_I	LOW level input voltage HIGH level input voltage input leakage current clock frequency input capacitance	 I_{OH} = 3 mA; $V_{DD(min)}$ $V_{OH} = V_{DD}$ $V_I = V_{SS}$	-0.8 $0.7V_{DD}$ - - -	$0.3V_{DD}$ V_{DD}+0.8 0.4 1 7	V V V µA pF
Data retention time					
t_S	data region time	T_{amb} = 55 °C	10	-	yrs

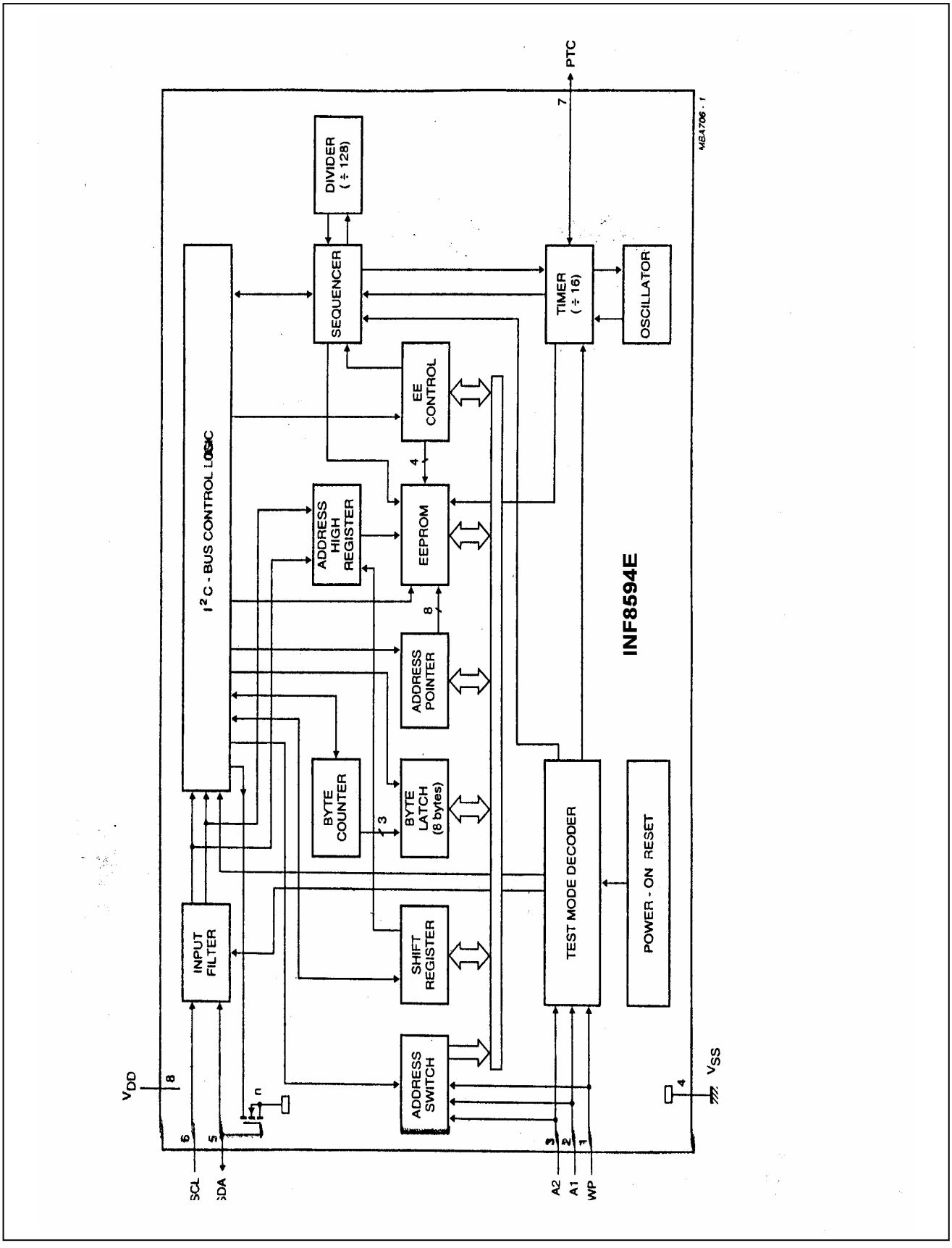
WRITE CYCLE LIMITS

The power-on reset circuit resets the I^2C-bus logic with a set-up time ≤ 10 µA.
Selection of chip address is achieved by connecting the A1 and A2 inputs to either V_{SS} or V_{DD}.

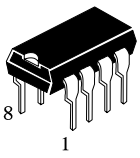
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
		Supply				
t_{SW}	ERASE/WRITE cycle time internal oscillator external clock		 - 4	 7 -	 - 10	 ms ms
		Endurance				
N_{SW}	ERASE/WRITE cycles per byte INF8594E	T_{amb} = -40 to +85°C $t_{E/W}$ = 4 to 10 ms T_{amb} = 22°C; $t_{E/W}$ = 5ms	- -	- -	10 000 100 000	
		Programming				
f_P	programming frequency		25	-	60	kHz
t_{IL}	LOW time		5	-	-	µs
t_{HIGH}	HIGH time		5	-	-	µs
t_r	rise time		-	-	300	ns
t_f	fall time		-	-	300	ns
t_d	delay time		0	-	t_{LOW}	µs

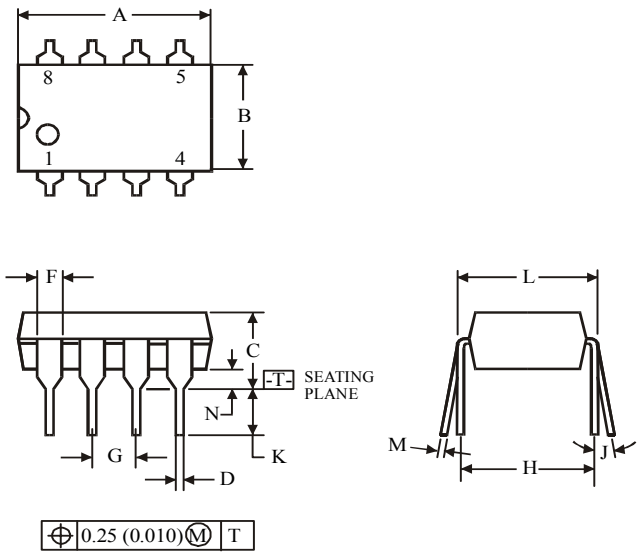
LOGIC DIAGRAMM




PTC
7
MEA706 - 1
DIVIDER (÷ 128)
SEQUENCER
TIMER (÷ 16)
OSCILLATOR
EE CONTROL
4
ADDRESS HIGH REGISTER
EEPROM
I²C - BUS CONTROL LOGIC
8
ADDRESS POINTER
INF8594E
BYTE COUNTER
3
BYTE LATCH (8 bytes)
INPUT FILTER
SHIFT REGISTER
TEST MODE DECODER
POWER - ON RESET
ADDRESS SWITCH
VDD
8
VSS
4
6
5
SCL
SDA
3
2
1
A2
A1
WP

N SUFFIX PLASTIC DIP
(MS – 001BA)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.