To Customer： _____

# Realtime Clock Module

## INS5A8900

# Datasheet

Document Version 1.0

Released on February 17, 2023

## Ordering Information

| Manufacture Part Number | Product Name | Description |
|---|---|---|
| INS5A8900CA | INS5A8900 | ±5ppm @ -40℃~+90℃<br>±20ppm@ +90℃~+105℃ |
|  |  |  |
|  |  |  |

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# INS5A8900 —Automotive High Accuracy I$^2$C RTC

## Key Features

- Low current consumption: 1.3uA(Typ.)

- High stability:ss

    ±5ppm @ -40℃~+90℃

    ±20ppm@ +90℃~+105℃

- Build-in TCXO: 32.768KHz

- Build-in temperature sensor

- Communication Interface: I$^2$C bus

- Power Supply Voltage: 1.6V~5.5V

- Operation Temperature Range: -40℃ ~ +105℃

- Leap years autocorrection

- Backup battery switchover function

- Timer output function with adjustable period

- Size:3.2mm × 2.5mm × 0.9mm

- AEC-Q100 Compliant

## Block Diagram
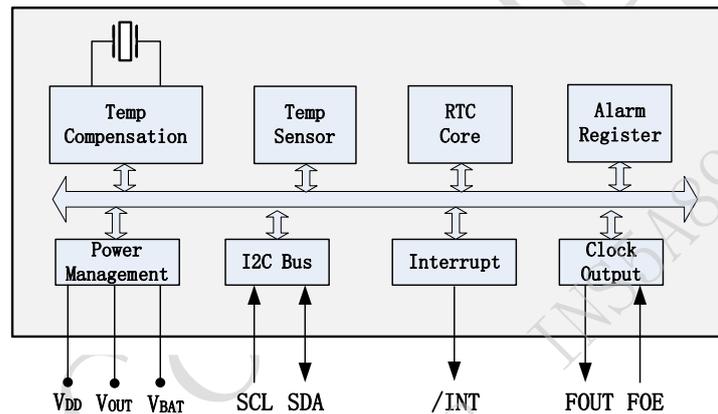


## Overview

INS5A8900 is a high-accuracy I$^2$C bus interface real-time clock with low power consumption. It embeds a 32.768KHz TCXO. The high precise temperature sensor and temperature compensated circuit ensure the high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. The SMD3225 package with only 0.9mm thickness and AEC-Q100 compliant makes it suitable for automotive applications.

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## Revision History

| Version | Change Contents | Prepared by | Revised Date |
|---------|-----------------|-------------|--------------|
| V1.0 | First Issued | | 2023.02.17 |
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# 1 Pin definition

INS5A8900

1. FOE          10. /INT
2. $V_{DD}$      9. GND
3. $V_{BAT}$    8. $V_{OUT}$
4. FOUT         7. SDA
5. SCL          6. T1
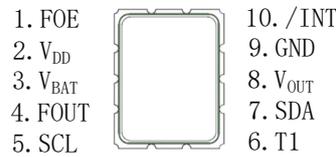
**Table1. Pin Definition**

| Pin Number | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | FOE | In | FOUT output control pin. "1" - enable FOUT, "0"- FOUT Hi-Z |
| 2 | $V_{DD}$ | - | Power supply |
| 3 | $V_{BAT}$ | - | Backup battery pin. Connect to large-capacity capacitors or a backup battery. Connect to $V_{DD}$ when switchover function is not necessary |
| 4 | FOUT | Out | Frequency output. Controlled by FOE. Frequency can be set by FSEL bits. |
| 5 | SCL | In | I²C clock signal |
| 6 | T1 | - | Manufacturer test only.   Ensure to be floating |
| 7 | SDA | In/Out | I²C data signal |
| 8 | $V_{OUT}$ | - | Internal voltage output pin. A 1.0uF capacitor to Ground is needed for backup switchover application. * |
| 9 | GND | - | Ground |
| 10 | /INT | Out | Interrupt Output, Open-Drain |

*Note: For backup switchover application, must connect a 1.0uF capacitor between VOUT pin and GND pin.

# 2 Electrical Characteristics

## 2.1 Absolute Maximum Ratings

**Table2. Absolute Maximum Ratings**

| Parameter | Symbol | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power Supply Voltage | $V_{DD}$ | -0.3 | | 6.5 | V | |
| Backup Battery Voltage | $V_{BAT}$ | -0.3 | | 6.5 | V | |
| Input Voltage | $V_{IN}$ | GND-0.3 | | 6.5 | V | FOE, SCL, SDA |
| Clock Output Voltage | $V_{OUT1}$ | GND-0.3 | | $V_{DD}$+0.3 | V | FOUT |
| Output Voltage | $V_{OUT2}$ | GND-0.3 | | 6.5 | V | SDA, /INT |
| Storage temperature | $T_{STG}$ | -55 | | 125 | °C | |

## 2.2 Recommended Operating Conditions

**Table3. Recommended Operating Conditions**

| Parameter | Symbol | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power Supply Voltage (normal mode) | $V_{DD}$ | 2.5 | 3.0 | 5.5 | V | |
| Power Supply Voltage In case of single supply ($V_{DD} = V_{BAT}$) | $V_{DD}$ | 1.6 | 3.0 | 5.5 | V | |
| Backup Battery | $V_{BAT}$ | 1.6 | 3.0 | 5.5 | V | |
| Current consumption | $I_{DD}$ | | 1.3 | | uA | Using Battery supply only, @25℃ |
| Operation temperature | $T_{OPR}$ | -40 | 25 | 105 | °C | |

Note:

1. During the power on and oscillation starting time, a voltage of more than 2.5V must be provided to ensure the oscillation circuit to a stable state.

2. After the power supply is removed or power off, ensure that VDD=GND for more than 10 seconds before next power on cycle.

3. If there is no special indication, the test conditions are GND =0V, VDD=1.6V~5.5V, Ta=-40°C~+105°C

## 2.3 Frequency Characteristics

**Table4. Frequency Characteristics**

| Parameter | Symbol | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Frequency stability | $\Delta f/f$ | -5 | | +5 | ppm | -40°C ~ +90°C |
| | | -20 | | +20 | ppm | +90°C~+105°C |
| Oscillation start time | $t_{STA}$ | | | 1 | s | @25℃ |
| Year Aging | $f_a$ | -5 | | +5 | ppm | @25℃, First year |
| Temperature Sensor Accuracy | $T_{emp}$ | -5 | | +5 | °C | VDD=3.0V |

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| Parameter | Symbol | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FOUT duty cycle | $t_{w/t}$ | 40 | 50 | 60 | % | |

Note：If there is no special indication, the test conditions are GND = 0V, VDD = Vbat = 2.5V ~ 5.5V, Ta = -40℃~+105℃

## 2.4 DC Characteristics

**Table5. DC Characteristics**

| Parameter | Symbol | Value | | | Unit | Notes | |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Average Current consumption1 | $I_{DD1}$ | | 1.4 | 50 | uA | $V_{DD}$=5.0V | $f_{SCL}$=0Hz, FOE=GND, /INT = VDD; VDD=VBAT; FOUT off (High-Z); Compensation interval 2s; VDD voltage detection time 2ms |
| Average Current consumption2 | $I_{DD2}$ | | 1.3 | 45 | | $V_{DD}$=3.0V | |
| Average Current consumption3 | $I_{DD3}$ | | 4.5 | 50 | uA | $V_{DD}$=5.0V | $f_{SCL}$=0Hz, FOE=$V_{DD}$, /INT = $V_{DD}$; $V_{DD}$=$V_{BAT}$; FOUT:32.768kHz, CL=0pF; Compensation interval 2s; $V_{DD}$ voltage detection time 2ms |
| Average Current consumption4 | $I_{DD4}$ | | 2.5 | 45 | | $V_{DD}$=3.0V | |
| High-level input voltage | $V_{IH}$ | 0.8*$V_{DD}$ | | 5.5 | V | SCL, SDA, FOE pin | |
| Low-level input voltage | $V_{IL}$ | GND-0.3 | | 0.2*$V_{DD}$ | V | | |
| High-level output voltage | $V_{OH1}$ | 4.0 | | 5.0 | V | $V_{DD}$=5.0V, $I_{OH}$ = -1mA | FOUT pin |
| | $V_{OH2}$ | 2.2 | | 3.0 | | $V_{DD}$=3.0V, $I_{OH}$ = -1mA | |
| | $V_{OH3}$ | 2.9 | | 3.0 | | $V_{DD}$=3.0V, $I_{OH}$ = -100uA | |
| Low-level output voltage | $V_{OL1}$ | GND | | GND+0.5 | V | $V_{DD}$=5.0V, $I_{OL}$ = 1mA | FOUT pin |
| | $V_{OL2}$ | GND | | GND+0.8 | | $V_{DD}$=3.0V, $I_{OL}$ = 1mA | |
| | $V_{OL3}$ | GND | | GND+0.1 | | $V_{DD}$=3.0V, $I_{OL}$ = 100uA | |
| | $V_{OL4}$ | GND | | GND+0.25 | V | $V_{DD}$=5.0V, $I_{OL}$ = 1mA | /INT pin |
| | $V_{OL5}$ | GND | | GND+0.4 | | $V_{DD}$=3.0V, $I_{OL}$ = 1mA | |
| | $V_{OL6}$ | GND | | GND+0.4 | V | $V_{DD}$≥3.0V, $I_{OL}$ = 3mA | SDA pin |
| Input leakage current | $I_{LK}$ | -0.5 | | 0.5 | uA | FOE, SDA, SCL pin, $V_{IN}$ = $V_{DD}$ or GND | |
| Output leakage current | $I_{OZ}$ | -0.5 | | 0.5 | uA | FOUT, SDA, /INT pin, $V_{IN}$ = $V_{DD}$ or GND | |

Note: If there is no special indication, the test conditions are GND=0V, VDD=1.6V~5.5V, Ta=-40°C~+105°C.
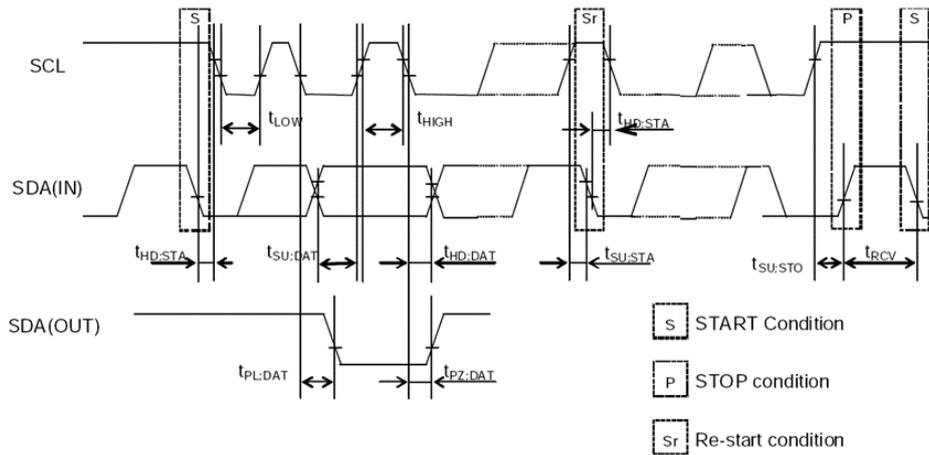
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## 2.5 AC Characteristics



Figure 1. I$^2$C bus Timing Chart

**Table6. AC Characteristics**

$V_{DD}$=2.5V ~ 4.5V; Ta=-40℃ ~ +105℃

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| SCL clock frequency | $f_{SCL}$ | | | 400 | kHz |
| SCL low level time | $t_{LOW}$ | 1.3 | | | us |
| SCL high level time | $t_{HIGH}$ | 0.6 | | | us |
| Start condition setup time | $t_{HD;STA}$ | 0.6 | | | us |
| Start condition hold time | $t_{SU;STA}$ | 0.6 | | | us |
| Stop condition setup time | $t_{SU;STO}$ | 0.6 | | | us |
| Bus idle time between start condition and stop condition | $t_{RCV}$ | 1.3 | | | us |
| Data setup time | $t_{SU;DAT}$ | 100 | | | ns |
| Data hold time | $t_{HD;DAT}$ | 0 | | | ns |
| SCL, SDA rising time | $t_r$ | | | 0.4 | us |
| SCL, SDA falling time | $t_f$ | | | 0.4 | us |

Note: when the master accesses the equipment through I2C bus, all communication from sending start condition to sending stop shall be completed within 1 second. If it exceeds 1 second, the I2C bus interface will be reset through the internal bus timeout function.

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# 3 Registers

## 3.1 Register Lists

Address 0x00~0x0F: Basic Time and Calendar Registers

Address 0x10~0x1F: Extended Register Group 1

Address 0x20~30: Extended Register Group 2

Note: 0x10~16 and 0x00~06 with the same function, 0x1B~1F and 0x0B~0F with the same function

**Table7. Basic Time and Calendar Registers**

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | R/W |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | SEC | O | BCD code, Second tens place, 0-5 | | | BCD code, Second ones place, 0-9 | | | | R/W |
| 0x01 | MIN | O | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | R/W |
| 0x02 | HOUR | O | O | BCD code, Hour tens place, 0-2 | | BCD code, Hour ones place, 0-9 | | | | R/W |
| 0x03 | WEEK | O | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R/W |
| 0x04 | DAY | O | O | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | R/W |
| 0x05 | MONTH | O | O | O | BCD code, Month tens place, 0-1 | BCD code, Month ones place, 0-9 | | | | R/W |
| 0x06 | YEAR | BCD code, Year tens place, 0-9 | | | | BCD code, Year ones place, 0-9 | | | | R/W |
| 0x07 | RAM | ● | ● | ● | ● | ● | ● | ● | ● | R/W |
| 0x08 | MIN Alarm | AE | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | R/W |
| 0x09 | HOUR Alarm | AE | ● | BCD code, Hour tens place, 0-2 | | BCD code, Hour ones place, 0-9 | | | | R/W |
| 0x0A | WEEK Alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R/W |
| 0x0A | DAY Alarm | AE | ● | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | R/W |
| 0x0B | Timer Counter 0 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | R/W |
| 0x0C | Timer Counter 1 | 32768 | 16384 | 8192 | 4096 | 2048 | 1024 | 512 | 256 | R/W |
| 0x0D | Extension Register | TEST | WADA | USEL | TE | FSEL[1] | FSEL[0] | TSEL[1] | TSEL[0] | R/W |
| 0x0E | Flag Register | O | O | UF | TF | AF | O | VLF | VDET | R/W |
| 0x0F | Control Register | CSEL[1] | CSEL[0] | UIE | TIE | AIE | O | O | RESET | R/W |

**Table8. Extended Register Group 1**

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | R/W |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x10~0x16 | RSV | Reserved | | | | | | | | R |
| 0x17 | TEMP1 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | R |

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| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | R/W |
|---------|----------|------|------|------|------|------|------|------|------|-----|
| 0x18 | Backup Function | ○ | ○ | ○ | ○ | VDET OFF | SWOFF | BKSMP [1] | BKSMP [0] | R/W |
| 0x19 | RSV | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | R |
| 0x1A | RSV | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | R |
| 0x1B | Timer Control | TSTP | TRES | ○ | ○ | ○ | ○ | ○ | ○ | R/W |
| 0x1C | Timer Counter Monitor 0 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | R |
| 0x1D | Timer Counter Monitor 1 | 32768 | 16384 | 8192 | 4096 | 2048 | 1024 | 512 | 256 | R |
| 0x1E | Timer Counter Monitor 2 | 8388608 | 4194304 | 2097152 | 1048576 | 524288 | 262144 | 131072 | 65536 | R |
| 0x1F | Timer Counter 2 | 8388608 | 4194304 | 2097152 | 1048576 | 524288 | 262144 | 131072 | 65536 | R/W |

**Table9.  Extended Register Group2**

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | R/W |
|---------|----------|------|------|------|------|------|------|------|------|-----|
| 0x20 | Device ID | Vendor ID[3:0] | | | | Ver[3:0] | | | | R |
| 0x21 | Control Register 1 | Reserved: Ensure to be 0x0 | | | | SWSEL1 | SWSEL0 | VBAT_FULL_SEL | | R/W |
| 0x22 | Control Register 2 | Chgen | Inien | Reserved | | | | | | R/W |
| 0x23-26 | RSV | Reserved | | | | | | | | R |
| 0x27 | SubSEC | Reserved | | | | SubSEC[3:0] | | | | R |
| 0x28 | RSV | Reserved: Ensure to be 0x00 | | | | | | | | R/W |
| 0x29-2F | RSV | Reserved | | | | | | | | R |

Note:

1, After power-up reset or in case VLF bit returns "1", make sure to initialize all registers to default state before using the RTC. Ensure all inputs are in the required range and the defined values are set for the reserved bits in case the clock cannot work normally.

✓ During the initial power-up, below bits will be in the state as below:

Initial 0:TEST, WADA, USEL, TE, FSEL[1:0], TSEL[0], UF, TF, AF, CSEL[1], UIE, TIE, RESET,

VDETOFF, SWOFF, BKSMP[1:0], VBATSW.

Initial 1: VLF, VDET, CSEL[0].

✓ All other register values are undefined, so make sure to reset the module before using it.

✓ The bits marked with "○" can be read out "0" only after initializing.

✓ The bits marked with "●" are RAM bits which can be used to write or read any data.

✓ Only 0 can be written to UF, TF, AF, VLF, VDET bits.

✓ Make sure "0" to be written for TEST bits which are used for testing only.

✓ Reserved bits must be set to the defined values accordingly.

## 3.2 Details of Registers

### 3.2.1 Clock counter registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x00 | SEC | O | BCD code, Second tens place, 0-5 | | | BCD code, Second ones place, 0-9 | | | | 0x00 |
| 0x01 | MIN | O | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | 0x00 |
| 0x02 | HOUR | O | O | BCD code, Hour tens place, 0-2 | | BCD code, Hour ones place, 0-9 | | | | 0x00 |

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x03 | WEEK | O | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x40 |

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

**Table10. WEEK Register**

| WEEK | Data | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|------|------|
| Sunday | 01h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Monday | 02h | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Tuesday | 04h | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Wednesday | 08h | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Thursday | 10h | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Friday | 20h | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Saturday | 40h | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x04 | DAY | O | O | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | 0x01 |

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not .

**Table11.  DAY Register Value**

| Month | Day Value Range |
|-------|-----------------|
| 1, 3, 5, 7, 8, 10, 12 | 1~31 |
| 4, 6, 9, 11 | 1~30 |
| February in normal year | 1~28 |
| February in leap year | 1~29 |

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x05 | MONTH | O | O | O | BCD code, Month | BCD code, Month ones place, 0-9 | | | | 0x01 |

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| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| | | | | | tens place, 0-1 | | | | | |
| 0x06 | YEAR | BCD code, Year tens place, 0-9 | | | | BCD code, Year ones place, 0-9 | | | | 0x00 |

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

Example: 2020/01/01 Wednesday 21:18:36

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|----------|------|------|------|------|------|------|------|------|
| 0x00 | SEC | ○ | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0x01 | MIN | ○ | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0x02 | HOUR | ○ | ○ | 1 | 0 | 0 | 0 | 0 | 1 |
| 0x03 | WEEK | ○ | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0x04 | DAY | ○ | ○ | 0 | 0 | 0 | 0 | 0 | 1 |
| 0x05 | MONTH | ○ | ○ | ○ | 0 | 0 | 0 | 0 | 1 |
| 0x06 | YEAR | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

## 3.2.2 Alarm registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x08 | MIN Alarm | AE | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | 0x00 |
| 0x09 | HOUR Alarm | AE | ● | BCD code, Hour tens place, 0-2 | | BCD code, Minute ones place, 0-9 | | | | 0x00 |
| 0x0A | WEEK Alarm | | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 |
| | DAY Alarm | AE | ● | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | |
| 0x0E | Flag Register | ○ | ○ | UF | TF | AF | ○ | VLF | VDET | |
| 0x0F | Control Register | CSEL[1] | CSEL[0] | UIE | TIE | AIE | ○ | ○ | RESET | |

According to AIE, AF, WADA bits setting, the alarm interrupt will be generated once the current time match the settings in the above registers, the /INT pin goes to low level and AF bit is set to '1' to record an alarm interrupt event has occurred.

WEEK Alarm/DAY Alarm: Controlled by WADA bit in 0x0D register.

AE: Alarm Enable bit, 0-enable; 1-disenable.

AF: Defined in 0x0E register bit3.

AIE: Defined in 0x0F register bit3.

## 3.2.3 Timer control registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x0B | **Timer Counter 0** | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x00 |
| 0x0C | **Timer Counter 1** | 32768 | 16384 | 8192 | 4096 | 2048 | 1024 | 512 | 256 | 0x00 |
| 0x1F | **Timer Counter 2** | 8388608 | 4194304 | 2097152 | 1048576 | 524288 | 262144 | 131072 | 65536 | 0x00 |

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| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x0D | Extension Register | TEST | WADA | USEL | **TE** | FSEL[1:0] | | TSEL[1:0] | | 0x02 |
| 0x0E | Flag Register | ○ | ○ | Reserved | **TF** | Reserved | ○ | Reserved | | 0x03 |
| 0x0F | Control Register | CSEL[1] | CSEL[0] | UIE | **TIE** | AIE | ○ | ○ | RESET | 0x00 |
| 0x1B | Timer Control | **TSTP** | **TRES** | ○ | ○ | ○ | ○ | ○ | ○ | 0x00 |
| 0x1C | **Timer Counter Monitor 0** | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0xFF |
| 0x1D | **Timer Counter Monitor 1** | 32768 | 16384 | 8192 | 4096 | 2048 | 1024 | 512 | 256 | 0Xff |
| 0x1E | **Timer Counter Monitor 2** | 8388608 | 4194304 | 2097152 | 1048576 | 524288 | 262144 | 131072 | 65536 | 0xFF |

According to TE, TF, TIE, TSEL[1:0] bits setting, a timer interrupt will be generated once the value counts down to 0 from the one set in the above registers.

TE: Defined in 0x0D register bit4

TF: Defined in 0x0E register bit4.

TIE: Defined in 0x0F register bit4.

TSEL[1:0]: Defined in 0x0D register bit1 and bit0

TSTP: This bit is used to stop wake-up timer count down.

TRES: Reset the timer counter values.

Timer Counter Monitor: Real-time timer counter value.

Timer Counter: Preset values of timer counter.

## 3.2.4 Extension registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x0D | Extension Register | TEST | WADA | USEL | TE | FSEL[1] | FSEL[0] | TSEL[1] | TSEL[0] | 0x02 |

TEST: Test bit, must be set to "0"

WADA: Week Alarm/Day Alarm control bit, decide 0x0A register as DAY Alarm or WEEK Alarm. 0-WEEK alarm, 1-DAY alarm

USEL: Update Interrupt Select bit, 0-output interrupt once a second, 1-output interrupt once a minute

TE: Timer Enable bit, 0-disenable, 1-enable

FSEL[1], FSEL[0]: FOUT frequency setting:

| FSEL[1] | FSEL[0] | FOUT Frequency |
|---------|---------|----------------|
| 0 | 0 | 32.768KHz (Default) |
| 0 | 1 | 1024Hz |
| 1 | 0 | 1Hz |
| 1 | 1 | 32.768KHz |

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TSEL[1], TSEL[0]: Timer countdown period(source clock) setting:

| TSEL[1] | TSEL[0] | Source clock |
|---------|---------|--------------|
| 0 | 0 | 4096Hz |
| 0 | 1 | 64Hz |
| 1 | 0 | 1Hz |
| 1 | 1 | 1/60Hz |

## 3.2.5   Flag registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x0E | Flag Register | ○ | ○ | UF | TF | AF | ○ | VLF | VDET | 0x03 |

UF: Update flag bit. When time update interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.

TF: Timer Flag bit. When a fixed-cycle timer interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.

AF: Alarm Flag bit. When an alarm interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.

VLF: Voltage Low Flag bit. When supply voltage is lower than 1.6V, it will be set to "1" and keeps "1" until a "0" is written to it.

VDET: Voltage Detection Flag bit. When supply voltage is lower than 1.95V, it will be set to "1" and keeps "1" until a "0" is written to it.

## 3.2.6   Control registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x0F | Control Register | CSEL[1] | CSEL[0] | UIE | TIE | AIE | ○ | ○ | RESET | 0x40 |

CSEL[1], CSEL[0]: Compensation interval Select 1, 0 bits, used to set temperature compensation interval.

| CSEL[1] | CSEL[0] | Compensation interval |
|---------|---------|-----------------------|
| 0 | 0 | 0.5s |
| 0 | 1 | 2s(default) |
| 1 | 0 | 10s |
| 1 | 1 | 30s |

UIE: Update Interrupt Enable bit. When UF changes from "0" to "1", this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

TIE: Timer Interrupt Enable bit: When TF changes from "0" to "1", this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

AIE: Alarm Interrupt Enable bit: When AF changes from "0" to "1", this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

RESET: Reset IC, prepared for the synchronized starting of time or timer.

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## 3.2.7 Temperature register

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x17 | TEMP | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x00 |

Read digital temperature data, Temp [°C] = TEMP *4 *0.1839-55.155.

## 3.2.8 Battery Backup switchover register

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x18 | Backup Function | ○ | ○ | ○ | ○ | VDET OFF | SWOFF | BKSMP [1] | BKSMP [0] | 0x00 |
| 0x21 | Control Register 1 | Reserved: Ensure to be 0x0 | | | | | SWSEL1 | SWSEL0 | VBAT_FULL_SEL | 0x00 |
| 0x22 | Control Register 2 | CHGEN | INIEN | Reserved: Ensure to be 0 | | | | | | 0x00 |

This register controls the power switchover function. Once abnormal VDD is detected, it will be switched to use battery as the power supply.

VDETOFF (Voltage Detector OFF): Main power supply VDD voltage detection control bit. 0-enable detection function (Default), VDD voltage will be detected once a second; 1-disable detection function.

SWOFF (Switch OFF): SW1 control bit. 0- SW1 controlled by swsel[1:0], 1- SW1 turn on.

BKSMP[1:0] (Backup mode Sampling time): Control the voltage detection sampling time. Default: 00.

VBAT_FULL_SEL: Select the threshold volt of full battery supply. Default 0, 1-no threshold volt. 0- threshold volt set to 3V.

SWSEL[1:0]: Power switch control bits during battery backup switchover function disable.

CHGEN: Setting of backup battery charge control(ON/OFF). To set CHGEN active user should set INIEN to "1".

INIEN: Setting of a power switchover function(ON/OFF).

**Table12. Power Switch Control Setting**

| Inien | Swsel[1:0] | SW3 | SW2 | SW1 |
|-------|-----------|-----|-----|-----|
| 0 | 00 | 1 | 1 | 0 |
| | 01（default） | 1 | 0 | 0 |
| | 10 | 0 | 0 | 1 |
| | 11 | -（1） | -（1） | -（0） |
| 1 | - | Power Switch Auto Control | | |

**Table13. V$_{DD}$ Voltage Sampling Time**

| VDD Detect Function | VDETOFF | SWOFF | BKSMP [1] | BKSMP [0] | V$_{DD}$ Voltage Sampling Time | Switch K1 ON/OFF | Notes |
|---|---|---|---|---|---|---|---|
| ON | 0 | X | 0 | 0 | 2ms | 2ms OFF | Default |
| | | | 0 | 1 | 16ms | 16ms OFF | |
| | | | 1 | 0 | 128ms | 128ms OFF | |
| | | | 1 | 1 | 256ms | 256ms OFF | |
| OFF | 1 | 0 | x | x | OFF | ON | SW1 Close |
| | | 1 | x | x | OFF | OFF | SW1 Open |

The power circuit diagram is shown below:
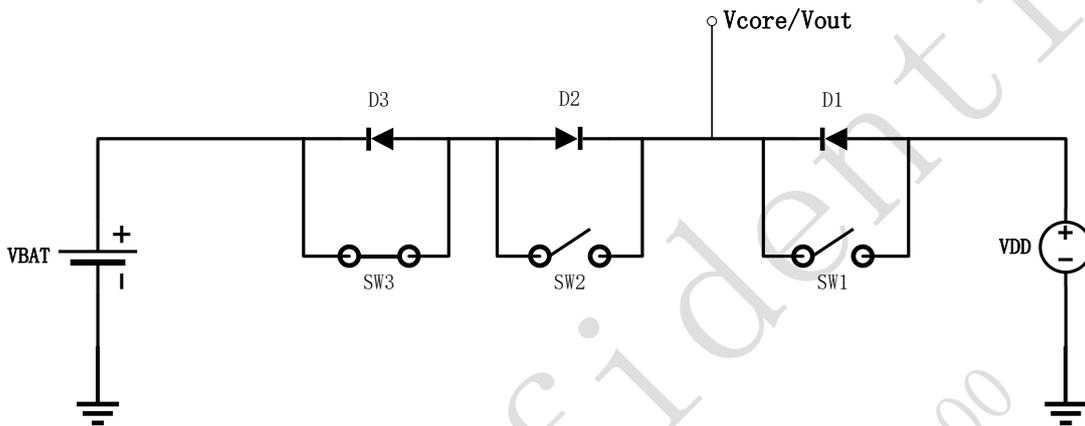


When chip power on, SW1 and SW2 are open, SW3 is close. Chip power supply is from VBAT or VDD through a diode.

a. Non-re-chargeable control (INIEN=1, CHGEN=0):
   When VDD is greater than VDET1, chip work on normal mode. Vdet1 detection always work, and SW1 will open once/1s.
   When VDD is smaller than VDET1, chip work on backup mode. Vdet1 detection work once per 31.25ms.
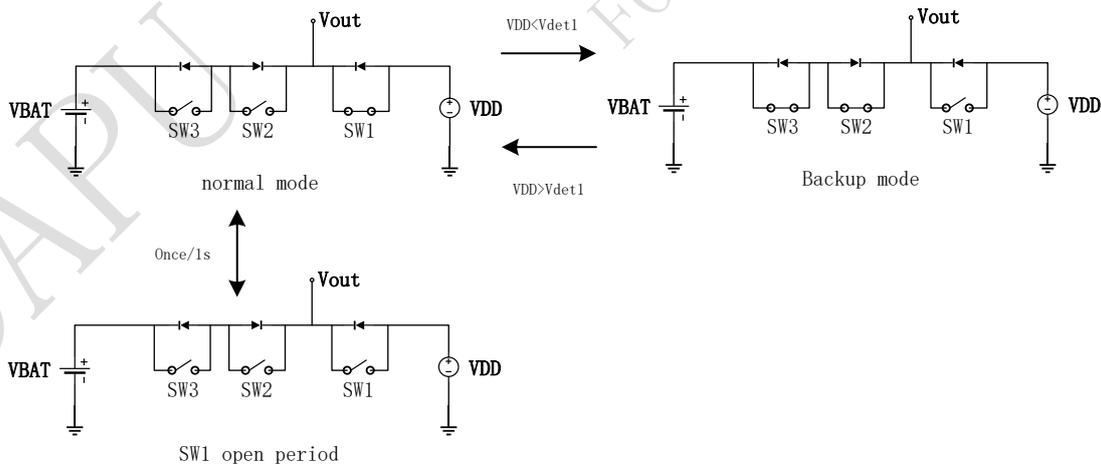


b. Re-chargeable control (INIEN=1, CHGEN=1):
   Charge mode is valid when VDD is greater than VBAT, and VDD is greater than VDET1. In this mode, SW1/SW2/SW3 are close. The VDD charges VBAT. Vdet1 detection always work. SW1 open once/s.
   When VDD < VBAT, chip will enter normal mode. Vdet1 detection always work. SW1 open once/s.

When VDD<VDET1, chip will enter backup mode. Vdet1 detection work once per 31.25ms.
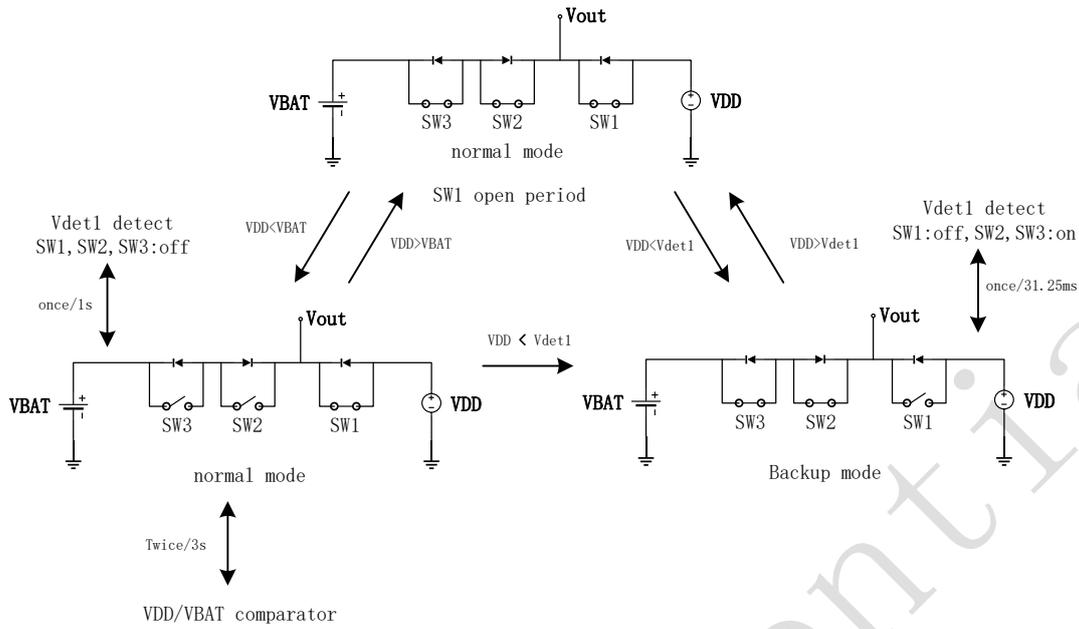


### 3.2.9 Device ID register

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x20 | Device ID | VendorID[3:0] | | | | Ver[3:0] | | | | 0xD5 |

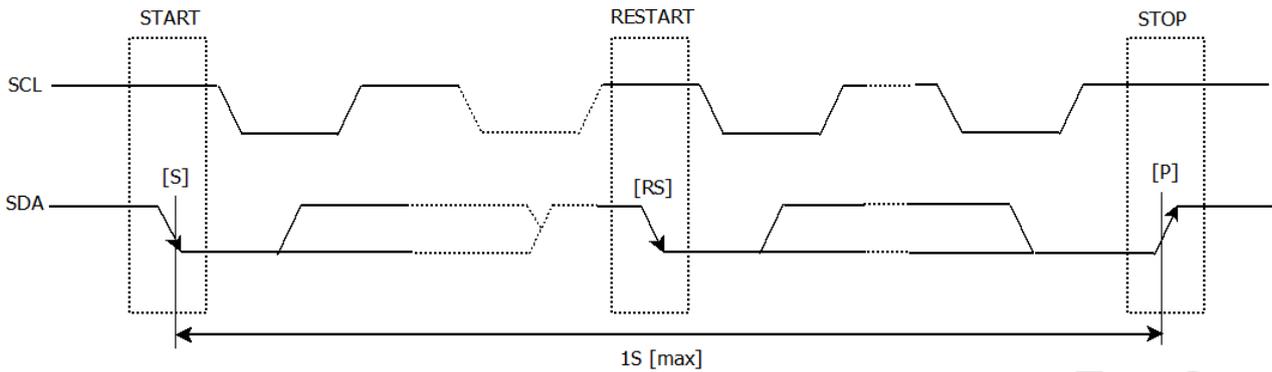VendorID[3:0]: The fixed value is defined as VendorID[3:0]=1101b=Dh to represent DAPU.
Ver[3:0]: version of the IC

### 3.2.10 Sub-second timer register

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x27 | SubSEC | Reserved | | | | SubSEC[3:0] | | | | 0x00 |

SubSEC[3:0]: sub second bit, and unit is 1/16s.

# 4  I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as "Master" and "Slave". INS5A8900 can only be used as Slave.

## 4.1  Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. A new START condition must be transferred before restarting of any communications.

INS5A8900 I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

## 4.2  Slave Address

**Table14.  I²C Bus Slave Address**

| Transfer data | Slave address | | | | | | | R/W |
|---|---|---|---|---|---|---|---|---|
| | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| 65h (Read) | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 (Read) |
| 64h (Write) | | | | | | | | 0 (Write) |

INS5A8900 I²C bus Slave Address is [0110 010*].

## 4.3  I²C bus protocol

It is assumed CPU is master and INS5A8900 is slave in this section.

### 4.3.1  Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the INS5A8900 increments (+1) the address automatically after each data is sent, then to write next data.

(1) CPU sends start condition[S]

(2) CPU sends INS5A8900's slave address with R/W bit to set to write mode

(3) CPU verifies ACK signal from INS5A8900

(4) CPU sends write address to INS5A8900

(5) CPU verifies ACK signal from INS5A8900

(6) CPU sends write data to the address specified at step (4)

(7) CPU verifies ACK signal from INS5A8900

(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically

(9) CPU ends stop condition[P]
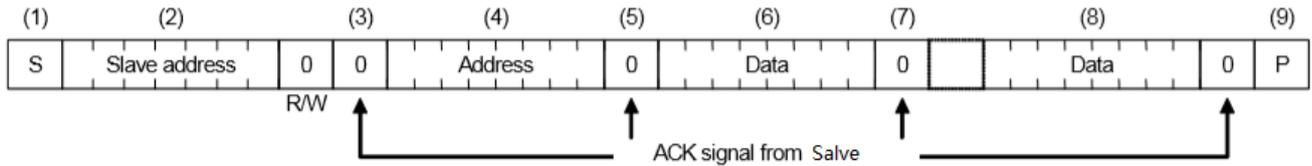


## 4.3.2   Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

(1) CPU sends start condition[S]

(2) CPU sends INS5A8900's slave address with R/W bit to set to write mode

(3) CPU verifies ACK signal from INS5A8900

(4) CPU sends address for reading from INS5A8900

(5) CPU verifies ACK signal from INS5A8900

(6) CPU sends RESTART condition [Sr]

(7) CPU sends INS5A8900's slave address with R/W bit to set to read mode

(8) CPU verifies ACK signal from INS5A8900

(9) CPU reads data from the specified address in step (4)

(10)     CPU sends ACK signal for "0"

(11)     Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically

(12)     CPU sends ACK signal for "1"

(13)     CPU sends stop condition[P]
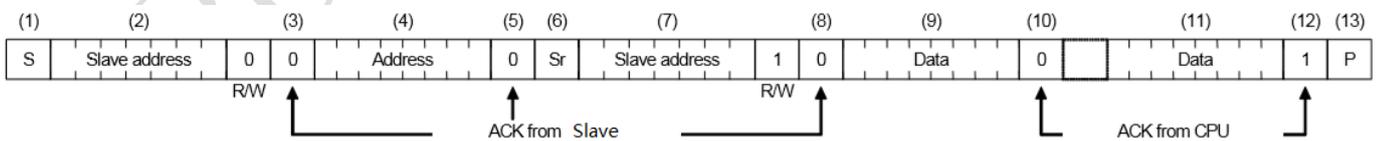
# 5 Reflow Soldering Curve

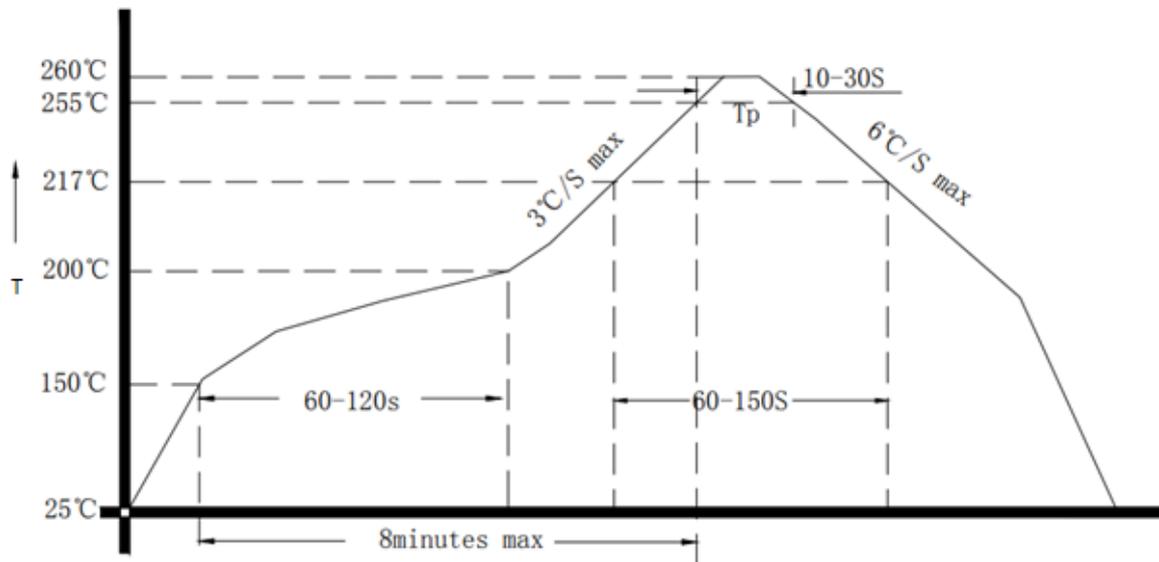Standard: IPC/JEDEC J-STD-020



Figure 2. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260°C, or you will make the xo performance bad, even damage it.

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# 6 Dimensions

[TOP VIEW]

[BOTTOM VIEW]

5A8900
XXXXXXX

| Dimension | Min. | Typ. | Max. |
|---|---|---|---|
| **A** | 3.1 | 3.2 | 3.3 |
| **B** | 2.4 | 2.5 | 2.6 |
| **C** | 0.8 | 0.9 | 1.0 |
| **D** | -- | 0.45 | -- |
| **E** | -- | 1.4 | -- |
| **F1** | -- | 0.4 | -- |
| **F2** | -- | 0.3 | -- |
| **G** | -- | 0.6 | -- |
| **H** | -- | 1.3 | -- |

unit：mm

[SIDE VIEW 1]

[SIDE VIEW 2]
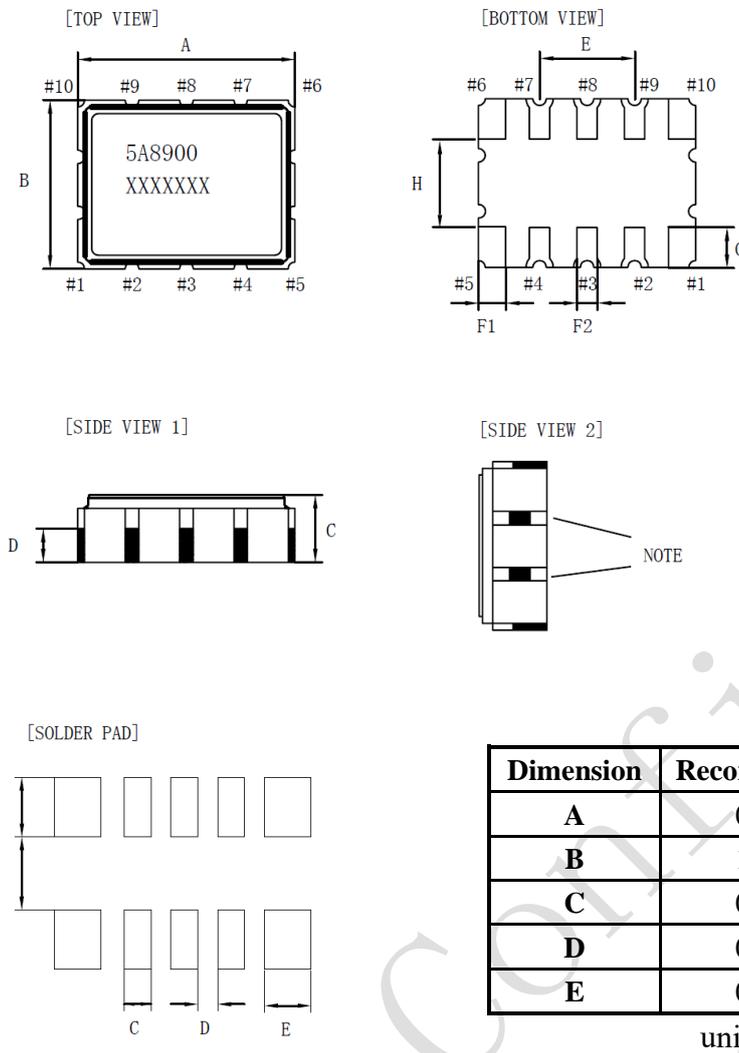
NOTE

[SOLDER PAD]

| Dimension | Recommend |
|---|---|
| **A** | 0.9 |
| **B** | 1.1 |
| **C** | 0.4 |
| **D** | 0.3 |
| **E** | 0.7 |

unit：mm

Figure 3.    Dimensions and Recommended Solder Pad

Note:

1. The metal surface on the side shown in the figure is used for crystal test. Please avoid short circuit caused by contact between the metal surface and other electrical networks or other device surfaces during design and assembly.
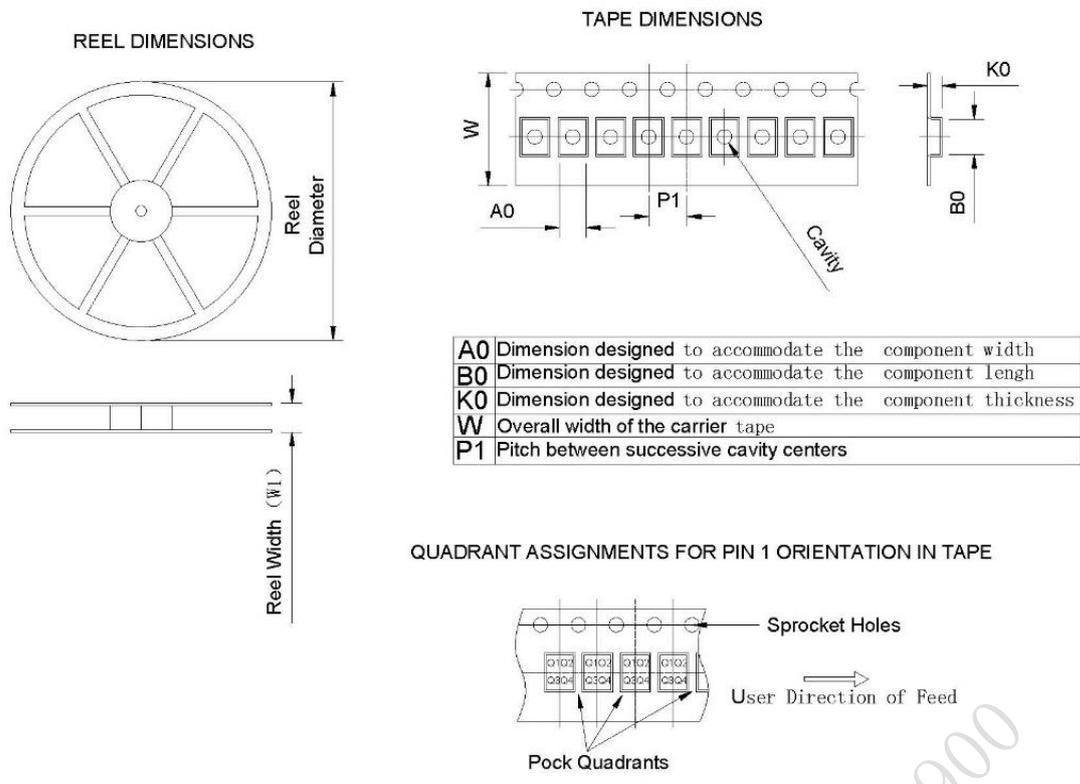
2. The unnoted tolerance is ±0.1mm.

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# 7 Package



Figure 4.    Package

| Device | Package Type | Pins | SPQ | Reel Diameter (mm) | Reel Width W1(mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | PIN1 Quadrant |
|--------|-------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| INS5A8900 | Ceramic | 10 | 3000 | 180 | 11.6±2.0 | 3.00 | 3.70 | 1.50 | 4 | 8.00 | Q1 |

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