National Semiconductor

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INS8208 8-Bit Bidirectional Transceiver

General Description

The INS8208 is an 8-bit TRI-STATE® low power Schottky transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with low power Schottky drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

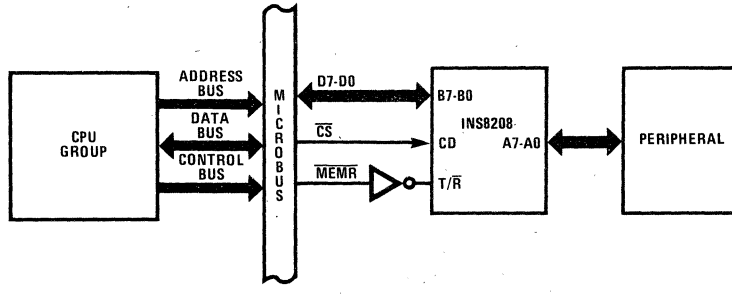
One input, Transmit/Receive, determines the direction of logic signals through the bidirectional transceiver: Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Chip Disable input disables both A and B ports by placing them in a TRI-STATE® condition.

The output high voltage (V_{OH}) is specified at 3.6 V minimum to allow interfacing microprocessors, TTL, MOS, CMOS, RAM, or ROM.

Features

- 8-Bit Bidirectional Data Flow Reduces System Package Count
- Bidirectional TRI-STATE® Inputs/Outputs Interface with Bus-Oriented Systems
- PNP inputs Reduce Input Loading
- 3.6V Output High Voltage Interfaces with TTL, MOS, and CMOS
- 48mA/300pF Bus Drive Capability
- Pinouts Simplify System Interconnections
- Transmit/Receive and Chip Disable Simplify Control Logic
- Compact 20-Pin Dual-In-Line Package
- Low I_{CC} Power (8mA per bidirectional bit)
- MICROBUS™ * Compatible

INS8208 MICROBUS™ Configuration



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Absolute Maximum Ratings (Note 1)

Supply Voltage	7 V
Input Voltage	5.5 V
Output Voltage	5.5 V
Storate Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	600 mW

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions	Limits			Units
Symbol	Description		Min	Typ	Max	
A Port (A0 - A7)						
V_{IH}	Logical "1" Input Voltage	CD = 0.8 V, T/$\overline{R}$ = 2.0 V	2.0			V
V_{IL}	Logical "0" Input Voltage	CD = 0.8 V, T/$\overline{R}$ = 2.0 V			0.8	V
V_{OH}	Logical "1" Output Voltage	CD = 0.8 V, T/$\overline{R}$ = 0.8 V I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
V_{OL}	Logical "0" Output Voltage	CD = 0.8 V, T/$\overline{R}$ = 0.8 V, I_{OL} = 5 mA		0.3	0.45	V
I_{OS}	Output Short Circuit Current	CD = 0.8 V, T/$\overline{R}$ = 0.8 V, V_O = 0 V, V_{CC} = 5.25 V, Note 4	−10	−22	−75	mA
I_{IH}	Logical "1" Input Current	CD = 0.8 V, T/$\overline{R}$ = 2.0 V, V_{IH} = 2.7 V		1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0 V, V_{CC} = 5.25 V, V_{IH} = 5.25 V			1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8 V, T/$\overline{R}$ = 2.0 V, V_{IL} = 0.4 V		−70	−250	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0 V, I_{IN} = −12 mA		−0.2	−1.5	V
I_{OD}	Output/Input TRI-STATE® Current	CD = 2.0 V, V_{IN} = 0.4 V			−200	μA
		CD = 2.0 V, V_{IN} = 4.0 V			80	μA
B Port (B0 - B7)						
V_{IH}	Logical "1" Input Voltage	CD = 0.8 V, T/$\overline{R}$ = 0.8 V	2.0			V
V_{IL}	Logical "0" Input Voltage	CD = 0.8 V, T/$\overline{R}$ = 0.8 V			0.8	V
V_{OH}	Logical "1" Output Voltage	CD = 0.8 V, T/$\overline{R}$ = 2.0 V, I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
		CD = 0.8 V, T/$\overline{R}$ = 2.0 V, I_{OH} = −5 mA	2.7	3.6		V
		CD = 0.8 V, T/$\overline{R}$ = 2.0 V, I_{OH} = −10 mA	2.4	3.3		V
V_{OL}	Logical "0" Output Voltage	CD = 0.8 V, T/$\overline{R}$ = 2.0 V, I_{OL} = 20 mA		0.3	0.4	V
		CD = 0.8 V, T/$\overline{R}$ = 2.0 V, I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = 0.8 V, T/$\overline{R}$ = 2.0 V, V_O = 0 V, V_{CC} = 5.25 V, Note 4		−35	−150	mA
I_{IH}	Logical "1" Input Current	CD = 0.8 V, T/$\overline{R}$ = 0.8 V, V_{IH} = 2.7 V		1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0 V, V_{CC} = 5.25 V, V_{IH} = 5.25 V			1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8 V, T/$\overline{R}$ = 0.8 V, V_{IL} = 0.4 V		−12	−250	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0 V, I_{IN} = −12 mA		−0.3	−1.5	V
I_{OD}	Output/Input TRI-STATE® Current	CD = 2.0 V, V_{IN} = 0.4 V			−200	μA
		CD = 2.0 V, V_{IN} = 4.0 V			+200	μA

DC Electrical Characteristics continued (Notes 2 and 3)

Parameter		Conditions		Limits			Units
Symbol	Description			Min	Typ	Max	
Control Inputs CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7 V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.25 V, V_{IH} = 5.25 V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4 V	T/$\overline{R}$		0.23	0.4	mA
			CD		0.45	0.8	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	CD = 2.0 V, V_{CC} = 5.25 V, V_{IN} = 0.4 V			65	100	mA

AC Electrical Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4 V, T/$\overline{R}$ = 0.4 V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		24	40	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4 V, T/$\overline{R}$ = 0.4 V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		11	20	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE® from CD to A Port	B0 to B7 = 0.4 V, T/$\overline{R}$ = 0.4 V (figure C) S_3 = 1, R5 = 1k, C4 = 15 pF		12	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE® from CD to A Port	B0 to B7 = 2.4 V, T/$\overline{R}$ = 0.4 V (figure C) S_3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE® to a Logical "0" from CD to A Port	B0 to B7 = 0.4 V, T/$\overline{R}$ = 0.4 V (figure C) S_3 = 1, R5 = 1k, C4 = 30 pF		32	50	ns
t_{PZHA}	Propagation Delay from TRI-STATE® to a Logical "1" from CD to A Port	B0 to B7 = 2.4 V, T/$\overline{R}$ = 0.4 V (figure C) S_3 = 0, R5 = 5k, C4 = 30 pF		16	25	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4 V, T/$\overline{R}$ = 2.4 V (figure A) R1 = 100 Ω, R2 = 1k, C1 = 300 pF		17	27	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4 V, T/$\overline{R}$ = 2.4 V (figure A) R1 = 100 Ω, R2 = 1k, C1 = 300 pF		15	23	ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE® from CD to B Port	A0 to A7 = 0.4 V, T/$\overline{R}$ = 2.4 V (figure C) S_3 = 1, R5 = 1k, C4 = 15 pF		25	40	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE® from CD to B Port	A0 to A7 = 2.4 V, T/$\overline{R}$ = 2.4 V (figure C) S_3 = 0, R5 = 1k, C4 = 15 pF		16	25	ns
t_{PZLB}	Propagation Delay from TRI-STATE® to a Logical "0" from CD to B Port	A0 to A7 = 0.4 V, T/$\overline{R}$ = 2.4 V (figure C) S_3 = 1, R5 = 100 Ω, C4 = 300 pF		33	50	ns
t_{PZHB}	Propagation Delay from TRI-STATE® to a Logical "1" from CD to B Port	A0 to A7 = 2.4 V, T/$\overline{R}$ = 2.4 V (figure C) S_3 = 0, R5 = 1k, C4 = 300 pF		16	25	ns

AC Electrical Characteristics continued $V_{CC} = 5\,V$, $T_A = 25°C$

Parameter		Conditions	Min	Typ	Max	Units
Transmit/Receive Mode Specifications						
t_{PHZR}	Propagation Delay from a Logical "1" to TRI-STATE® from T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S_1 = 1, R4 = 100 Ω, C3 = 300 pF S_2 = 0, R3 = 1k, C2 = 15 pF		14	22	ns
t_{PLZR}	Propagation Delay from a Logical "0" to TRI-STATE® from T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S_1 = 0, R4 = 1k, C3 = 300 pF S_2 = 1, R3 = 1k, C2 = 15 pF		20	30	ns
t_{PHZT}	Propagation Delay from a Logical "1" to TRI-STATE® from T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S_1 = 0, R4 = 1k, C3 = 15 pF S_2 = 1, R3 = 5k, C2 = 30 pF		22	33	ns
t_{PLZT}	Propagation Delay from a Logical "0" to TRI-STATE® from T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S_1 = 1, R4 = 1k, C3 = 15 pF S_2 = 0, R3 = 1k, C2 = 30 pF		34	50	ns
t_{PRL}	Propagation Delay from Transmit Mode to a Logical "0," T/$\overline{R}$ to A Port	$t_{PRL} = t_{PHZT} + t_{PDHLA}$		46	70	ns
t_{PRH}	Propagation Delay from Transmit Mode to a Logical "1," T/$\overline{R}$ to A Port	$t_{PRH} = t_{PLZT} + t_{PDLHA}$		45	70	ns
t_{PTL}	Propagation Delay from Receive Mode to a Logical "0," T/$\overline{R}$ to B Port	$t_{PTL} = t_{PHZR} + t_{PDHLB}$		31	50	ns
t_{PTH}	Propagation Delay from Receive Mode to a Logical "1," T/$\overline{R}$ to B Port	$t_{PTH} = t_{PLZR} + t_{PDLHB}$		35	50	ns

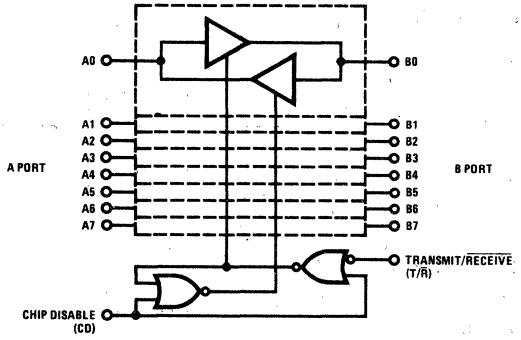
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75 V to 5.25 V power supply range. All typical values given are for $V_{CC} = 5\,V$ and $T_A = 25°C$.

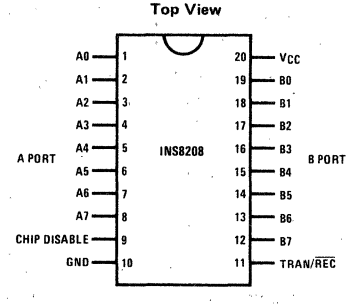
Note 3: All Currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Logic and Connection Diagrams



Top View



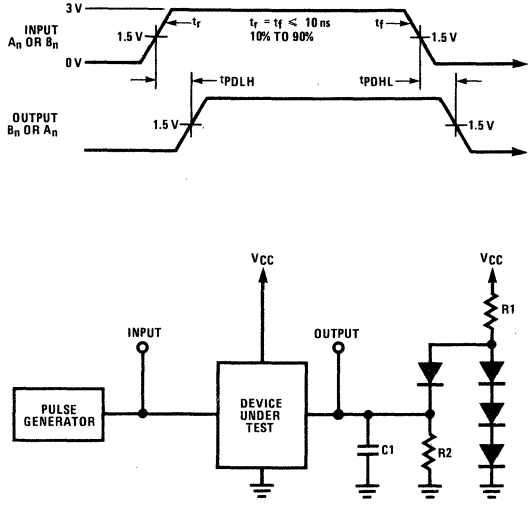
Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/Receive	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't Care

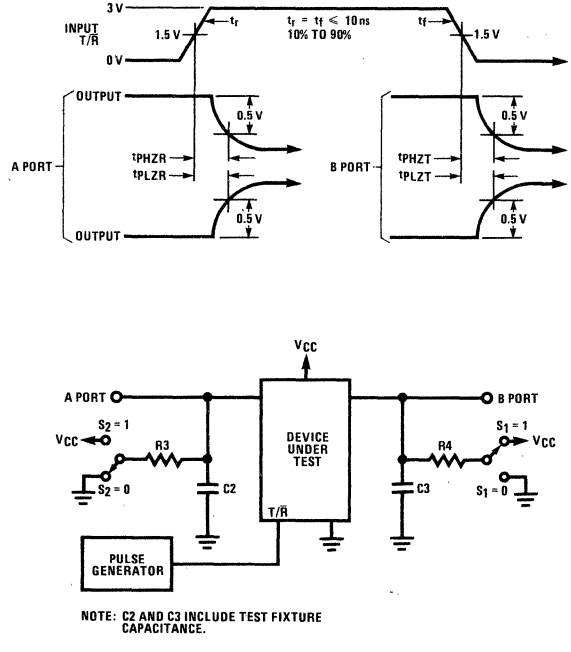
Note: INS8208 is identical to the DP8304

Switching Time Waveforms and AC Test Circuits



NOTE: C1 INCLUDES TEST FIXTURE CAPACITANCE.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port



NOTE: C2 AND C3 INCLUDE TEST FIXTURE CAPACITANCE.

FIGURE B. Propagation Delay from T/$\overline{R}$ to A Port or B Port

D.2