

## INS8212 8-Bit Input/Output Port

### General Description

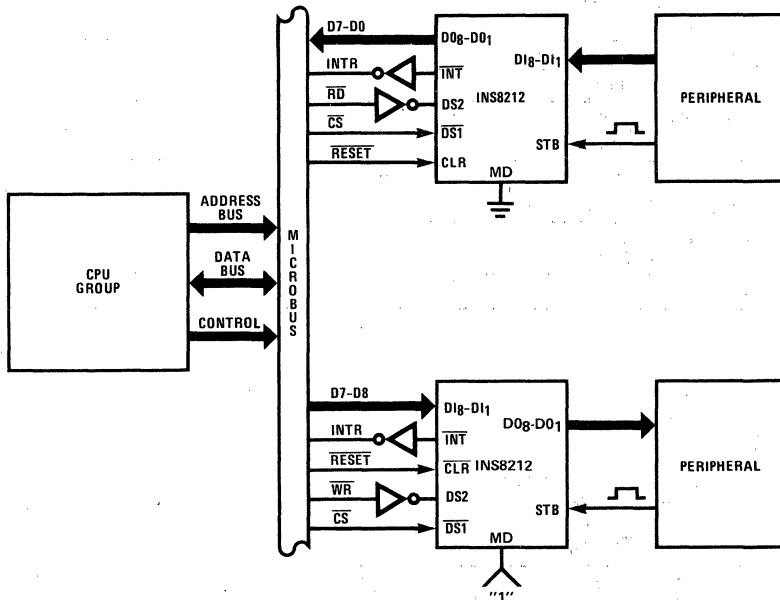
The INS8212 is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's INS8080A microprocessor family. The INS8212 can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The INS8212 includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

### Features

- 8-Bit Data Latch and Buffer
- Service Request Flip-Flop for Generation and Control of Interrupts
- 0.25 mA Input Load Current
- TRI-STATE TTL Output Drive Capability
- Outputs Sink 15 mA
- Asynchronous Latch Clear
- 3.65V Output for Direct Interface to INS8080A
- Reduces System Package Count by Replacing Buffers, Latches, and Multiplexers in Microcomputer Systems
- MICROBUSTM™ Compatible

### INS8212 MICROBUS Configuration



\*Trademark, National Semiconductor Corp.

## Absolute Maximum Ratings

Temperature Under Bias Plastic . . . . .  $-65^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$   
 Storage Temperature . . . . .  $-65^{\circ}\text{C}$  to  $+160^{\circ}\text{C}$   
 All Output or Supply Voltages . . . . .  $-0.5\text{V}$  to  $+7\text{V}$   
 All Input Voltages . . . . .  $-1.0\text{V}$  to  $5.5\text{V}$   
 Output Currents . . . . .  $125\text{mA}$

**Note:** Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

## DC Electrical Characteristics

$T_A = 0^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
$I_F$	Input Load Current STB, DS <sub>2</sub> , CLR, DI <sub>1</sub> -DI <sub>8</sub> Inputs			-0.25	mA	$V_F = 0.45\text{V}$
$I_F$	Input Load Current MD Input			-0.75	mA	$V_F = 0.45\text{V}$
$I_F$	Input Load Current DS <sub>1</sub> Input			-1.0	mA	$V_F = 0.45\text{V}$
$I_R$	Input Leakage Current STB, DS <sub>2</sub> , CLR, DI <sub>1</sub> -DI <sub>8</sub> Inputs			10	$\mu\text{A}$	$V_R = 5.25\text{V}$
$I_R$	Input Leakage Current MD Input			30	$\mu\text{A}$	$V_R = 5.25\text{V}$
$I_R$	Input Leakage Current DS <sub>1</sub> Input			40	$\mu\text{A}$	$V_R = 5.25\text{V}$
$V_C$	Input Forward Voltage Clamp			-1	V	$I_C = -5\text{mA}$
$V_{IL}$	Input "Low" Voltage			0.85	V	
$V_{IH}$	Input "High" Voltage	2.0			V	
$V_{OL}$	Output "Low" Voltage			0.45	V	$I_{OL} = 15\text{mA}$
$V_{OH}$	Output "High" Voltage	3.65	4.0		V	$I_{OH} = -1\text{mA}$
$I_{SC}$	Short Circuit Output Current	-15		-75	mA	$V_O = 0\text{V}$
$I_{IOL}$	Output Leakage Current High Impedance State			20	$\mu\text{A}$	$V_O = 0.45\text{V}/5.25\text{V}$
$I_{CC}$	Power Supply Current		90	130	mA	

## Capacitance\*

$F = 1\text{MHz}$ ,  $V_{BIAS} = 2.5\text{V}$ ,  $V_{CC} = +5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

Symbol	Test	Limits	
		Typ.	Max.
$C_{IN}$	DS <sub>1</sub> , MD Input Capacitance	9pF	12pF
$C_{IN}$	DS <sub>2</sub> , CLR, STB, DI <sub>1</sub> -DI <sub>8</sub> Input Capacitance	5pF	9pF
$C_{OUT}$	DO <sub>1</sub> -DO <sub>8</sub> Output Capacitance	8pF	12pF

\*This parameter is sampled and not 100% tested.

## AC Electrical Characteristics

$T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$

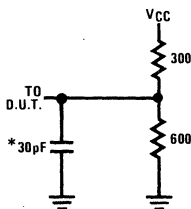
Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{PW}$	Pulse Width	30			ns	
$t_{PD}$	Data to Output Delay			30	ns	
$t_{WE}$	Write Enable to Output Delay			40	ns	
$t_{SET}$	Data Setup Time	15			ns	
$t_H$	Data Hold Time	20			ns	
$t_R$	Reset to Output Delay			40	ns	
$t_S$	Set to Output Delay			30	ns	
$t_E$	Output Enable/Disable Time			45	ns	
$t_C$	Clear to Output Delay			55	ns	

## Switching Characteristics

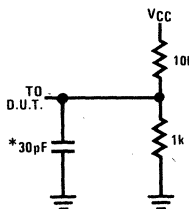
### Conditions of Test:

1. Input Pulse Amplitude = 2.5V.
2. Input Rise and Fall Times = 5ns.
3. Between 1V and 2V Measurements made at 1.5V with 15mA & 30pF Test Load.

**Test Load  
15mA & 30pF**

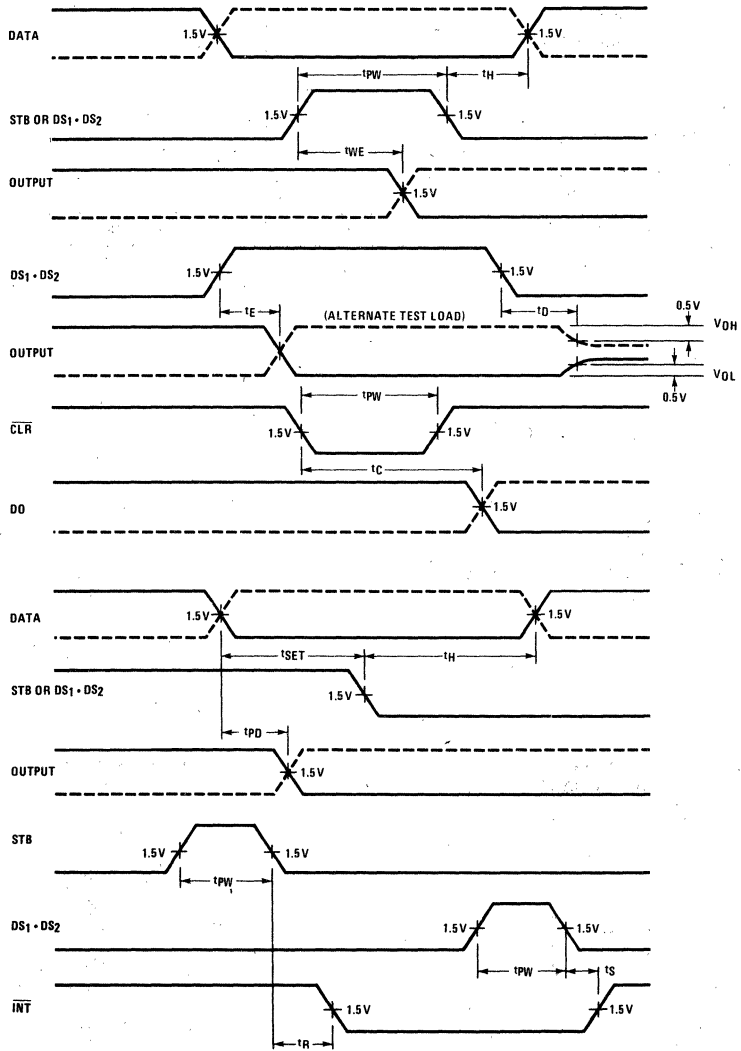


**Alternate Test Load**

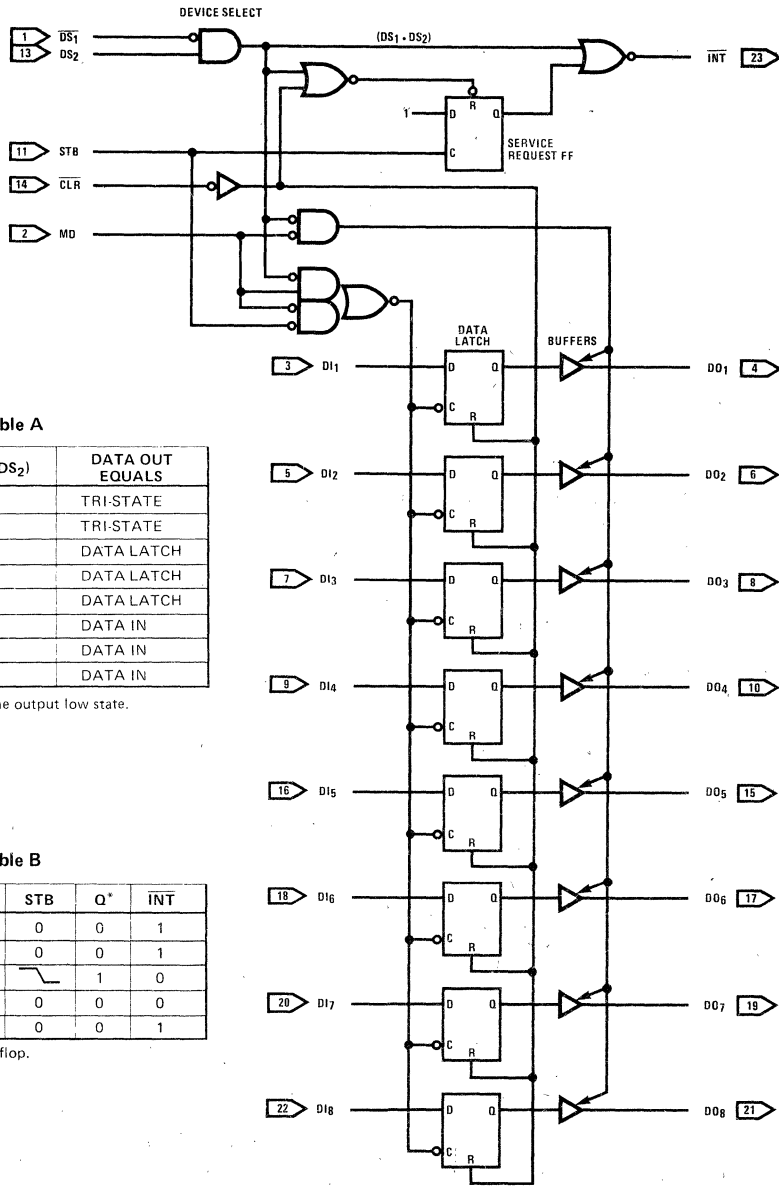


\*including jig & probe capacitance

# Timing Diagram



# INS8212 Logic Diagram



Logic Table A

STB	MD	(DS <sub>1</sub> -DS <sub>2</sub> )	DATA OUT EQUALS
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

CLR  $\overline{\phantom{x}}$  resets data latch to the output low state.

Logic Table B

CLR	(DS <sub>1</sub> -DS <sub>2</sub> )	STB	Q*	INT
0 RESET	0	0	0	1
1	0	0	0	1
1	0	$\overline{\phantom{x}}$	1	0
1	1 RESET	0	0	0
1	0	0	0	1

\* Internal Service Request flip-flop.

## INS8212 Functional Pin Definitions

The following describes the function of all the INS8212 input/output pins. Some of these descriptions reference internal circuits.

### INPUT SIGNALS

**Device Select (DS<sub>1</sub>, DS<sub>2</sub>):** When DS<sub>1</sub> is low and DS<sub>2</sub> is high, the device is selected. The output buffers are

enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

**Mode (MD):** When high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic (DS<sub>1</sub> · DS<sub>2</sub>). When low (input mode), the state of the output buffers is determined by the device selection logic (DS<sub>1</sub> · DS<sub>2</sub>) and the source of the data latch clock input is the strobe (STB) input.

**D.2**

## INS8212 Functional Pin Definitions continued

**Strobe (STB):** Used as data latch clock input when the mode (MD) input is low (input mode). Also used to synchronously set the service request flip-flop, which is negative edge triggered.

**Data In (DI<sub>1</sub>-DI<sub>8</sub>):** Eight-bit data input to the data latch, which consists of eight D-type flip-flops. While the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. The clock input high overrides the clear (CLR) input data latch reset.

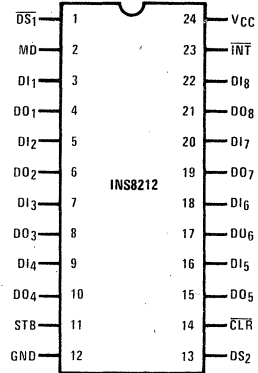
**Clear (CLR):** When low, asynchronously resets (clears) the data latch and the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

### OUTPUT SIGNALS

**Interrupt (INT):** Goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

**Data Out (DO<sub>1</sub>-DO<sub>8</sub>):** Eight-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

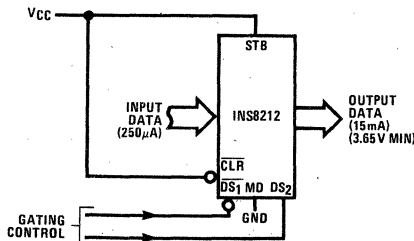
## Pin Configuration



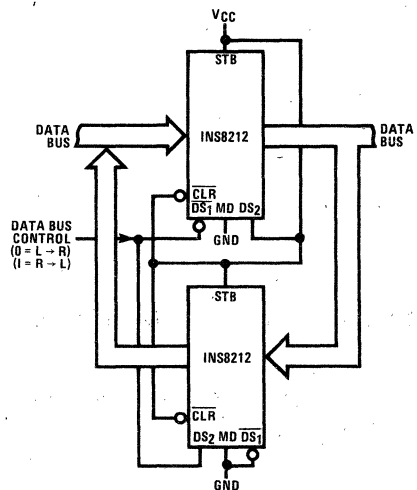
**NOTE:** INS8212 Identical to DP8212

## Applications in Microcomputer Systems

### Gated Buffer (TRI-STATE)

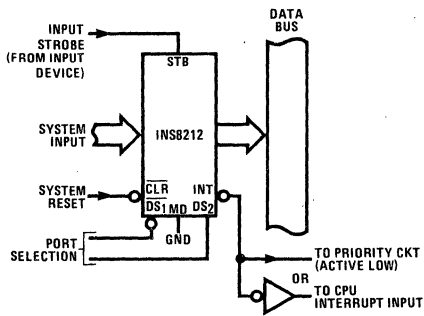


### Bidirectional Bus Driver

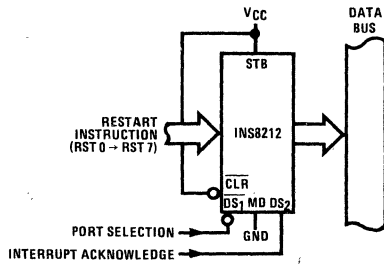


# Applications in Microcomputer Systems continued

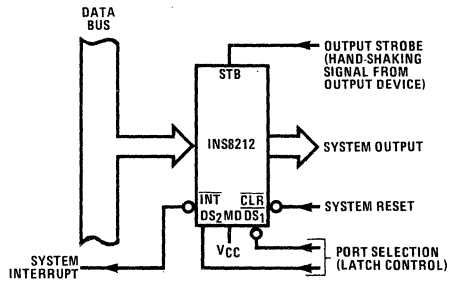
### Interrupting Input Port



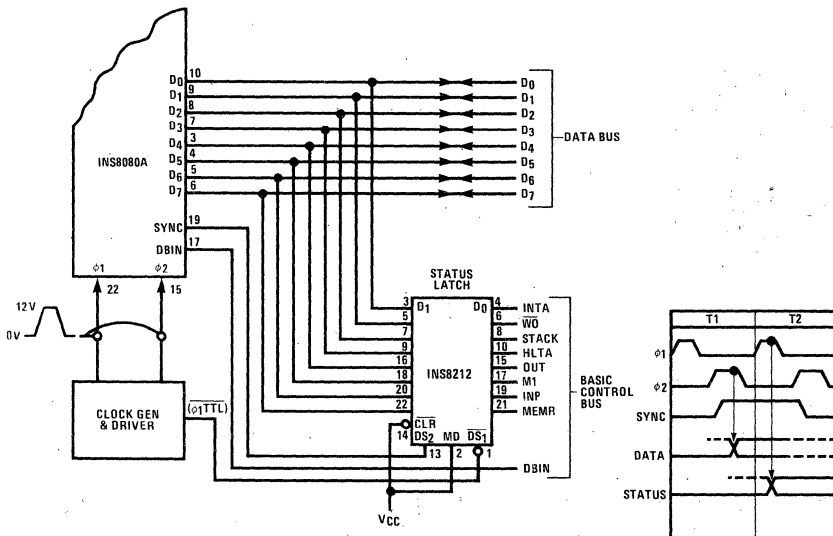
### Interrupt Instruction Port



### Output Port (with Hand-Shaking)

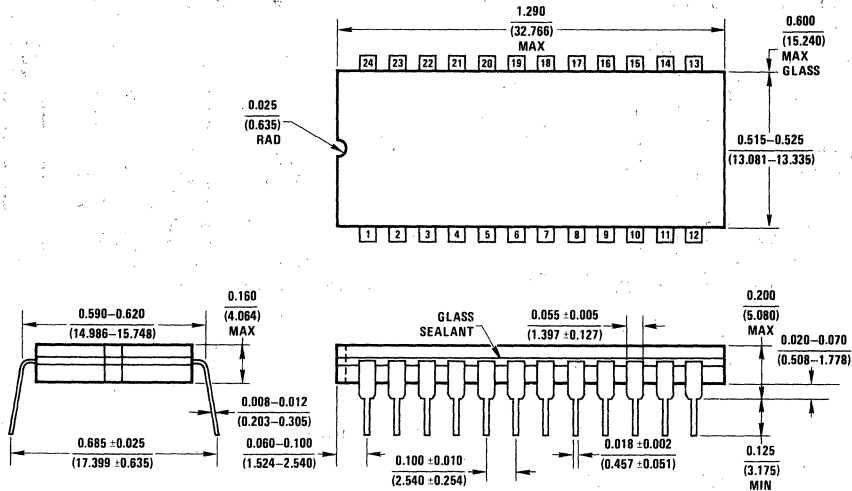


### INS8080A Status Latch

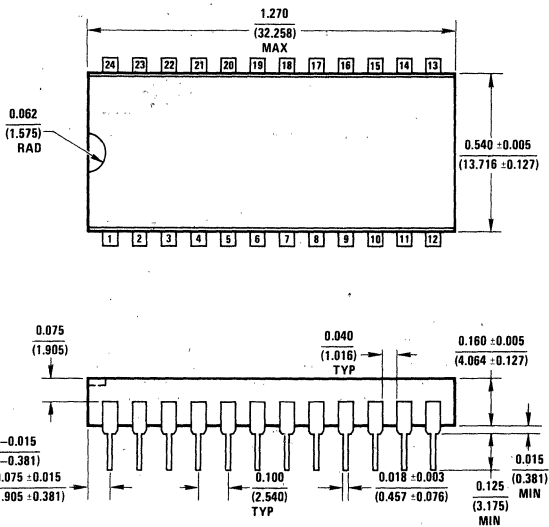


**D.2**

**Physical Dimensions**



**Ceramic Dual-in-Line Package (J)**  
Order Number INS8212J



**Epoxy Dual-in-Line Package (N)**  
Order Number INS8212N



National Semiconductor Corporation  
2900 Semiconductor Drive  
Santa Clara, California 95051  
Tel: (408) 737-5000  
TWX: (910) 339-9240

National Semiconductor GmbH  
8000 München 21  
61/2 Eisenheimerstrasse  
West Germany  
Tel: 089/9 15027  
Telex: 05-22772

NS International Inc., Japan  
Miyake Building  
1-9 Yotsuya, Shinjuku-ku 160  
Tokyo, Japan  
Tel: (03) 355-3711  
TWX: 232-2015 NSCJ-J

NS Electronics (Hong Kong) Ltd.  
8th Floor,  
Cheung Kong Electronic Bldg.  
4 Hing Yip Street  
Kwun Tong  
Kowloon, Hong Kong  
Tel: 3-41241-3  
Telex: 73866 NSEHK HX  
Cable: NATSEMI

NS Electronics Do Brasil  
Avda Brigadero Faria Lima 844  
11 Andar Conjunto 1104  
Jardim Paulistano  
Sao Paulo, Brasil  
Telex: 1121008 CABINE SAO PAULO

NS Electronics Pty. Ltd.  
Cnr. Stud Rd. & Min. Highway  
Bayswater, Victoria 3153  
Australia  
Tel: 03-728-6333  
Telex: 32096