National Semiconductor

APRIL 1978

INS8224 Clock Generator and Driver

General Description

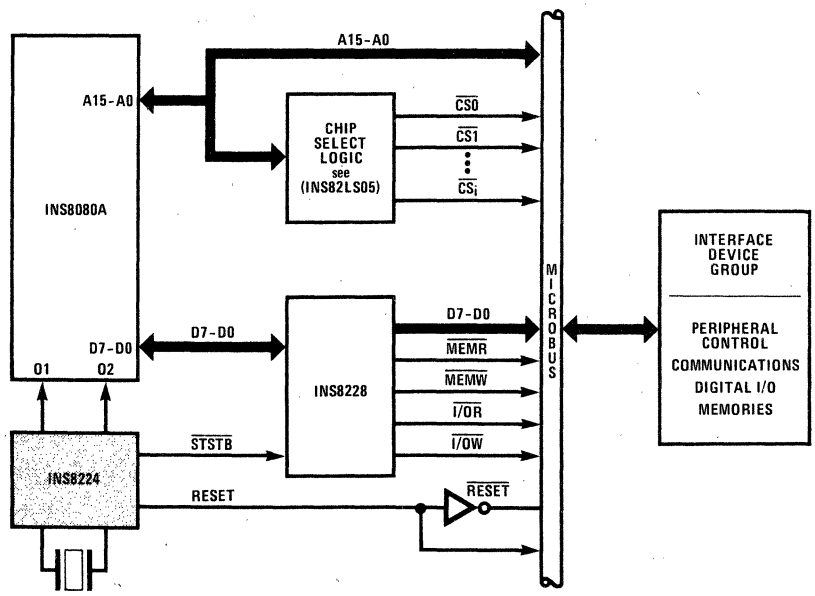
The INS8224 is a clock generator/driver contained in a standard, 16-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates clocks and timing for National Semiconductor's INS8080 microcomputer family.

Included in the INS8224 is an oscillator circuit that is controlled by an external crystal, which is selected by the designer to meet a variety of system speed requirements. Also included in the chip are circuits that provide: a status strobe for the INS8228 or INS8238 system controllers, power-on reset for the INS8080A microprocessor, and synchronization of the READY input to the INS8080A.

Features

- Crystal-Controlled Oscillator for Stable System Operation
- Single Chip Clock Generator and Driver for INS8080A Microprocessor
- Provides Status Strobe for INS8228 or INS8238 System Controllers
- Provides Power-On Reset for INS8080A Microprocessor
- Synchronizes READY Input to INS8080A Microprocessor
- Provides Oscillator Output for Synchronization of External Circuits
- Reduces System Component Count

INS8080 Family CPU Group to MICROBUS™* Configuration



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Absolute Maximum Ratings (NOTE 2)

Supply Voltage, V_{CC} . . . . . 7 V
V_{DD} . . . . . 15 V
Input Voltage . . . . . −1.0 V to +5.5 V
Storage Temperature Range. . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

Operating Conditions

	Min.	Max.	Units
Supply Voltage			
V_{CC}	4.75	5.25	V
V_{DD}	11.4	12.6	V
Temperature	0	70	°C

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = +5.0 V ± 5%; V_{DD} = +12 V ± 5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Current Loading			−0.25	mA	V_F = 0.45 V
I_R	Input Leakage Current			10	μA	V_R = 5.25 V
V_C	Input Forward Clamp Voltage			−1.0	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC} = 5.0 V
V_{IH}	Input "High" Voltage	2.6 2.0			V V	$\overline{RESIN}$ Input All Other Inputs
V_{IH} - V_{IL}	$\overline{RESIN}$ Input Hysteresis	0.25			V	V_{CC} = 5.0 V
V_{OL}	Output "Low" Voltage			0.45 0.45	V V	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} = 2.5 mA All Other Outputs I_{OL} = 15 mA
V_{OH}	Output "High" Voltage ϕ_1, ϕ_2 READY, RESET All Other Outputs	 9.4 3.6 2.4			 V V V	 I_{OH} = −100 μA I_{OH} = −100 μA I_{OH} = −1 mA
I_{SC}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	−10		−60	mA	V_O = 0 V V_{CC} = 5.0 V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Notes:

1. Caution — ϕ_1 and ϕ_2 output drivers do not have short circuit protection.
2. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Crystal Requirements*

Tolerance. . . . . 0.005% at 0°C to +70°C
Resonance . . . . . Fundamental*
Load Capacitance . . . . . 20 pF to 30 pF
Equivalent Resistance. . . . . 75 Ω to 20 Ω
Power Dissipation (min). . . . . 4 mW

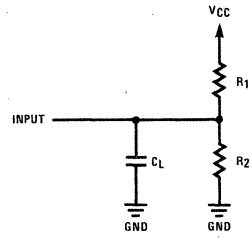
*It is good design practice to ground the case of the crystal
*With tank circuit use 3rd overtone mode.

AC Electrical Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = +5.0\ V \pm 5\%$; $V_{DD} = +12\ V \pm 5\%$.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2t_{CY}}{9} - 20\ ns$			ns	$C_L = 20\ pF$ to $50\ pF$
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5t_{CY}}{9} - 35\ ns$				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2t_{CY}}{9} - 14\ ns$				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9} + 20\ ns$		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	−5		+15	ns	ϕ_2 TTL, $C_L = 30\ pF$ $R_1 = 300\ \Omega$ $R_2 = 600\ \Omega$
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6t_{CY}}{9} - 30\ ns$		$\frac{6t_{CY}}{9}$		$\overline{STSTB}$, $C_L = 15\ pF$ $R_1 = 2\ k\Omega$ $R_2 = 4\ k\Omega$
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{t_{CY}}{9} - 15\ ns$				
t_{DRS}	RDYIN Setup Time to Status Strobe	$50\ ns - \frac{4t_{CY}}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4t_{CY}}{9}$				
t_{DR}	READY or RESET to ϕ_2 Delay	$\frac{4t_{CY}}{9} - 25\ ns$				Ready & Reset $C_L = 10\ pF$ $R_1 = 2\ k\Omega$ $R_2 = 4\ k\Omega$
t_{CLK}	CLK Period		$\frac{t_{CY}}{9}$			
f_{MAX}	Maximum Oscillating Frequency	27			MHz	
C_{IN}	Input Capacitance			8	pF	$V_{CC} = +5.0\ V$ $V_{DD} = +12\ V$ $V_{BIAS} = 2.5\ V$ $f = 1\ MHz$

Test Circuit



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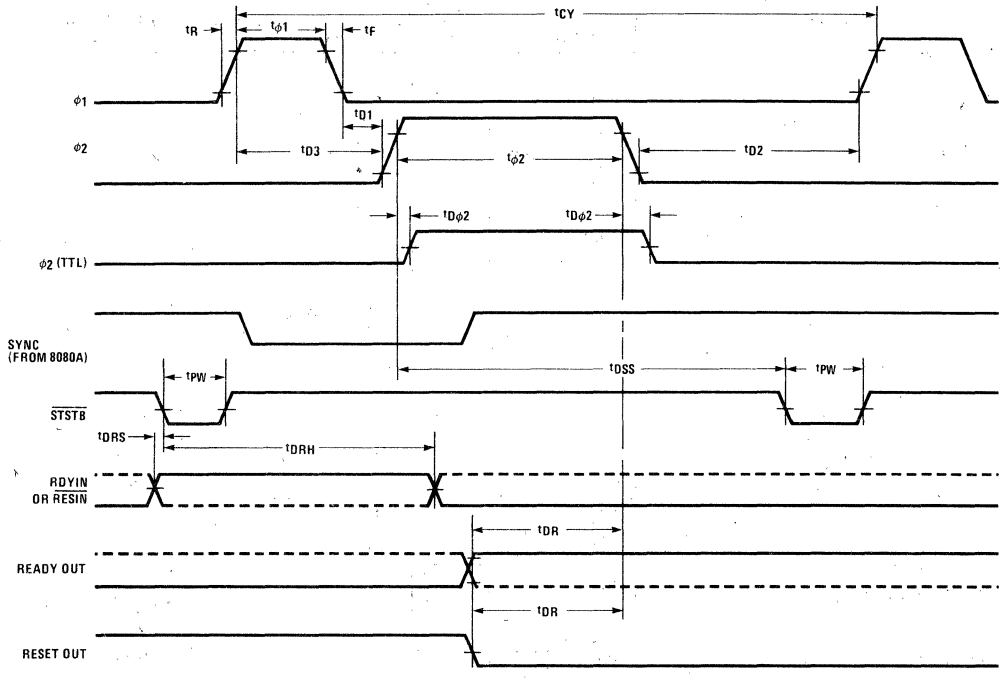
Waveforms



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0 V, Logic "1" = 8.0 V. All other signals measured at 1.5 V.

AC Electrical Characteristics (For t_{CY} = 488.28 ns)

$T_A = 0°C$ to $+70°C$; V_{CC} = +5.0 V ± 5%; V_{DD} = +12 V ± 5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY} = 488.28 ns
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50 pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	Ready & Reset Loaded to 2 mA/10 pF
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5 V unless specified otherwise.
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	

INS8224 Functional Pin Definitions

The following describes the function of all of the INS8224 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Crystal Connections (XTAL 1 and XTAL 2): Two inputs that connect an external crystal to the oscillator circuit of the INS8224. Normally, a fundamental mode crystal is used to determine the basic operating frequency of the oscillator. However, overtone mode crystals may also be used. The crystal frequency is nine times the desired microprocessor speed (that is, crystal frequency equals $1/t_{CY} \times 9$). When the crystal frequency is above 10 MHz, a selected capacitor (3 to 10 picofarads) may have to be connected in series with the crystal to produce the exact desired frequency. Figure A.

Tank: Allows the use of overtone mode crystals with the oscillator circuit. When an overtone mode crystal is used, the tank input connects to a parallel LC network that is ac coupled to ground. The formula for determining the resonant frequency of this LC network is as follows:

$$F = \frac{1}{2\pi\sqrt{LC.}}$$

Synchronizing (SYNC) Signal: When high, indicates the beginning of a new machine cycle. The INS8080A microprocessor outputs a status word (which describes the current machine cycle) onto its data bus during the first state (SYNC interval) of each machine cycle.

Reset In ($\overline{\text{RESIN}}$): Provides an automatic system reset and start-up upon application of power as follows. The $\overline{\text{RESIN}}$ input, which is obtained from the junction of an external RC network that is connected between V_{CC} and ground, is routed to an internal Schmitt Trigger circuit. This circuit converts the slow transition of the power supply rise into a sharp, clean edge when its input reaches a predetermined value. When this occurs, an internal D-type flip-flop is synchronously reset, thereby providing the RESET output signal discussed below.

For manual system reset, a momentary contact switch that provides a low (ground) when closed is also connected to the $\overline{\text{RESIN}}$ input.

Ready In (RDYIN): An asynchronous READY signal that is re-clocked by a D-type flip-flop of the INS8224 to provide the synchronous READY output discussed below.

+5 Volts: V_{CC} supply.

+12 Volts: V_{DD} supply.

Ground: 0 volt reference.

OUTPUT SIGNALS

Oscillator (OSC): A buffered oscillator signal that can be used for external timing purposes.

ϕ_1 and ϕ_2 Clocks: Two non-TTL compatible clock phases that provide nonoverlapping timing references for internal storage elements and logic circuits of the INS8080A microprocessor. The two clock phases are produced by an internal clock generator that consists of a divide-by-nine counter and the associated decode gating logic. Figure B.

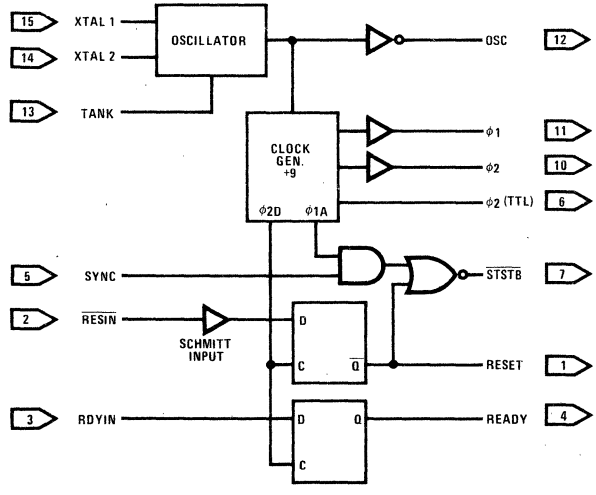
ϕ_2 (TTL) Clock: A TTL ϕ_2 clock phase that can be used for external timing purposes.

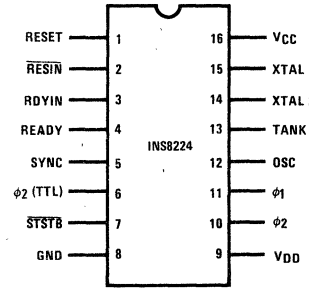
Status Strobe ($\overline{\text{STSTB}}$): Activated (low) at the start of each new machine cycle. The $\overline{\text{STSTB}}$ signal is generated by gating a high-level SYNC input with the ϕ_{1A} timing signal from the internal clock generator of the INS8224. The $\overline{\text{STSTB}}$ signal is used to clock status information into the status latch of the INS8228 system controller and bus driver.

Reset: When the RESET signal is activated, the content of the program counter of the INS8080A is cleared. After RESET, the program will start at location 0 in memory.

Ready: The READY signal indicates to the INS8080A that valid memory or input data is available. This signal is used to synchronize the INS8080A with slower memory or input/output devices.

Logic Diagram and Pin Configuration





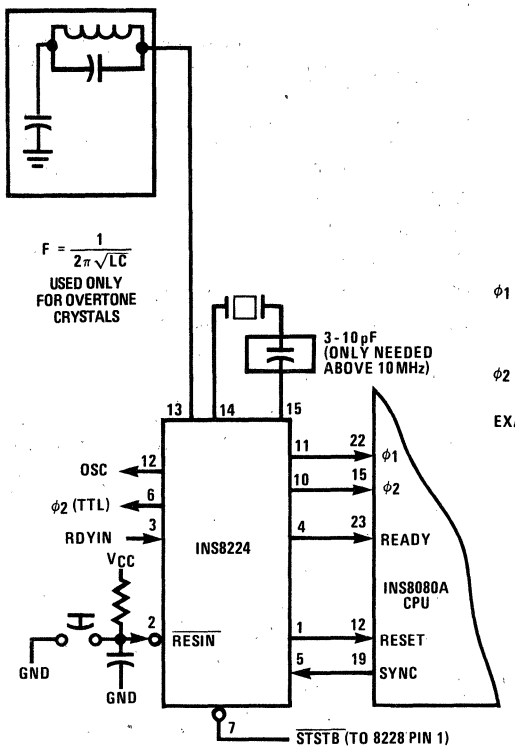


Figure A. INS8224 Connection Diagram

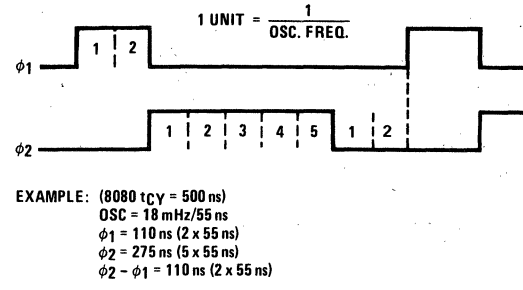
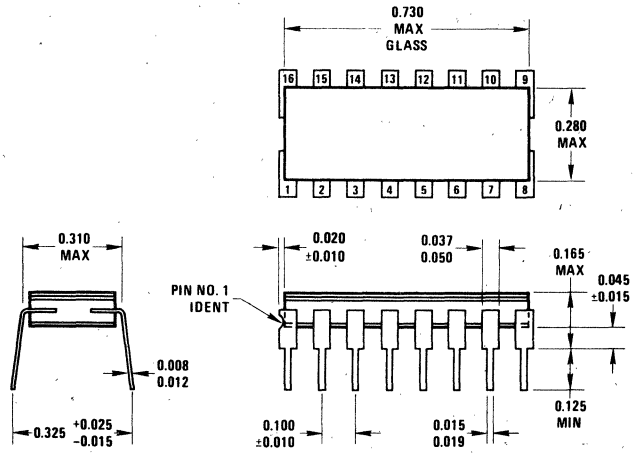


Figure B. INS8224 Clock Generator Waveforms

Physical Dimensions



16-Pin D Package
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