National Semiconductor

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INS8228/INS8238 System Controller and Bus Driver

General Description

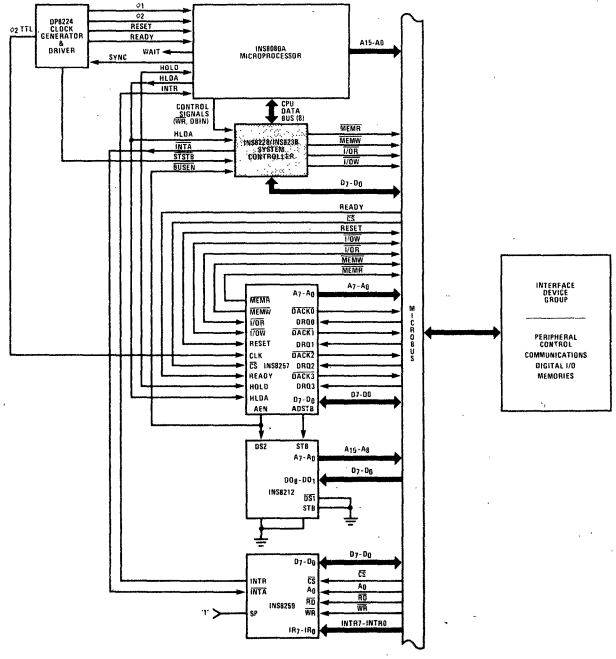
The INS8228/INS8238 is a system controller/bus driver contained in a standard, 28-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates all the read and write control signals required to directly interface the memory and input/output components of National Semiconductor's INS8080A microcomputer family. The chip also provides drive and isolation for the bidirectional data bus of the INS8080A microprocessor. Data bus isolation enables the use of slower memory and input/output components in a system, and provides for enhanced system noise immunity.

A user-selected single-level interrupt vector (RST 7) is provided by the chip for use in the interrupt structure of small systems that need only one basic vector. No additional components (such as an interrupt instruction port) are required to use the single interrupt vector in these systems. The INS8228/INS8238 also generates an Interrupt Acknowledge ($\overline{INTA}$) control signal for each byte of a multibyte CALL instruction when an interrupt is acknowledged by the INS8080A. This feature permits the use of a multilevel priority interrupt structure in large, interrupt-driven systems.

Features

- MICROBUS™* Compatible
- Single Chip System Controller and Bus Driver for INS8080A Microcomputer Systems
- Allows Use of Multibyte CALL Instructions for Interrupt Acknowledge
- Provides User-Selected Single-Level Interrupt Vector (RST 7)
- Provides Isolation for Data Bus
- Supports a Wide Variety of System Bus Structures
- Reduces System Component Count
- INS8238 Provides Advanced Input/Output Write and Memory Write Control Signals for Large System Timing Control

INS8080 Family CPU Group to MICROBUS Configuration



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 V to +7 V
Input Voltage . . . . . -1.5 V to +7 V
Output Current . . . . . 100 mA

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = 5 V ± 5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage, All Inputs		0.75	-1.0	V	V_{CC} = 4.75 V; I_C = -5 mA
I_F	Input Load Current					
	$\overline{STSTB}$			500	μA	V_{CC} = 5.25 V
	D_2 & D_6			750	μA	V_F = 0.45 V
	D_0, D_1, D_4, D_5, & D_7			250	μA	
	All Other Inputs			250	μA	
I_R	Input Leakage Current					
	$\overline{STSTB}$			100	μA	V_{CC} = 5.25 V
	DB_0 - DB_7			20	μA	V_R = 5.25 V
	All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	V_{CC} = 5 V
I_{CC}	Power Supply Current		140	190	mA	V_{CC} = 5.25 V
V_{OL}	Output Low Voltage					
	D_0 - D_7			0.45	V	V_{CC} = 4.75 V; I_{OL} = 2 mA
	All Other Outputs			0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage					
	D_0 - D_7	3.6	3.8		V	V_{CC} = 4.75 V; I_{OH} = -10 μA
	All Other Outputs	2.4			V	I_{OH} = -1 mA
I_{OS}	Short Circuit Current, All Outputs	15		90	mA	V_{CC} = 5 V
$I_{O\,(off)}$	Off State Output Current					
	All Control Outputs			100	μA	V_{CC} = 5.25 V; V_O = 5.25 V
				-100	μA	V_O = 0.45 V
I_{INT}	INTA Current			5	mA	(See Test Conditions—Pg. 3)

Notes:
1. Typical values are for T_A = 25°C and nominal supply voltages.

Capacitance

This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits			Units
		Min.	Typ.[1]	Max.	
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

V_{BIAS} = 2.5 V, V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz.

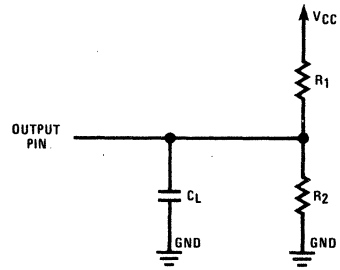
AC Electrical Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = 5\ V \pm 5\%$.

Symbol	Parameter	Limits		Units	Condition
		Min.	Max.		
t_{PW}	Width of Status Strobe	22		ns	
t_{SS}	Setup Time, Status Inputs D_0 - D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0 - D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	60	ns	$C_L = 100$ pF
t_{RR}	Delay from DBIN to Control Outputs		30	ns	$C_L = 100$ pF
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	$C_L = 25$ pF
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	$C_L = 25$ pF
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	45	ns	$C_L = 100$ pF
t_{WE}	Delay to Enable System Bus DB_0 - DB_7 after $\overline{STSTB}$		30	ns	$C_L = 100$ pF
t_{WD}	Delay from 8080 Bus D_0 - D_7 to System Bus DB_0 - DB_7 during Write	5	40	ns	$C_L = 100$ pF
t_E	Delay from System Bus Enable to System Bus DB_0 - DB_7		30	ns	$C_L = 100$ pF
t_{HD}	HLDA to Read Status Outputs		25	ns	$C_L = 100$ pF
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	

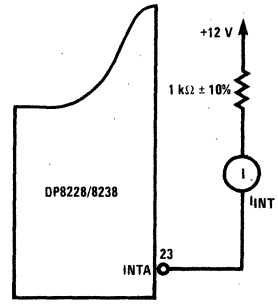
Test Conditions

Test Load[2]



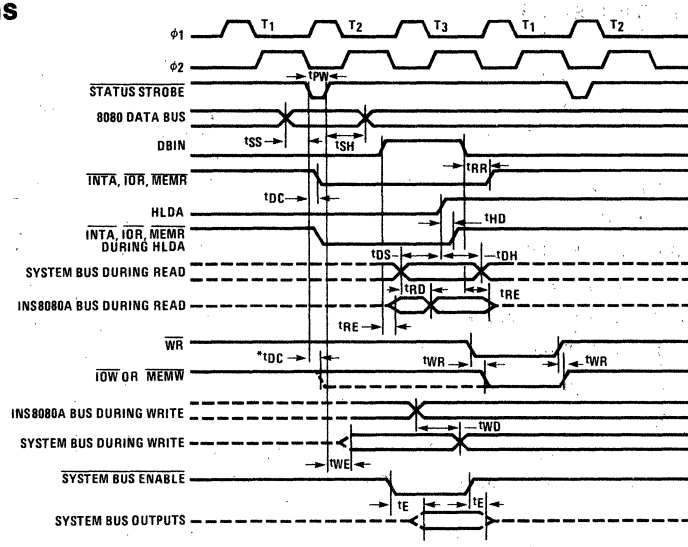
2. For D_0 - D_7: $R_1 = 4\ k\Omega$, $R_2 = \infty$, $C_L = 25$ pF. For all other outputs: $R_1 = 500\ \Omega$, $R_2 = 1\ k\Omega$, $C_L = 100$ pF.

INTA Test Circuit (for RST 7)



D.1

Waveforms



VOLTAGE MEASUREMENT POINTS: D_0 - D_7 (when outputs) Logic "0" = 0.8 V, Logic "1" = 3.0 V. All other signals measured at 1.5 V.

*Advanced $\overline{I/OW}$ $\overline{MEMW}$ for 8238 only.

INS8228/INS8238 Functional Pin Definitions

The following describes the function of all of the INS8228/INS8238 pinouts. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Status Strobe ($\overline{STSTB}$): Activated (low) at the start of each new machine cycle. The $\overline{STSTB}$ input is used to store a status word (refer to chart) from the INS8080A microprocessor into the internal status latch of the INS8228/INS8238. The INS8080A outputs this status word onto its data bus during the first state (SYNC interval) of each machine cycle.

Data Bus In (DBIN): When high, indicates that the INS8080A data bus is in the input mode. The DBIN signal is used to gate data from memory or an input/output device onto the data bus.

Write ($\overline{WR}$): When low, indicates that the data on the INS8080A data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): When high, indicates that the INS8080A data and address buses will go to their high impedance state. When in the data bus read mode, DBIN input in the high state, a high HLDA input will latch the data bus information into the driver circuits and gate off the applicable control signal $\overline{I/OR}$, $\overline{MEMR}$, or $\overline{INTA}$ (return to the output high state).

Bus Enable ($\overline{BUSEN}$): Asynchronous DMA input to the internal gating array of the INS8228/INS8238. When low, normal operation of the internal bidirectional bus driver and gating array occurs. When high, the bus driver and gating array are driven to their high impedance state.

V_{CC} Supply: +5 volts.

Ground: 0 volt reference.

OUTPUT SIGNALS

Memory Read ($\overline{MEMR}$): When low, signals data to be loaded in from memory. The $\overline{MEMR}$ signal is generated by strobing in status word 1, 2, or 4. (Refer to status word chart.)

Memory Write ($\overline{MEMW}$): When low, signals data to be stored in memory. The $\overline{MEMW}$ signal is generated for the INS8238 by strobing in status word 3 or 5. (Refer to status word chart.) For the INS8228, the $\overline{MEMW}$ signal is generated by gating a low-level $\overline{WR}$ input with the strobed in status word 3 or 5.

Input/Output Read ($\overline{I/OR}$): When low, signals data to be loaded in from an addressed input/output device. The $\overline{I/OR}$ signal is generated by strobing in status word 6.

Input/Output Write ($\overline{I/OW}$): When low, signals data to be transferred to an addressed input/output device. The $\overline{I/OW}$ signal for the INS8238 is generated by strobing in status word 7. For the INS8228 the $\overline{I/OW}$ signal is generated by gating in a low-level $\overline{WR}$ input with the strobed in status word 7.

Interrupt Acknowledge ($\overline{INTA}$): When low, indicates that an interrupt has been acknowledged by the INS8080A microprocessor. The $\overline{INTA}$ signal is generated by strobing in status word 8 or 10.

Single Level Interrupt (RST 7): When the $\overline{INTA}$ output is tied to 12V through a 1 kΩ resistor, strobing in status word 8 or 10 will cause the CPU data bus outputs, when active, to go to the high state.

INPUT/OUTPUT SIGNALS

CPU Data (D_7-D_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the INS8080A microprocessor. The bus provides bidirec-

INS8228/INS8238 Functional Pin Definitions (cont'd)

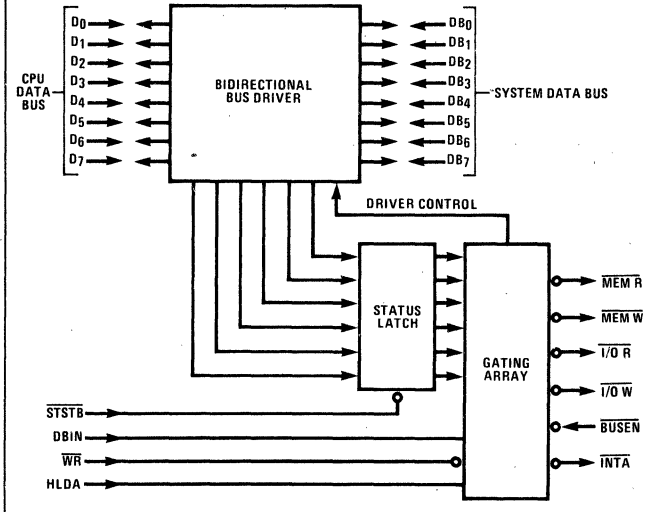
tional communication between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on this data bus during the first microcycle of each machine cycle (SYNC = logic 1).

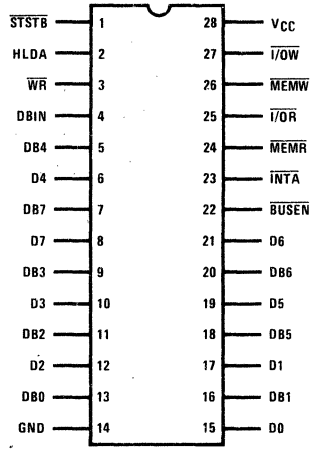
System Data (DB_7-DB_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the memory and input/output components of the system. The internal bidirectional bus driver isolates the DB_7-DB_0 Data Bus from the D_7-D_0 Data Bus.

Status Word Chart

Machine Cycle	Status Word	Data Bus Bit								Control Signal
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Instruction Fetch	1	1	0	1	0	0	0	1	0	$\overline{MEMR}$
Memory Read	2	1	0	0	0	0	0	1	0	$\overline{MEMR}$
Memory Write	3	0	0	0	0	0	0	0	0	$\overline{MEMW}$
Stack Read	4	1	0	0	0	0	1	1	0	$\overline{MEMR}$
Stack Write	5	0	0	0	0	0	1	0	0	$\overline{MEMW}$
Input Read	6	0	1	0	0	0	0	1	0	$\overline{I/OR}$
Output Write	7	0	0	0	1	0	0	0	0	$\overline{I/OW}$
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1	$\overline{INTA}$
Halt Acknowledge	9	1	0	0	0	1	0	1	0	(none)
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1	$\overline{INTA}$

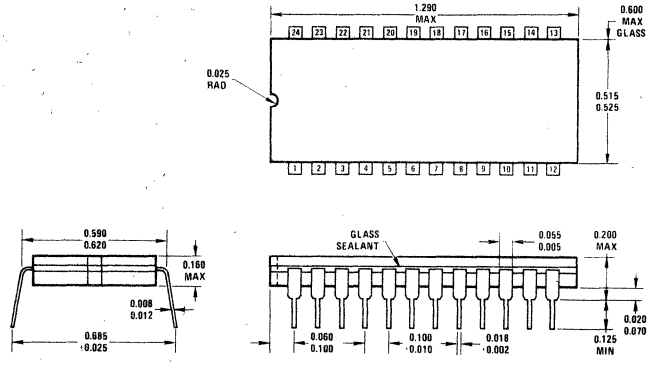
INS8228/INS8238 Block Diagram and Pin Configuration



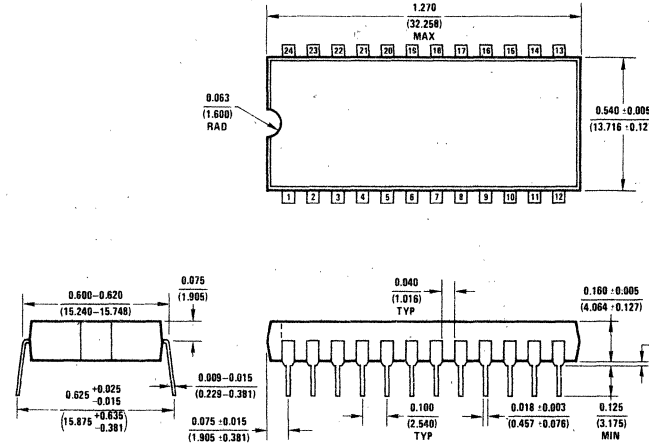


NOTE: INS8228/INS8238 Identical to DP8228/DP8238

Physical Dimensions



Ceramic Dual-in-Line Package (J)
Order Number INS8228J/INS8238J



24-Lead Molded DIP (N)
Order Number INS8228N/INS8238N

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