National Semiconductor

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INS8251 Programmable Communication Interface

General Description

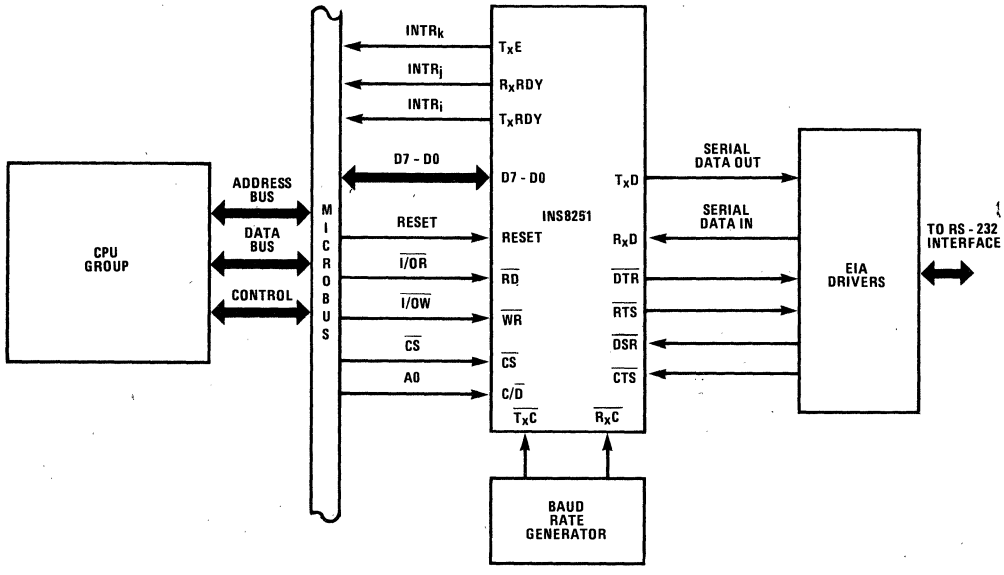
The INS8251 is a programmable Universal Synchronous/Asynchronous Receiver/Transmitter (USART) chip contained in a standard 28-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a serial data input/output interface in National Semiconductor's N8080 microcomputer family. The functional configuration of the INS8251 is programmed by the system software for maximum flexibility, thereby allowing the system to receive and transmit virtually any serial data communication signal presently in use (including IBM Bisync).

The INS8251 can be programmed to receive and transmit either synchronous or asynchronous serial data. The INS8251 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS8251 at any time during the functional operation. Status information reported includes the type and the condition of the transfer operations being performed by the INS8251, as well as any transmission error conditions (parity, overrun, or framing).

Features

- Synchronous and Asynchronous Full Duplex Operations
- Synchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - Internal or External Character Synchronization
  - Automatic Sync Insertion
- Asynchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - 3 Selectable Clock Rates (1x, 16x or 64x the Baud Rate)
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Detection and Generation
  - False Start Bit Detection
- Baud Rates
  - DC to 56k Baud (Synchronous Mode)
  - DC to 9.6k Baud (Asynchronous Mode)
- Transmission Error Detection Capabilities
  - Parity
  - Overrun
  - Framing
- Double Buffering of Data
- TTL Compatible
- Single TTL Clock
- Reduces System Component Count
- MICROBUS™* Compatible

INS8251 MICROBUS Configuration



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings

Ambient Temperature Under Bias. . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . -0.5 V to +7 V
Power Dissipation . . . . . 1 Watt

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = 5.0 V ± 5%; GND = 0 V

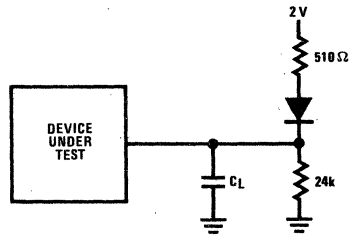
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100 μA
I_{DL}	Data Bus Leakage			-50 10	μA μA	V_{OUT} = 0.45 V V_{OUT} = V_{CC}
I_{IL}	Input Leakage			10	μA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	

Capacitance

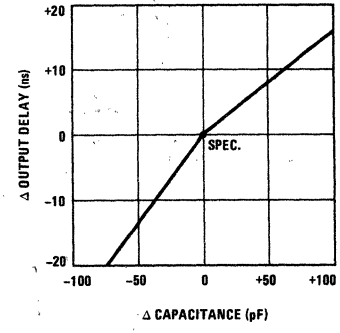
T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

Test Load Circuit



Typical Δ Output Delay vs. Δ Capacitance (pF)



AC Electrical Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = 5.0\ V \pm 5\%$; GND = 0 V

Symbol	Parameter	Min	Max	Unit	Test Conditions
BUS PARAMETERS (Note 1)					
Read Cycle					
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	5		ns	
t_{RR}	$\overline{READ}$ Pulse Width	430		ns	
t_{RD}	Data Delay from $\overline{READ}$		350	ns	$C_L = 100\ pF$
t_{DF}	$\overline{READ}$ to Data Floating		200	ns	$C_L = 100\ pF$
		25		ns	$C_L = 15\ pF$
t_{RV}	Recovery Time Between WRITES (Note 2)	6		t_{CY}	
Write Cycle					
t_{AW}	Address Stable Before $\overline{WRITE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	400		ns	
t_{DW}	Data Set-Up Time for $\overline{WRITE}$	200		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		ns	
OTHER TIMINGS					
t_{CY}	Clock Period (Note 3)	0.420	1.35	μs	
$t_{\phi W}$	Clock Pulse Width	220	0.7 t_{CY}	ns	
t_R, t_F	Clock Rise and Fall Time	0	50	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	$C_L = 100\ pF$
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	$C_L = 100\ pF$
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	$C_L = 100\ pF$
f_{Tx}	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	56	kHz	
	16x and 64x Baud Rate	DC	520	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1x Baud Rate	DC	56	kHz	
	16x and 64x Baud Rate	DC	520	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
t_{Tx}	TxRDY Delay from Center of Data Bit		16	t_{CY}	$C_L = 50\ pF$
t_{Rx}	RxRDY Delay from Center of Data Bit		20	t_{CY}	
t_{IS}	Internal SYNDET Delay from Center of Data Bit		25	t_{CY}	
t_{ES}	Internal SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$		16	t_{CY}	
t_{TxE}	TxEMPTY Delay from Center of Data Bit		16	t_{CY}	$C_L = 50\ pF$
t_{WC}	Control Delay from Rising Edge of $\overline{WRITE}$ (TxE, $\overline{DTR}$, $\overline{RTS}$)		16	t_{CY}	
t_{CR}	Control to $\overline{READ}$ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		16	t_{CY}	

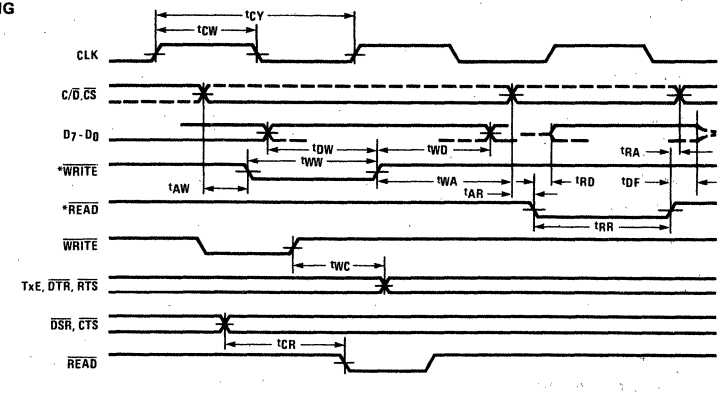
NOTES:

1. AC timings measured at $V_{OH} = 2.0\ V$, $V_{OL} = 0.8\ V$, and with test load circuit of page 2.
2. This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.
3. The $\overline{TxC}$ and $\overline{RxC}$ frequencies have the following limitations with respect to CLK:
   for 1x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/30\ t_{CY}$)
   for 16x and 64x Baud Rate, f_{Tx} or $f_{RX} \leq 1/4.5\ t_{CY}$)
4. Reset Pulse Width = $6\ t_{CY}$ minimum.

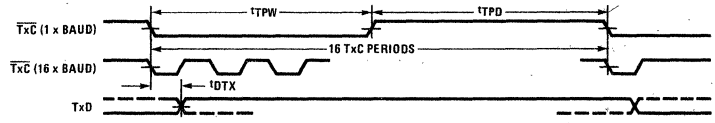
Timing Waveforms

READ AND WRITE TIMING

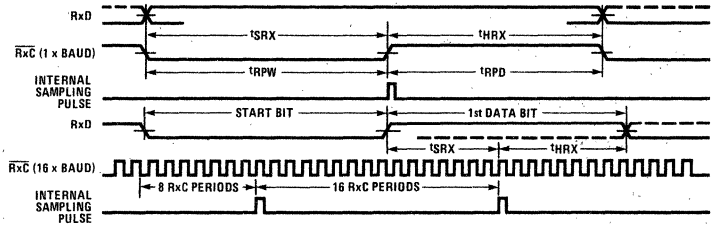
*WRITE AND READ PULSES HAVE NO TIMING LIMITATION WITH RESPECT TO CLK.



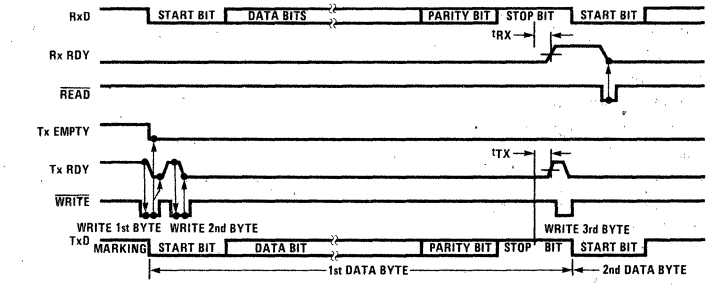
TRANSMITTER CLOCK AND DATA



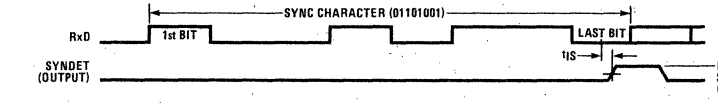
RECEIVER CLOCK AND DATA



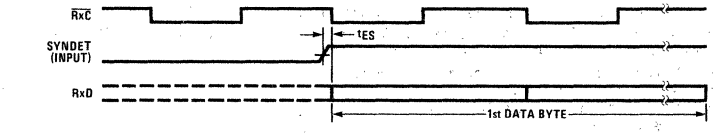
Tx RDY AND Rx RDY TIMING (ASYNC MODE)



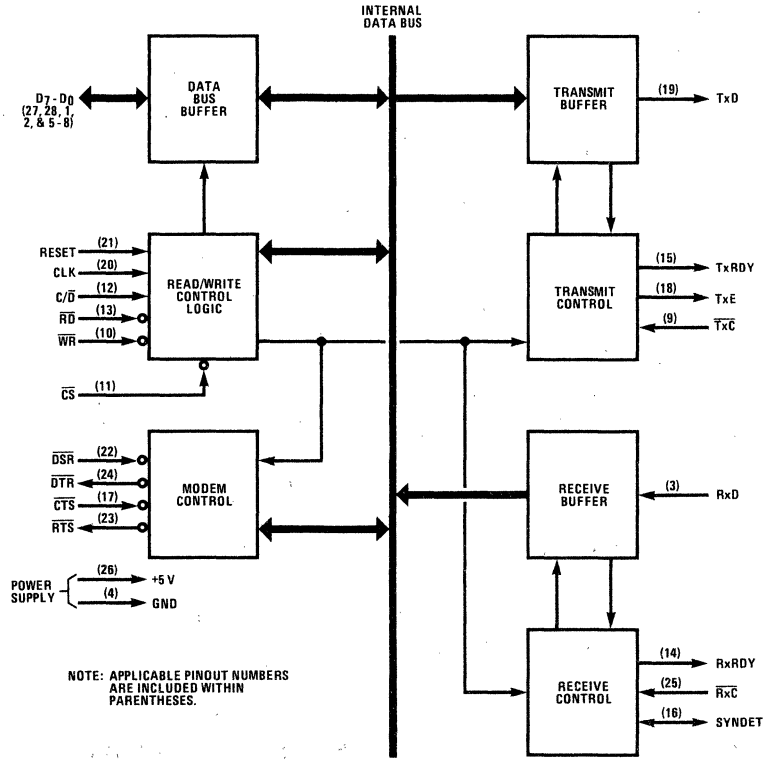
INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT



INS8251 Block Diagram



INS8251 Functional Pin Definitions

The following describes the function of all the INS8251 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Chip Select ($\overline{CS}$): When low (logic 0), the chip is selected. This enables communication between the INS8251 and the INS8080A microprocessor.

Read ($\overline{RD}$): When low, allows the INS8080A to read data or status information from the INS8251.

Write ($\overline{WR}$): When low, allows the INS8080A to write data or control words into the INS8251.

Control/Data (C/$\overline{D}$): Used in conjunction with an active $\overline{RD}$ or $\overline{WR}$ input (logic 0) to determine overall device operation as indicated below.

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Operation
0	0	0	1	Data character read from INS8251
0	0	1	0	Data character written into INS8251
0	1	0	1	Status information read from INS8251
0	1	1	0	Control word written into INS8251
1	x	x	x	Device not selected

Reset: When high (logic 1), places the INS8251 in the idle mode. The device remains in this mode until a new set of control words is written into the INS8251 to program its functional definition. Minimum Reset pulse width is 6 t_{CY}.

Clock (CLK): TTL clock that is used to generate internal timing signals for the INS8251. The minimum frequency of the CLK input is 30 times the receiver/transmitter clock frequency for the synchronous mode, and 4.5 times the receiver/transmitter clock frequency for the asynchronous mode. The CLK input is normally connected to the ϕ_2 (TTL) output of the INS8224 Clock Generator and Driver device.

Transmitter Clock ($\overline{TxC}$): This clock input controls the rate at which a data character is to be transmitted. The frequency of the $\overline{TxC}$ input is equal to the Baud Rate for the synchronous mode, and is a multiple (1x, 16x or 64x) of the Baud Rate for the asynchronous mode. A portion of the Mode Instruction Word (see figure) selects the value of the Baud Rate Factor when in the asynchronous mode. Transmitter Data are clocked out of the INS8251 on the falling edge of the $\overline{TxC}$ input.

Data Set Ready ($\overline{DSR}$): General-purpose input whose condition can be tested by the INS8080A using a status read operation. However, a low-level $\overline{DSR}$ input is normally used to test data set ready conditions.

Clear to Send ($\overline{CTS}$): If low when the TxEN bit (D_0) of the Command Instruction Control Word (see figure) is set high, enables the INS8251 to transmit serial data.

Receiver Data (RxD): Serial data input from a MODEM or an input/output device.

Receiver Clock ($\overline{RxC}$): This clock input controls the rate at which a data character is to be received. The frequency and selection of the $\overline{RxC}$ input is as described above for the $\overline{TxC}$ input. Receiver data are clocked into the INS8251 on the rising edge of the $\overline{RxC}$ input.

V_{CC}: +5-volt supply.

Ground: 0-volt reference.

OUTPUT SIGNALS

Data Terminal Ready ($\overline{DTR}$): General-purpose output which can be set to an active low by programming the $\overline{DTR}$ bit (D_1) of the Command Instruction Control Word. However, a low-level DTR output is normally used for data terminal ready or rate select control.

Request to Send ($\overline{RTS}$): General-purpose output which can be set to an active low by programming the $\overline{RTS}$ bit (D_5) of the Command Instruction Control Word. However, the RTS output is normally used for request to send control in the transmit mode.

Transmitter Data (TxD): Composite serial data output to a MODEM or input/output device. The TxD output is held in the marking state (logic 1) upon a Reset operation.

Transmitter Ready (TxRDY): When high, alerts the INS8080A that the transmitter is ready to accept a data character. The TxRDY output, which is automatically reset whenever a character is written into the INS8251, can be used as an interrupt to the system. For polled operation, the condition of the TxRDY signal can be tested by the INS8080A using a status read operation.

Transmitter Empty (TxE): Goes high to indicate the end of a transmit mode. The TxE output is automatically reset whenever a character is written into the INS8251. In the synchronous mode, a high-level TxE output indicates that a character has not been loaded, the transmitter buffer is empty, and the sync character(s) of a data block are soon to be transmitted automatically as fillers.

Receiver Ready (RxRDY): When high, alerts the INS8080A that the receiver contains a data character that is ready to be input to the CPU. The RxRDY output, which is automatically reset whenever a character is read from the INS8251, can be used as an interrupt to the system. For polled operation, the condition of the RxRDY signal can be tested by the INS8080A using a status read operation.

INPUT/OUTPUT SIGNALS

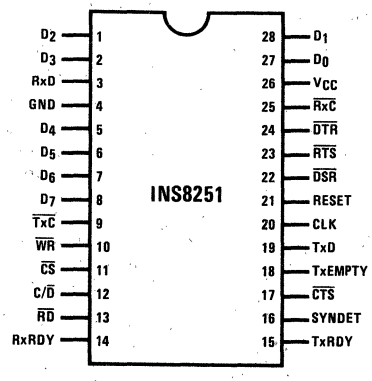
Data (D_7 - D_0) Bus: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8251 and the INS8080A. Data are routed to or from the internal data bus buffer upon execution of an INS8080A OUT or IN instruction, respectively. In addition, control words, command words and status information are transferred through the data bus buffer.

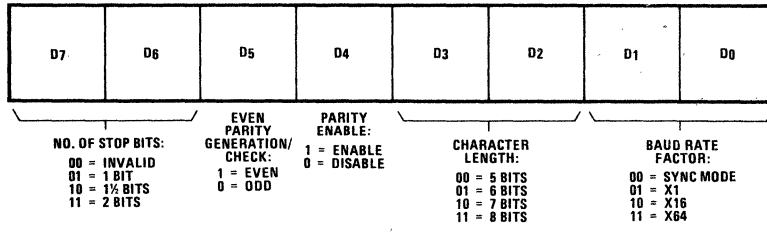
Sync Detect (SYNDET): This pin may be used in the synchronous mode only. System software can program SYNDET as either an input or an output. When used as an output (internal sync detect mode), a high-level SYNDET indicates that the INS8251 has detected sync character(s) in the received serial data. The SYNDET output is automatically reset upon a status read operation by the INS8080A. When used as an input (external sync detect mode), a high-level SYNDET causes the INS8251 to start assembling data characters on the falling edge of the next RxC input.

INS8251 Programming

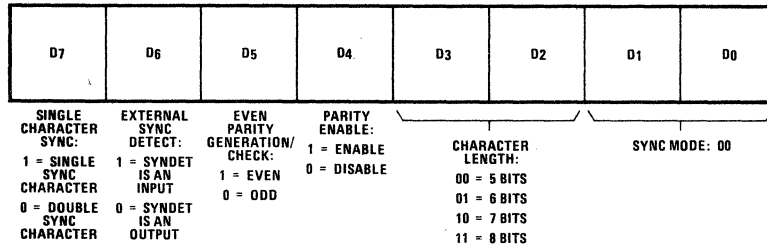
The system software uses a Mode Instruction Control Word and a Command Instruction Control Word (see figures) to establish the complete functional definition of the INS8251. These control words must immediately follow an internal or external reset operation. Once the Mode Instruction Control Word has been written into the INS8251 by the CPU, sync characters (when applicable) or Command Instruction Control Words may be inserted as shown in the typical data block transfer diagram.

Pin Configuration



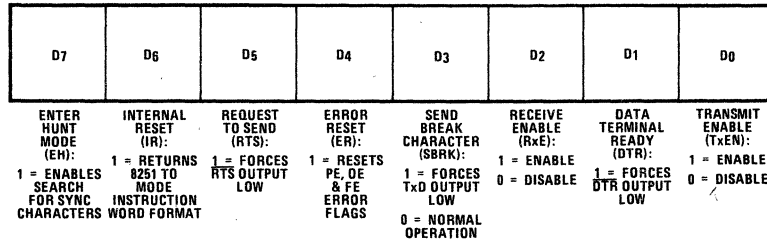


ASYNCHRONOUS MODE

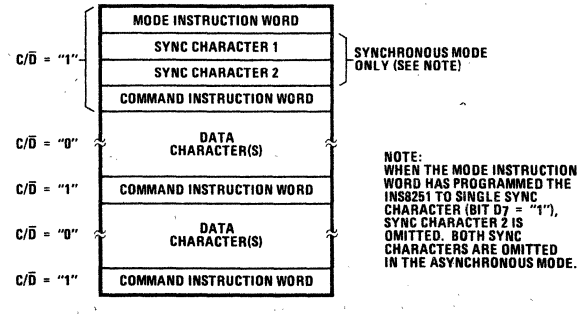


SYNCHRONOUS MODE

mode instruction control word format



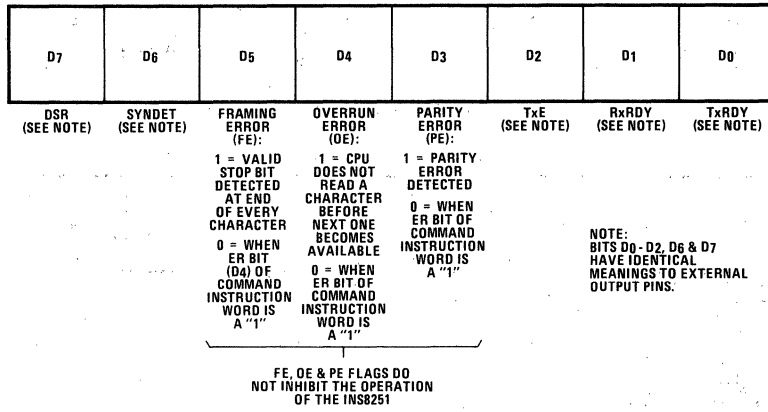
command instruction control word format



typical data block transfer

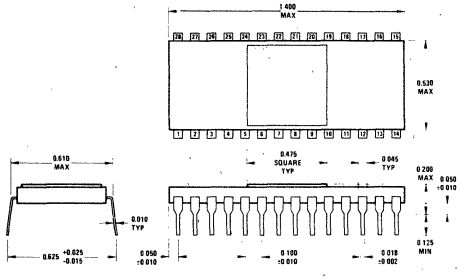
INS8251 Status

The INS8251 has provisions for allowing the programmer to read the status of the device at any time during the functional operation. When the C/$\overline{D}$ input is a high-level, a normal read operation is executed to read this status information. The figure below shows the bits in the Status Read Word format. Since some of the status word bits have identical meaning to external output pins, the INS8251 can be used in a completely polled environment or in an interrupt driven environment.

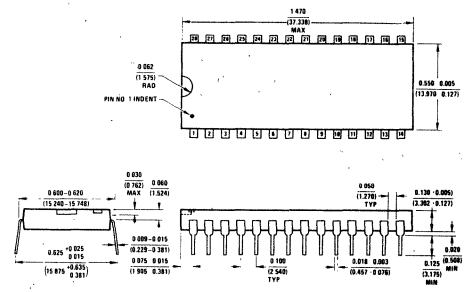


status read word format

Physical Dimensions



28-Lead Cavity DIP (D)
Order Number INS8251D
N.S. Package Number D28A



28-Lead Molded DIP (N)
Order Number INS8251N
N.S. Package Number N28A

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