National Semiconductor

APRIL 1978

INS8255 Programmable Peripheral Interface

General Description

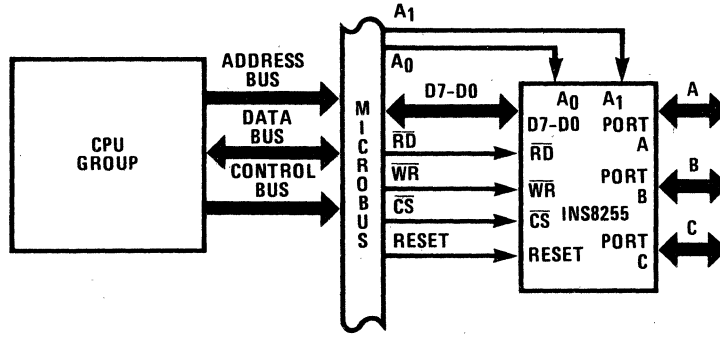
The INS8255 is a programmable peripheral interface contained in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a general-purpose parallel input/output interface in National Semiconductor's N8080 microcomputer family. The functional configuration of the INS8255 is programmed by the system software so that normally no external logic is required to interface peripheral devices.

The INS8255 has three basic modes of operation that can be selected by the system software. In the first mode (Mode 0), the INS8255 provides simple input and output operations for three 8-bit ports. Data is simply written to or read from a specified port (Port A, B or C) without the use of "handshaking" signals. In the second mode (Mode 1), the INS8255 enables the transfer of input/output data to or from a specified 8-bit port (Port A or B) in conjunction with strobes or "handshaking" signals. Ports A and B use the lines of Port C in this mode to generate or accept the "handshaking" signals with the peripheral device. In the third mode (Mode 2), the INS8255 enables communications with a peripheral device or structure via one bidirectional 8-bit bus port (Port A). "Handshaking" signals are provided over the lines of Port C in this mode to maintain proper bus flow discipline.

Features

- Outputs Source 1 mA at 1.5 Volts
- 24 Programmable Input/Output Pins
- Direct Bit Set/Reset Capability
- TTL Compatible
- Reduces System Component Count
- MICROBUS™* Compatible

INS8255 MICROBUS Configuration



Typical Diagram of MODE 0 operation. The 8 bit ports A, B, C are defined by the user's program to be either an input or an output from/to the peripherals.

*Trademark, National Semiconductor Corp.

DC Electrical Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = +5\,V \pm 5\%$; $V_{SS} = 0\,V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 1.6\,mA$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -50\,\mu A$ ($-100\,\mu A$ for D.B. Port)
I_{OH}[1]	Darlington Drive Current		2.0		mA	$V_{OH} = 1.5\,V$, $R_{EXT} = 390\,\Omega$
I_{CC}	Power Supply Current		40		mA	

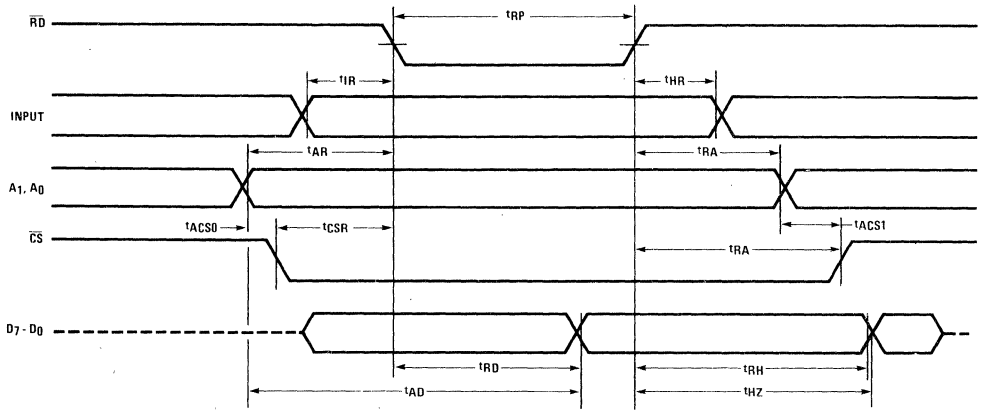
NOTE:
1. Available on 8 pins only of ports B and C. Selected randomly.

AC Electrical Characteristics

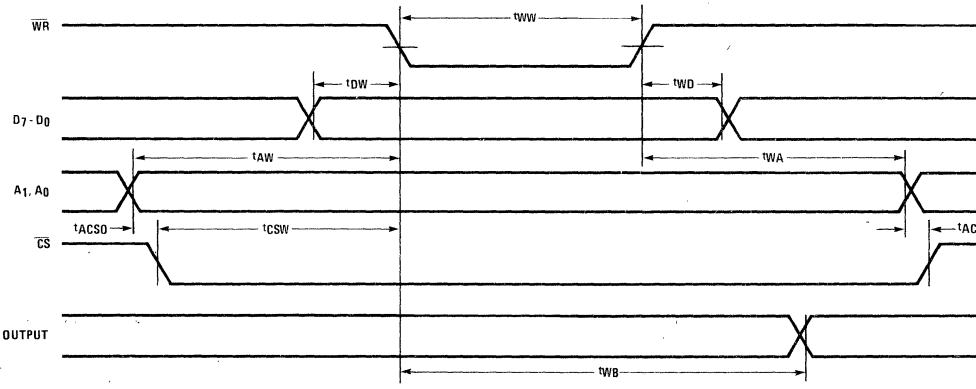
$T_A = 0°C$ to $+70°C$; $V_{CC} = +5\,V \pm 5\%$, $V_{SS} = 0\,V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WW}	Pulse Width of $\overline{WR}$	400			ns	
t_{DW}	Time D.B. Stable before $\overline{WR}$	50			ns	
t_{WD}	Time D.B. Stable after $\overline{WR}$	35			ns	
t_{AW}	Time Address Stable before $\overline{WR}$	20			ns	
t_{WA}	Time Address Stable after $\overline{WR}$	20			ns	
t_{CSW}	Chip Select on to $\overline{WR}$		450		ns	
t_{WB}	Delay from $\overline{WR}$ to Output			500	ns	
t_{RP}	Pulse Width of $\overline{RD}$	405			ns	
t_{IR}	$\overline{RD}$ Set-Up Time	0			ns	
t_{HR}	Input Hold Time	100			ns	
t_{RD}	Delay from $\overline{RD} = 0$ to System Bus			295	ns	
t_{RH}	Delay from $\overline{RD} = 1$ to System Bus			150	ns	
t_{HZ}	$\overline{RD} = 0$ to TRI-STATE of Bus Drivers	10		150	ns	
t_{AR}	Time Address Stable before $\overline{RD}$	50			ns	
t_{CSR}	Time $\overline{CS}$ Stable before $\overline{RD}$		70		ns	
t_{AK}	Width of $\overline{ACK}$ Pulse	500			ns	
t_{ST}	Width of $\overline{STB}$ Pulse	500			ns	
t_{PS}	Set-Up Time for Peripheral	60			ns	
t_{PH}	Hold Time for Peripheral	180			ns	
t_{RA}	Hold Time, Address Bus Trailing Edge to $\overline{RD}$	0			ns	
t_{RC}	Hold Time for $\overline{CS}$ after $\overline{RD} = 1$	5			ns	
t_{AD}	Address Bus Valid to Data Valid			400	ns	
t_{KD}	Time from $\overline{ACK} = 1$ to Output Floating	20		480	ns	
t_{WO}	Time from $\overline{WR} = 1$ to $\overline{OBF} = 0$			650	ns	
t_{AO}	Time from $\overline{ACK} = 0$ to $\overline{OBF} = 1$			450	ns	
t_{SI}	Time from $\overline{STB} = 0$ to IBF			450	ns	
t_{RI}	Time from $\overline{RD} = 1$ to IBF = 0			360	ns	
t_{ACS0}	Address Bus Valid to $\overline{CS}$		40		ns	
t_{ACS1}	Address Change to $\overline{CS}$ OFF		40		ns	

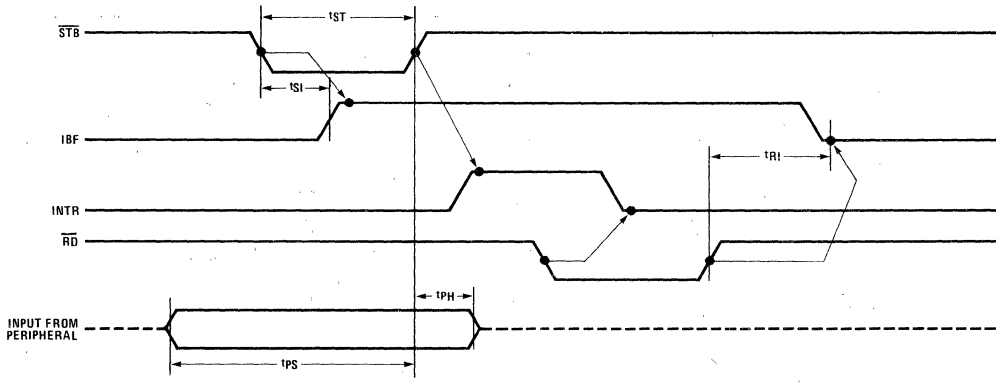
Timing Waveforms



Mode 0 (Basic Input)



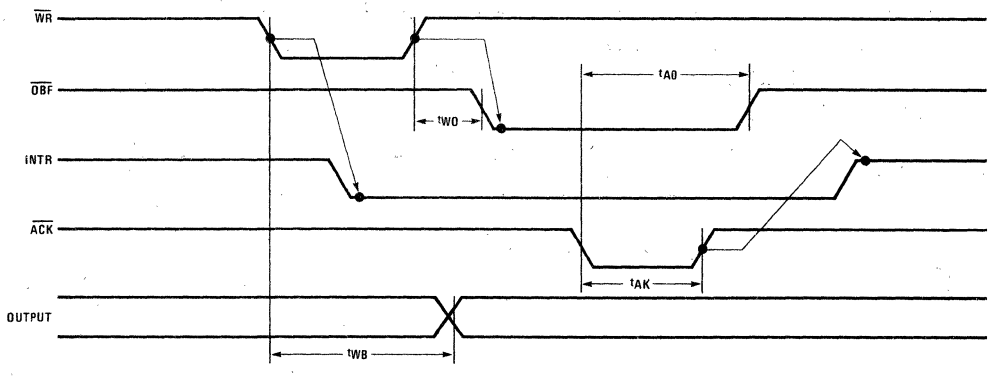
Mode 0 (Basic Output)



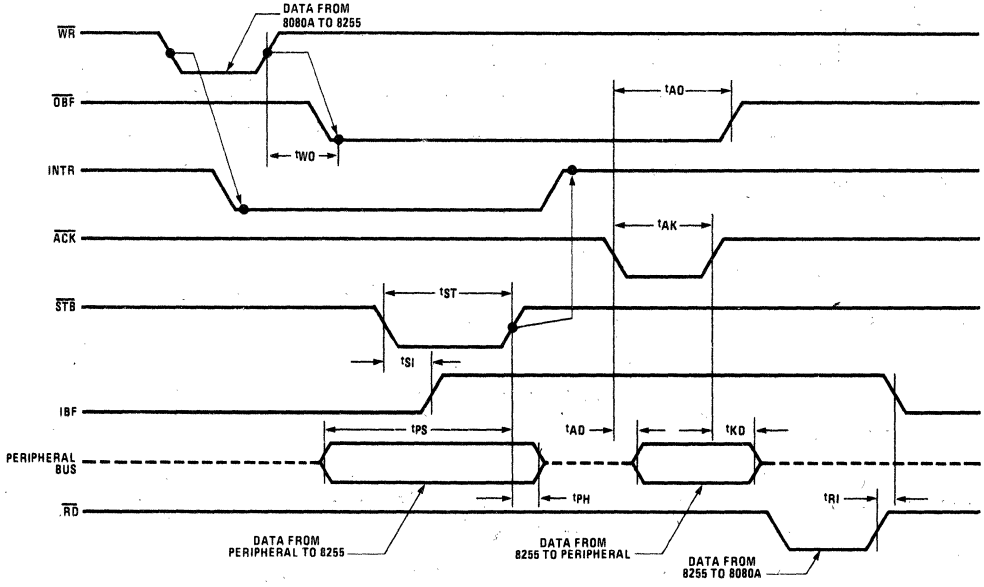
Mode 1 (Strobed Input)

D.2

Timing Waveforms (cont'd.)

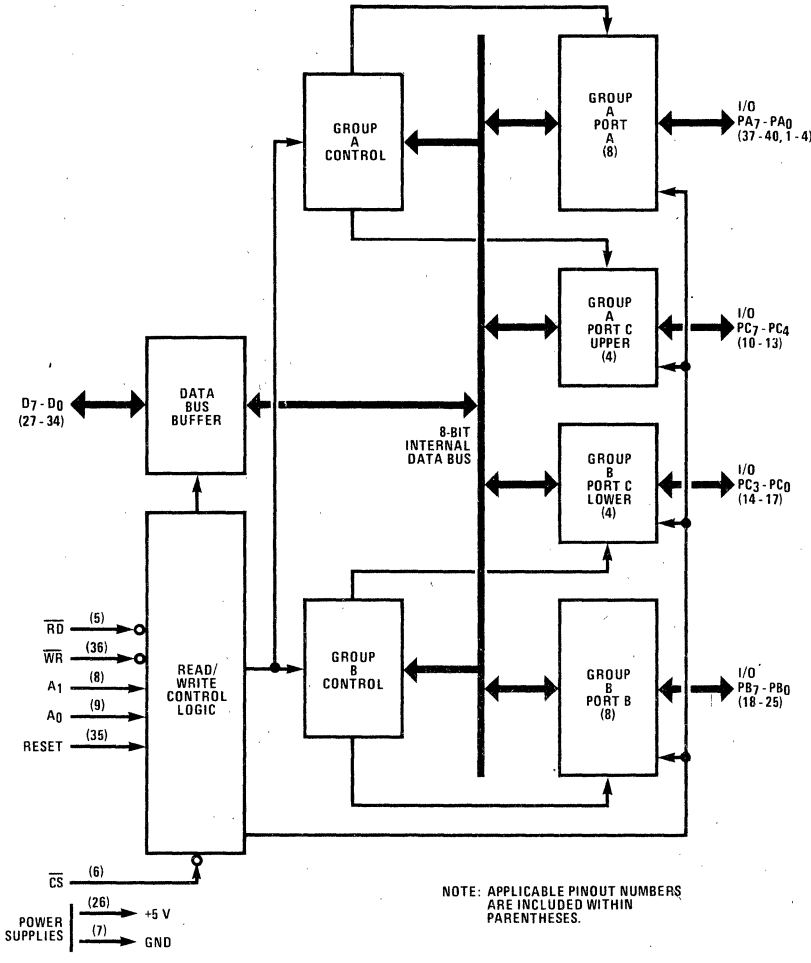


Mode 1 (Strobed Output)



Mode 2 (Bidirectional)

INS8255 Block Diagram



INS8255 Functional Pin Definitions

The following describes the function of all the INS8255 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Chip Select ($\overline{CS}$), Pin 6: When low, the chip is selected. This enables communication between the INS8255 and the INS8080A microprocessor.

Read ($\overline{RD}$), Pin 5: When low, allows the INS8080A to read data or status information from the INS8255.

Write ($\overline{WR}$), Pin 36: When low, allows the INS8080A to write data or control words into the INS8255.

Port Select (A_0, A_1), Pins 9 and 8: These two inputs, which are normally connected to the least significant bits of the A_{15}-A_0 Address Bus, control the selection of one of three 8-bit ports (A, B and C) or the internal control word register as indicated below.

A_1	A_0	Selected
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control Word Register

Reset, Pin 35: When high, clears all the internal registers of the chip and sets Ports A, B and C to the input high impedance mode.

+5 Volts, Pin 26: V_{CC} supply.

Ground, Pin 7: 0 Volt reference.

D.2

INPUT/OUTPUT SIGNALS

Data (D_7-D_0) Bus, Pins 27-34: This bus comprises eight TRI-STATE input/output lines. The bus provides bi-directional communication between the INS8255 and the INS8080A. Data is routed to or from the internal data bus buffer upon execution of an OUT or IN Instruction, respectively, by the INS8080A. In addition, control words and status information are transferred through the data bus buffer.

Port A (PA_7-PA_0), Pins 37-40, 1-4: This 8-bit input/output port forms one 8-bit data output latch/buffer and/or one 8-bit data input latch.

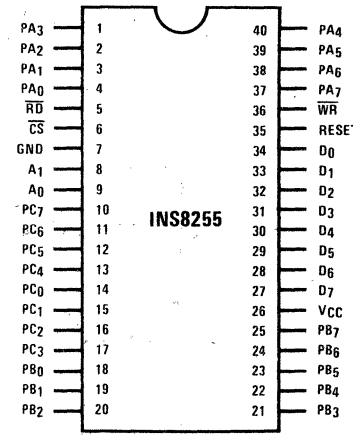
NOTE

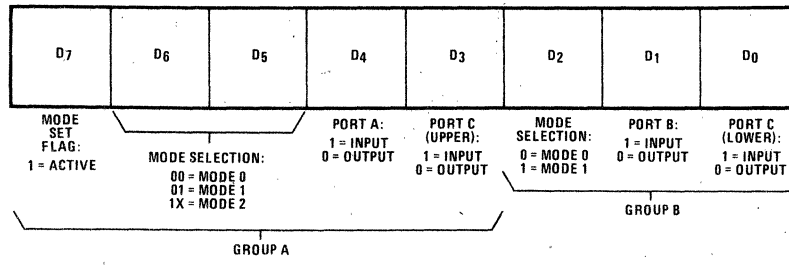
The system software uses a Mode Definition Control Word (see figure) as the second byte of OUT Instruction(s) to program the functional configuration of Ports A through C. Whenever the mode is changed, all output registers (and status flip-flops) are reset.

Port B (PB_7-PB_0), Pins 18-25: This 8-bit input/output port forms one 8-bit data output latch/buffer or one 8-bit data input buffer.

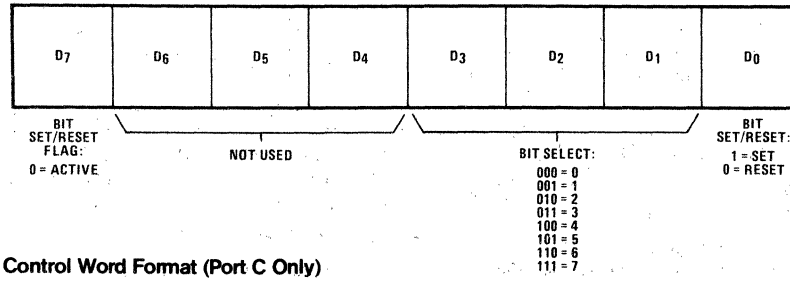
Port C (PC_7-PC_0), Pins 10-17: This 8-bit input/output port forms one 8-bit data output latch/buffer or one 8-bit data input buffer. The port can be split into two 4-bit ports under the mode control. Each of these 4-bit ports contains a 4-bit latch that may be used for the control and status signals, in conjunction with Ports A and B. The system software includes a Bit Set/Reset Control Word (see figure) for setting or resetting any of the eight bits of Port C. When Port C is being used as a status/control for Port A or B, the Port C bits can be set or reset by using the Bit Set/Reset Control Word as the second byte of OUT Instruction(s).

Pin Configuration





Mode Definition Control Word Format



Bit Set/Reset Control Word Format (Port C Only)

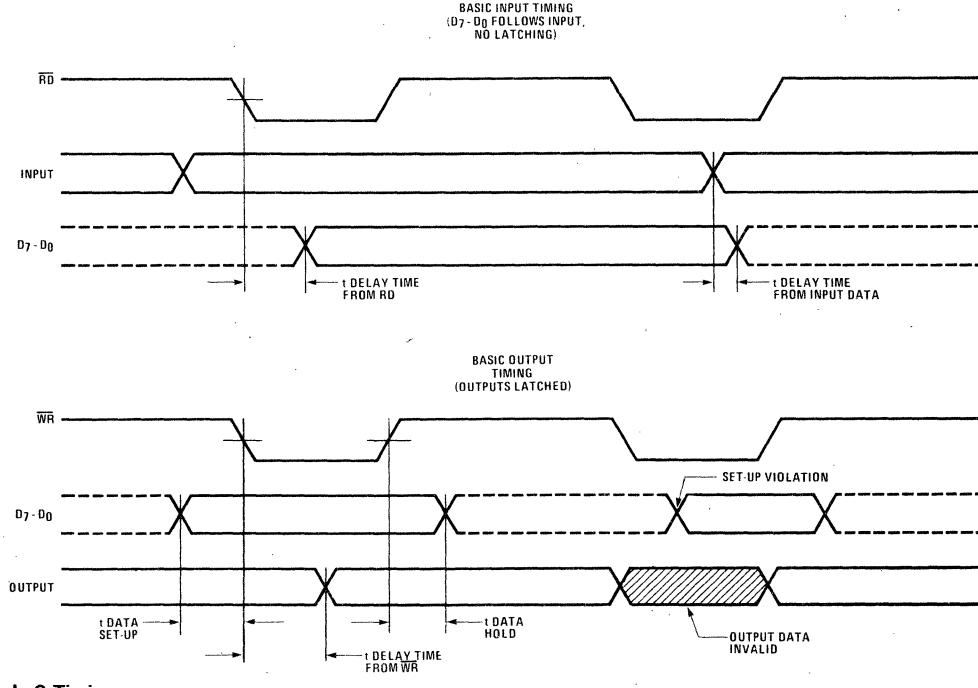
Operating Modes

Mode 0 (Basic Input/Output)

In this mode, simple input and output operations for each of the three ports are provided. No "handshaking" is required; data is simply written to or read from a specified port.

Mode 0 Port Definition Chart

No.	Control Word Bits								Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port A	Port C (Upper)	Port B	Port C (Lower)
0	1	0	0	0	0	0	0	0	OUTPUT	OUTPUT	OUTPUT	OUTPUT
1	1	0	0	0	0	0	0	1	OUTPUT	OUTPUT	OUTPUT	INPUT
2	1	0	0	0	0	0	1	0	OUTPUT	OUTPUT	INPUT	OUTPUT
3	1	0	0	0	0	0	1	1	OUTPUT	OUTPUT	INPUT	INPUT
4	1	0	0	0	1	0	0	0	OUTPUT	INPUT	OUTPUT	OUTPUT
5	1	0	0	0	1	0	0	1	OUTPUT	INPUT	OUTPUT	INPUT
6	1	0	0	0	1	0	1	0	OUTPUT	INPUT	INPUT	OUTPUT
7	1	0	0	0	1	0	1	1	OUTPUT	INPUT	INPUT	INPUT
8	1	0	0	1	0	0	0	0	INPUT	OUTPUT	OUTPUT	OUTPUT
9	1	0	0	1	0	0	0	1	INPUT	OUTPUT	OUTPUT	INPUT
10	1	0	0	1	0	0	1	0	INPUT	OUTPUT	INPUT	OUTPUT
11	1	0	0	1	0	0	1	1	INPUT	OUTPUT	INPUT	INPUT
12	1	0	0	1	1	0	0	0	INPUT	INPUT	OUTPUT	OUTPUT
13	1	0	0	1	1	0	0	1	INPUT	INPUT	OUTPUT	INPUT
14	1	0	0	1	1	0	1	0	INPUT	INPUT	INPUT	OUTPUT
15	1	0	0	1	1	0	1	1	INPUT	INPUT	INPUT	INPUT



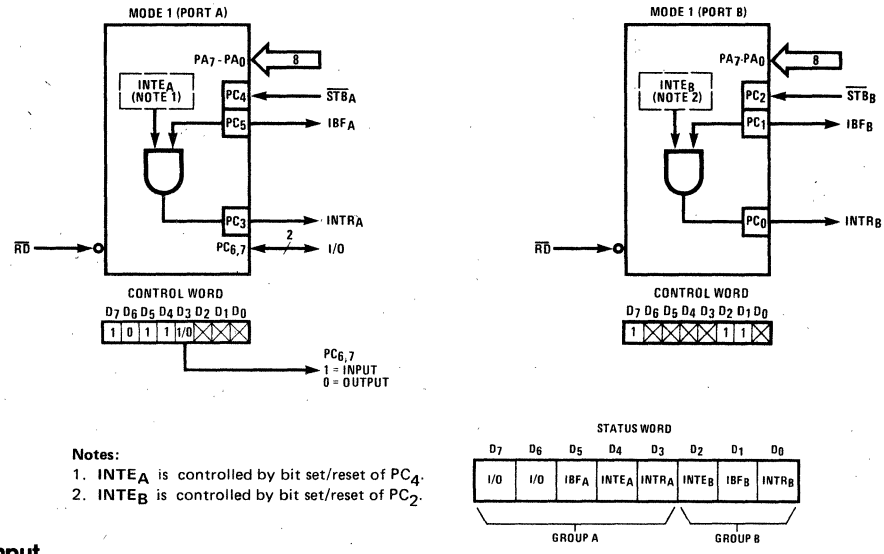
Mode 0 Timing

D.2

Operating Modes (cont'd.)

Mode 1 (Strobed Input/Output)

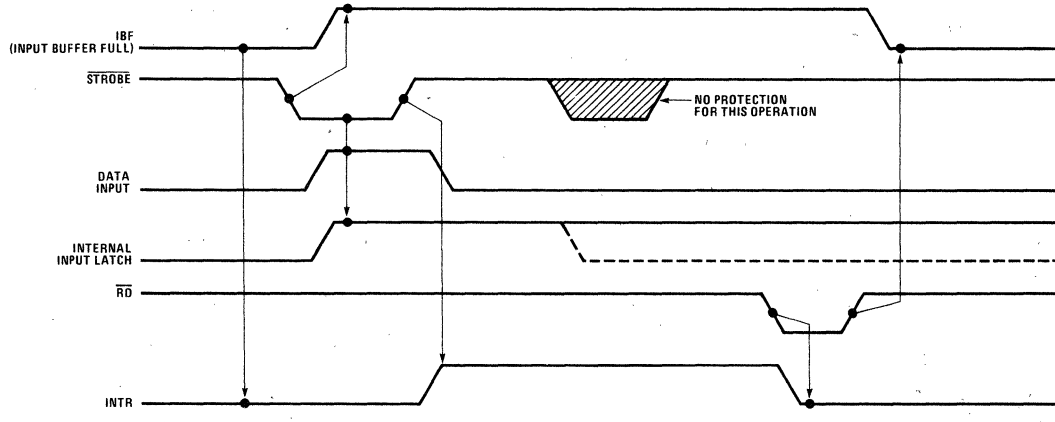
In this mode, a means for transferring input/output data to or from a specified port in conjunction with strobes or "handshaking" signals is provided. Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals in Mode 1. The programmer can read the contents of Port C to test or verify the status of each peripheral device. Since no special instruction is provided in the INS8080A microcomputer system to read the Port C status information, a normal read operation must be executed to perform this function.



Notes:

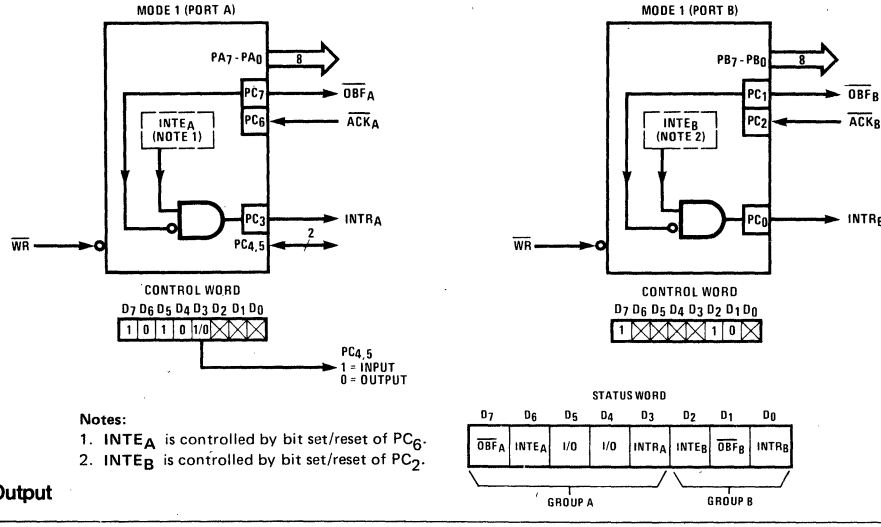
1. $INTE_A$ is controlled by bit set/reset of PC_4.
2. $INTE_B$ is controlled by bit set/reset of PC_2.

Mode 1 Input



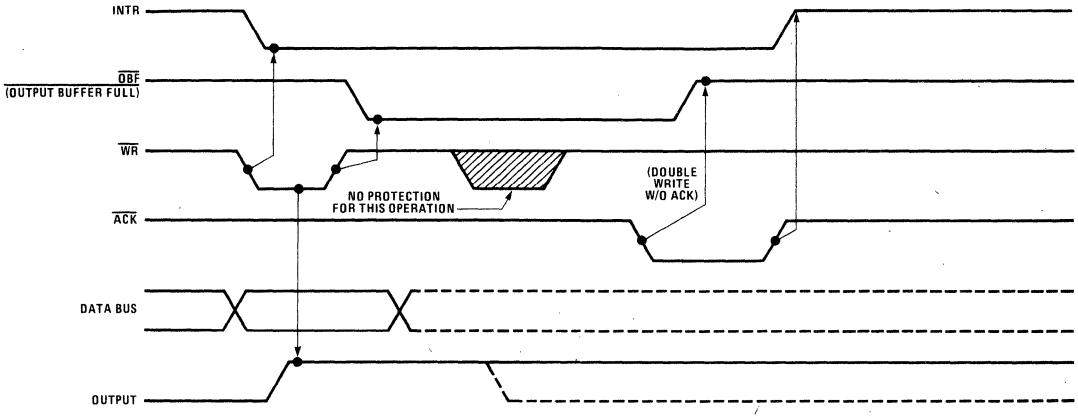
Mode 1 Input Timing

Operating Modes (cont'd.)

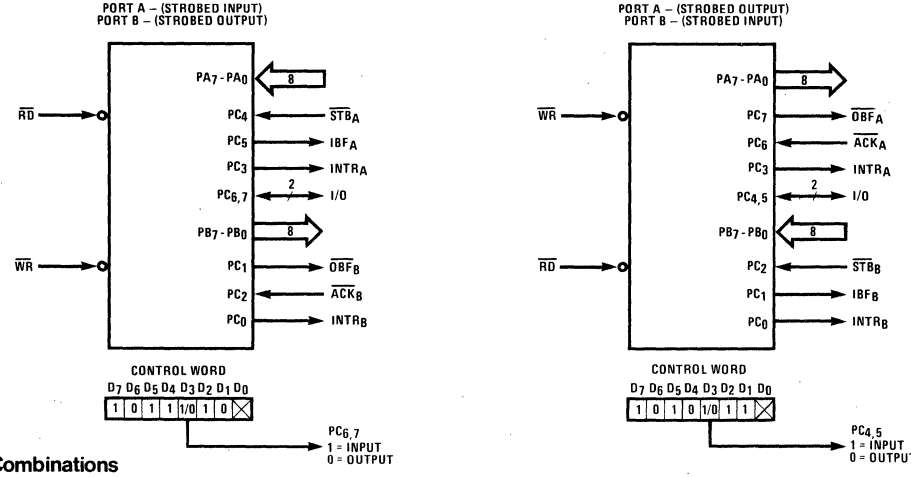


Notes:
1. $INTE_A$ is controlled by bit set/reset of PC_6.
2. $INTE_B$ is controlled by bit set/reset of PC_2.

Mode 1 Output



Mode 1 Output Timing



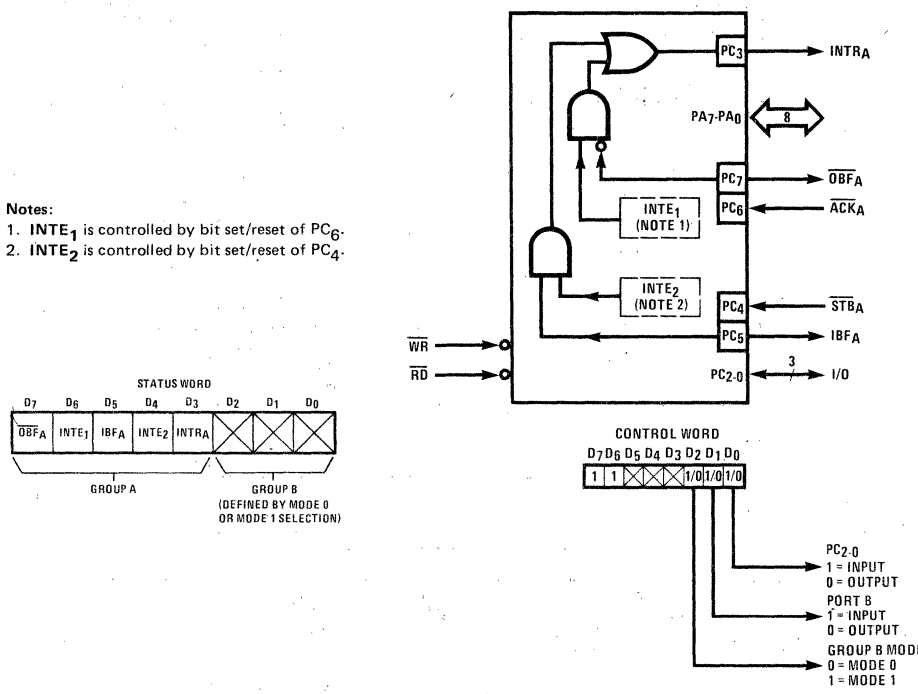
Mode 1 Combinations

D.2

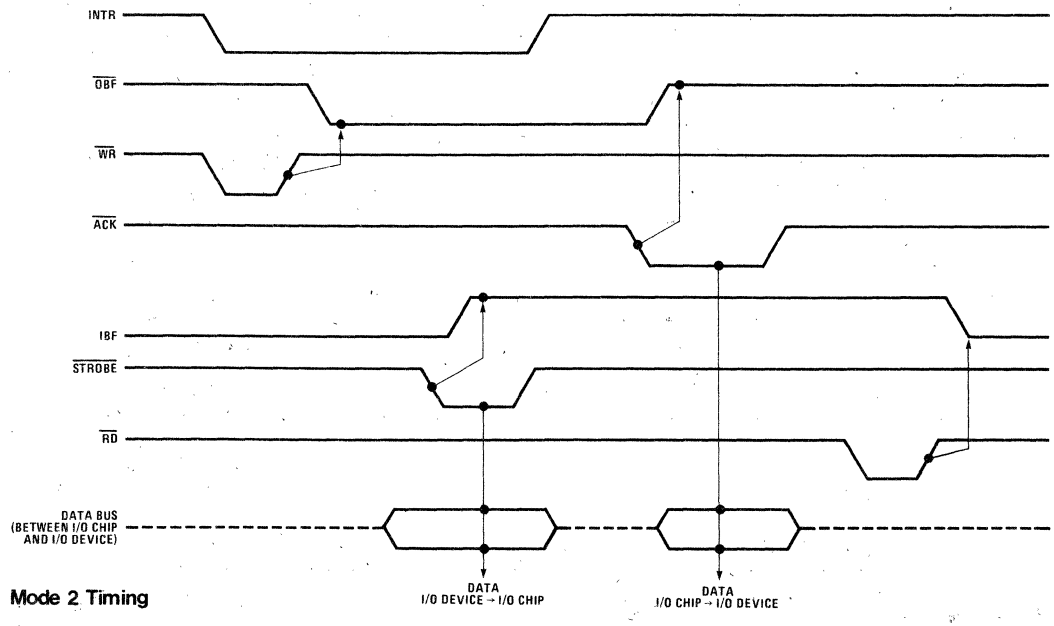
Operating Modes (cont'd.)

Mode 2 (Strobed Bidirectional Bus Input/Output)

This mode enables communication with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus input/output). "Handshaking" signals are provided to maintain proper bus flow discipline in a manner similar to Mode 1. In addition, interrupt generation and enable/disable functions are available in Mode 2.



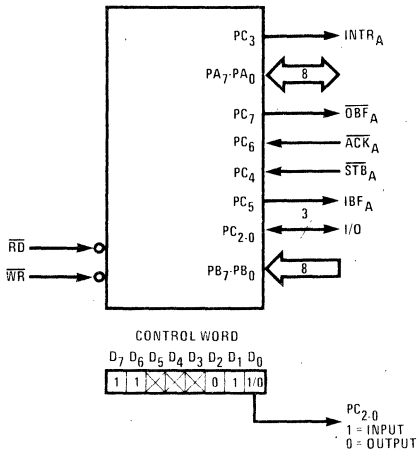
Mode 2



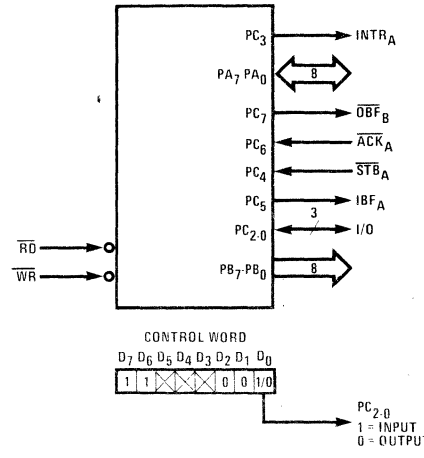
Mode 2 Timing

Operating Modes (cont'd.)

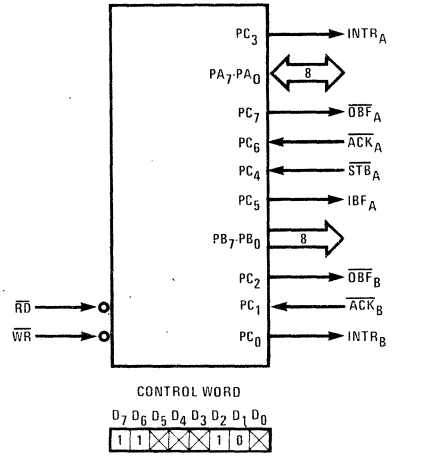
MODE 2 AND MODE 0 (INPUT)



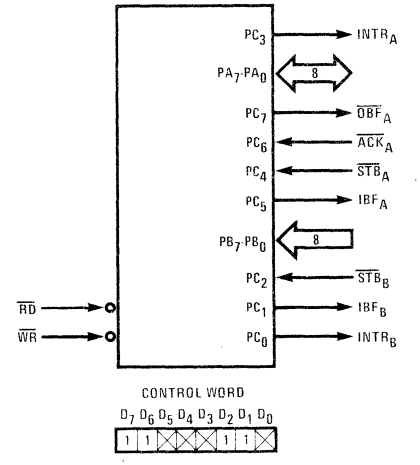
MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)



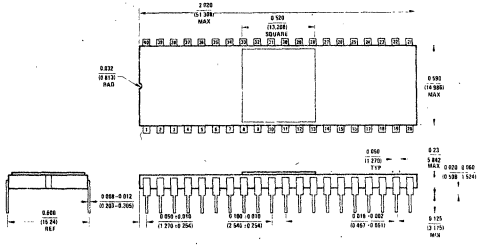
D.2

Mode 2 Combinations

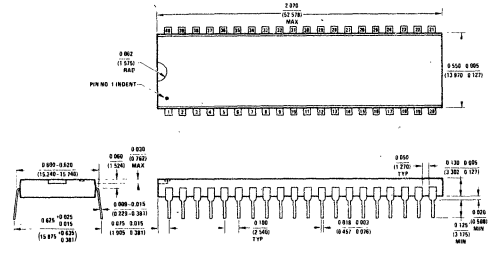
Mode Definition Summary Table

Port Bits	Mode 0		Mode 1		Mode 2
	IN	OUT	IN	OUT	Group A Only
PA_0	IN	OUT	IN	OUT	Bidirectional
PA_1	IN	OUT	IN	OUT	↕
PA_2	IN	OUT	IN	OUT	
PA_3	IN	OUT	IN	OUT	
PA_4	IN	OUT	IN	OUT	
PA_5	IN	OUT	IN	OUT	
PA_6	IN	OUT	IN	OUT	
PA_7	IN	OUT	IN	OUT	Bidirectional
PB_0	IN	OUT	IN	OUT	
PB_1	IN	OUT	IN	OUT	
PB_2	IN	OUT	IN	OUT	
PB_3	IN	OUT	IN	OUT	(Mode 0 or Mode 1 only)
PB_4	IN	OUT	IN	OUT	
PB_5	IN	OUT	IN	OUT	
PB_6	IN	OUT	IN	OUT	
PB_7	IN	OUT	IN	OUT	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

Physical Dimensions



Ceramic Dual-In-Line Package (D)
Order Number INS8255D



Plastic Dual-In-Line Package (N)
Order Number INS8255N

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