National Semiconductor

Preliminary

JULY 1978

INS8257 Programmable DMA Controller

General Description

The INS8257 is a Direct Memory Access (DMA) controller contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, performs direct control of high speed data transfers to and from memory over four separate channels. Data can be transferred in single bytes or in blocks containing up to 16,384 bytes.

The INS8257 accepts requests for memory access from peripheral devices attached to its four DMA channels and acquires control of the system bus whenever the DMA request is honored. Competing requests are resolved according to a programmable priority scheme (fixed or rotating).

Program control of the INS8257 is exercised via a mode set register and four pairs of channel control registers (one pair per channel). A status register is also included, which provides terminal count status for each channel. The status register also contains a register programming flag, which is a valuable aid in maintaining byte synchronization when programming channel control registers.

The mode set register contains four individual channel enable bits plus option select bits for the following options: rotating priority, extended write, TC stop and auto load.

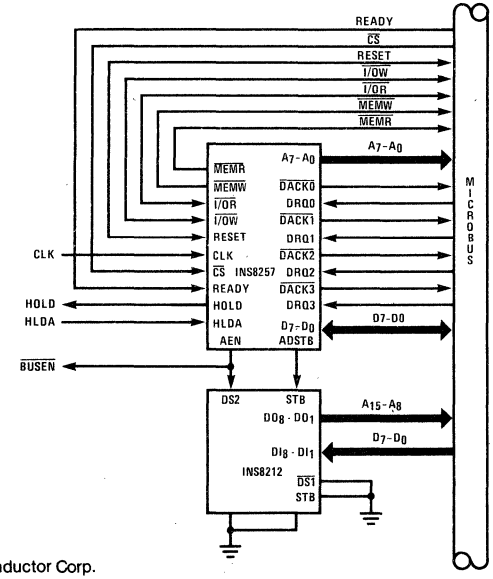
The channel control registers consist of four 16-bit DMA address registers and four 16-bit terminal count (TC) registers. These registers provide the means for controlling DMA transfers on their respective channels.

The auto load feature permits the repetition of block transfers or the chaining of data blocks with a minimum of register initialization required.

Features

- Four-Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Auto Load Mode
- Single TTL Clock
- Single +5V Supply
- Expandable
- MICROBUS™* Compatible

INS8080 Family CPU Group MICROBUS Configuration



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Absolute Maximum Ratings

Maximum Voltage to Any Input with Respect to GND ..... −0.5V to +7V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation ..... 1 Watt

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	**Input Low Voltage**	−0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4	V_{CC}	Volts	I_{OH} = −150μA for AB, DB and AEN I_{OH} = −80μA for others
V_{HH}	HRQ Output High Voltage	3.3	V_{CC}	Volts	I_{OH} = −80μA
I_{CC}	V_{CC} Current Drain		120	mA	
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC}
I_{OFL}	Output Leakage During Float		10	μA	V_{OUT} (Note 1)

Note 1: $V_{CC} > V_{OUT} >$ GND + 0.45V.

Capacitance T_A = 25°C, V_{CC} = *GND* = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	**Input Capacitance**		**10**	**pF**	f_C = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND

AC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, GND = 0V (Note 1)

Bus Parameters
READ CYCLE

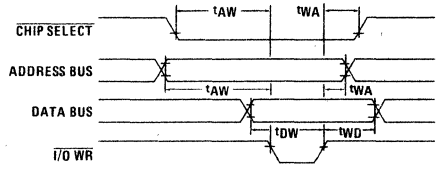
Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AR}	**Adr or CS↓** Setup to RD↓	0		ns	
t_{RA}	Adr or CS↑ Hold from RD↑	0		ns	
T_{RD}	Data Access from RD↓	0	300	ns	(Note 2)
t_{DF}	DB → Float Delay from RD↑	20	150	ns	
t_{RR}	RD Width	250		ns	
WRITE CYCLE					
t_{AW}	Adr Setup to WR↓	20		ns	
t_{WA}	Adr Hold from WR↑	0		ns	
t_{DW}	Data Setup to WR↑	200		ns	
t_{WD}	Data Hold from WR↑	0		ns	
t_{WW}	WR Width	200		ns	
OTHER TIMING					
t_{RSTW}	Reset Pulse Width	300		ns	
t_{RSTD}	Power Supply↑ (V_{CC}) Setup to Reset↓	500		ns	
t_R	Signal Rise Time		20	ns	
t_F	Signal Fall Time		20	ns	
t_{RSTS}	Reset to First IOWR	2		t_{CY}	

Note 1: All timing measurements are made at the following reference voltages unless otherwise specified: Input "1" at 2.0V, "0" at 0.8V; Output "1" at 2.0V, "0" at 0.8V.

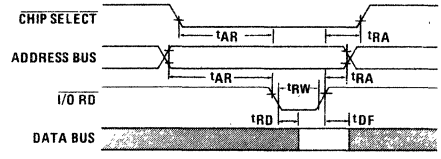
Note 2: C_L = 100pF.

Timing Waveforms (Peripheral Mode)

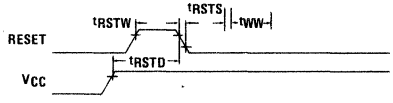
Write Timing



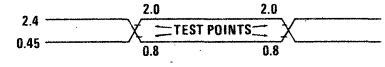
Read Timing



Reset



Input Waveforms for AC Tests



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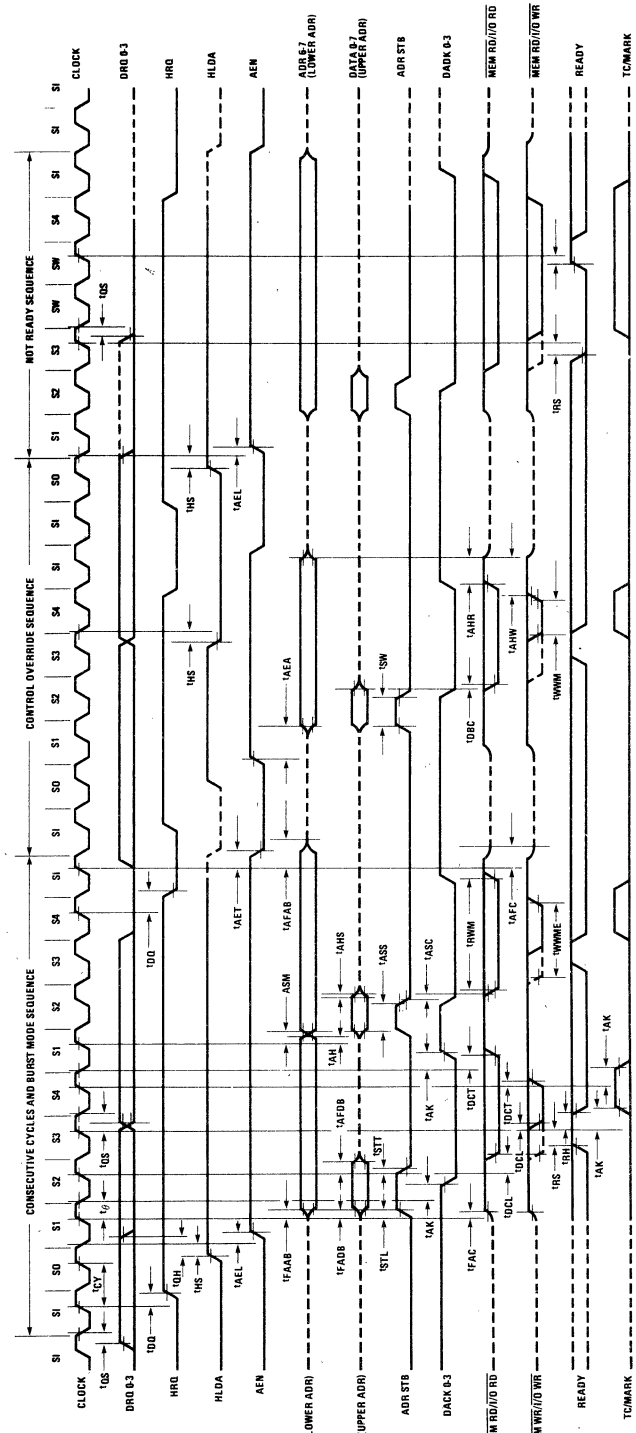
AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, GND = 0V

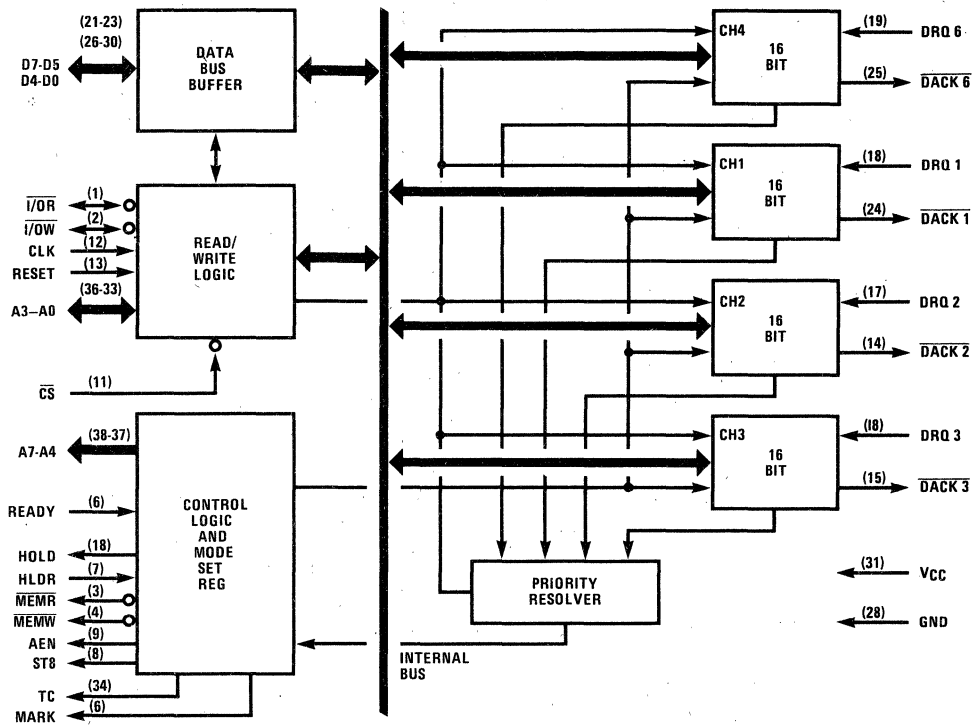
DMA (Master) Mode

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{CY}	**Cycle Time (Period)**	**0.320**	**4**	μs	
t_θ	Clock Active (High)	120	$0.8t_{CY}$	ns	
t_{QS}	DRQ↑ Setup to θ↓(SI,S4)	120		ns	
t_{QH}	DRQ↓ Hold from HLDA↑	0			Tracking Specification
t_{DQ}	HRQ↑ or ↓Delay from θ↑(SI,S4) at 2.0V)		160	ns	Load = 1 TTL
t_{DQ1}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 3.3V)		160	ns	Load = 1 TTL + (R_L = 3.3k), V_{OH} = 3.3V
t_{HS}	HLDA↑ or ↓Setup to θ↓(SI,S4)	100		ns	
t_{AEL}	AEN↑ Delay from θ↓(S1)		300	ns	Load = 1 TTL
t_{AET}	AEN↓ Delay from θ↑(SI)		200	ns	Load = 1 TTL
t_{AEA}	Adr(AB) (Active) Delay from AEN↑(S1)	20		ns	Tracking Specification
t_{FAAB}	Adr(AB) (Active) Delay from θ↑(S1)		250	ns	Load = 1 TTL + 50pF
t_{AFAB}	Adr(AB) (Float) Delay from θ↑(SI)		150	ns	Load = 1 TTL + 50pF
t_{ASM}	Adr(AB) (Stable) Delay from θ↑(S1)		250	ns	Load = 1 TTL + 50pF
t_{AH}	Adr(AB) (Stable) Hold from θ↑(S1)	$t_{ASM} - 50$		ns	Load = 1 TTL + 50pF
t_{AHR}	Adr(AB) (Valid) Hold from Rd↑(S1,SI)	60		ns	Tracking Specification
t_{AHW}	Adr(AB) (Valid) Hold from Wr↑(S1,SI)	300		ns	Tracking Specification
t_{FADB}	Adr(DB) (Active) Delay from θ↑(S1)		300	ns	Load = 1 TTL + 50pF
t_{AFDB}	Adr(DB) (Float) Delay from θ↑(S2)	$t_{SST} + 20$	250	ns	Load = 1 TTL + 50pF
t_{ASS}	Adr(DB) Setup to AdrStb↓(S1-S2)	100		ns	Tracking Specification
t_{AHS}	Adr(DB) (Valid) Hold from AdrStb↓(S2)	50		ns	Tracking Specification
t_{STL}	AdrStb↑ Delay from θ↑(S1)		200	ns	Load = 1 TTL
t_{STT}	AdrStb↓ Delay from θ↑(S2)		140	ns	Load = 1 TTL
t_{SW}	AdrStb Width (S1-S2)	$t_{CY} - 100$		ns	Tracking Specification
t_{ASC}	Rd↓ or Wr(Ext)↓ Delay from AdrStb↓(S2)	70		ns	Tracking Specification
t_{DBC}	Rd↓ or Wr(Ext)↓ Delay from Adr(DB) (Float)(S2)	20		ns	Tracking Specification
t_{AK}	DACK↑ or ↓Delay from θ↓(S2,S1) and TC/Mark↑ Delay from θ↑(S3) and TC/Mark↓ Delay from θ↑(S4)		250	ns	Load = 1 TTL, $\Delta t_{AK} < 50ns$
t_{DCL}	Rd↓ or Wr(Ext)↓ Delay from θ↑(S2) and Wr↓ Delay from θ↑(S3)		200	ns	Load = 1 TTL + 50pF, $\Delta t_{DCL} < 50ns$
t_{DCT}	Rd↑ Delay from θ↓(S1,SI) and Wr↑ Delay from θ↑(S4)		200	ns	Load = 1 TTL + 50pF, $\Delta t_{DCT} < 50ns$
t_{FAC}	Rd or Wr (Active) from θ↑(S1)		300	ns	Load = 1 TTL + 50pF
t_{AFC}	Rd or Wr (Float) from θ↑(SI)		150	ns	Load = 1 TTL + 50pF
t_{RWM}	Rd Width (S2-S1 or SI)	$2t_{CY} + t_\theta - 50$		ns	Tracking Specification
t_{WWM}	Wr Width (S3-S4)	$t_{CY} - 50$		ns	Tracking Specification
t_{WWME}	Wr(Ext) Width (S2-S4)	$2t_{CY} - 50$		ns	Tracking Specification
t_{RS}	READY Setup Time to θ↑(S3,Sw)	30		ns	
t_{RH}	READY Hold Time from θ↑(S3,Sw)	20		ns	

Timing Waveforms (DMA Mode)



INS8257 Functional Block Diagram



NOTE: APPLICABLE PINOUT NUMBERS ARE INCLUDED WITHIN PARENTHESES.

INS8257 Functional Pin Description

The following describes the functions of all INS8257 input/output pins. Some of these descriptions refer to internal circuits.

INPUT SIGNALS

Data Request (DRQ0-DRQ3): Each channel interface has a separate DRQ input, which is used by the peripheral to request DMA cycles. To make a request for DMA service, a peripheral raises its DRQ line and holds it high so long as DMA cycles are needed. The peripheral drops its DRQ n when the DMA acknowledge ($\overline{DACK}$ n) is received for the last DMA cycle in the data block. See Output Signals for a description of the $\overline{DACK}$ signal.

Clock (CLK): This clock is supplied by the $\phi 2$ (TTL) output of the INS8224 Clock Generator and Driver (pin 6) or its equivalent.

Reset: When raised to the high logic level, this input clears all INS8257 registers and control lines, excepting the channel address registers. It would normally be supplied by the INS8224 Clock Generator and Driver (pin 1) or its equivalent.

Chip Select ($\overline{CS}$): When this input is low, the chip is selected. This enables the INS8257 read/write interface logic.

Ready: This input inserts wait states into the INS8257's memory read and write cycles if required by the addressed memory.

Hold Acknowledge (HLDA): When high, this input from the CPU notifies the INS8257 that it has control of the system bus.

OUTPUT SIGNALS

DMA Acknowledge ($\overline{DACK3}$-$\overline{DACK0}$): Each channel interface has a separate DMA acknowledge output. When a channel's DMA request (DRQ) is honored by the priority logic, that channel's $\overline{DACK}$ output is brought low to notify the peripheral that it has been selected for a DMA cycle.

Address Lines (A7-A4): These four TRI-STATE® address outputs carry bits 7 through 4 of the memory address produced by the INS8257 during the addressing phase of DMA cycles.

Hold Request (HRQ): The INS8257 raises this output in order to request control of the system bus.

Memory Read ($\overline{MEMR}$): The INS8257 brings this TRI-STATE output low in order to read data from memory during DMA read operations.

Memory Write ($\overline{MEMW}$): The INS8257 brings this TRI-STATE output low in order to write data into memory during DMA write operations.

Address Strobe (ADSTB): The INS8257 uses this output to strobe address bits A15-A8 from the INS8257's bidirectional data lines (D7-D0) into the memory's address buffer (e.g., INS8212).

Address Enable (AEN): The INS8257 may use this output to disable the system data bus and the system control bus. It does this by applying AEN to the Bus Enable input of the CPU's System Controller chip (e.g., INS8228). It may also be used to isolate non-DMA devices from the system address bus during DMA operations. This is done by applying AEN to the enable input of each address bus driver chip to be disabled.

Terminal Count (TC): The INS8257 uses this output to notify the selected peripheral that the current DMA cycle is the last cycle in the data block. If the mode set register's TC Stop bit (bit 6) is set, the selected channel is automatically disabled at the end of that DMA cycle. The INS8257 control logic issues TC when the terminal count register decrements to 0 (excluding bits 14 and 15).

Modulo 128 Mark (MARK): The INS8257 uses this output to notify the selected peripheral that 128 DMA cycles have occurred since the previous MARK output. MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block.

INPUT/OUTPUT SIGNALS

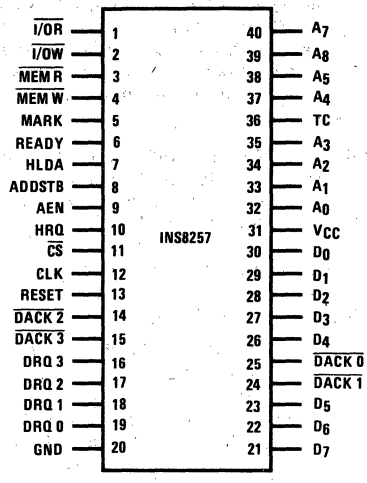
Data (D0-D7) Bus: This bus, which comprises eight TRI-STATE input/output lines, provides for bidirectional communication between the INS8257 and the CPU. When the CPU is initializing the INS8257, this bus may carry data for the DMA address register, terminal count register or mode set register. Read data is carried by these lines when the CPU reads a DMA address register, a terminal count register or the status register. During the address phase of a DMA cycle, these lines carry the eight high-order bits of the memory address. During the data transfer phase of a DMA cycle, this bus carries the data byte being written into or read from memory.

I/O Read ($\overline{I/OR}$): This is a low-true, bidirectional TRI-STATE line. It is used by the CPU to read INS8257 registers (DMA address register, terminal count register or status register) and by the INS8257 to input data from a selected peripheral during DMA write operations.

I/O Write ($\overline{I/OW}$): This is a low-true, bidirectional TRI-STATE line. It is used by the CPU to write into INS8257 registers (DMA address register, terminal count register or mode set register) and by the INS8257 to output data to a selected peripheral during DMA read operations.

Address Lines (A3-A0): These lines, which carry the four least significant system address bits, are bidirectional. They function as input lines when the CPU uses them to select one of the INS8257 registers. They function as output lines during DMA cycles when they carry the four least significant bits of the memory address.

Pin Configuration



INS8257 Programming Information

This section provides basic information for programming the INS8257 and describes the status information available to the programmer. Table 1 summarizes the bus controls needed to output control information to the INS8257 and to read INS8257 status.

Table 1. INS8257 System Bus Controls

Function	A_3	A_2	A_1	A_0	(Note 1) $\overline{I/OW}$	(Note 1) $\overline{I/OR}$	CS
Load Ch0 DMA Address Register	0	0	0	0	0	1	0
Load Ch1	0	0	1	0	0	1	0
Load Ch2	0	1	0	0	0	1	0
Load Ch3	0	1	1	0	0	1	0
Read Ch0 DMA Address Register	0	0	0	0	1	0	0
Read Ch1	0	0	1	0	1	0	0
Read Ch2	0	1	0	0	1	0	0
Read Ch3	0	1	1	0	1	0	0
Load Ch0 TC Register	0	0	0	1	0	1	0
Load Ch1	0	0	1	1	0	1	0
Load Ch2	0	1	0	1	0	1	0
Load Ch3	0	1	1	1	0	1	0
Read Ch0 TC Register	0	0	0	1	1	0	0
Read Ch1	0	0	1	1	1	0	0
Read Ch2	0	1	0	1	1	0	0
Read Ch3	0	1	1	1	1	0	0
Load Mode Set Register	1	0	0	0	0	1	0
Read Status Register	1	0	0	0	1	0	0

Note 1: First $\overline{I/OW}$ or $\overline{I/OR}$ loads or reads low-order byte, second $\overline{I/OW}$ or $\overline{I/OR}$ loads or reads high-order byte.

PROGRAMMING

There are three types of registers that must be initialized:

1. Four DMA address registers (one per channel)
2. Four terminal count registers (one per channel)
3. One mode set register.

The DMA address registers and TC registers can be programmed in any order. However, the mode set register should not be programmed until after the DMA address and TC registers are initialized. This precaution is intended to prevent invalid access of memory in the event a spurious DMA request (DRQ n) is generated.

NOTE

For any transfer on the system data bus involving position-weighted bits, D7 = most significant bit and D0 = least significant bit.

Because each channel register is two bytes wide, two I/O read or write operations are required to read or load an entire register. When one of these registers is selected by the CPU, INS8257 logic automatically accesses the register's lower half for the first I/O operation and the upper half for the second I/O operation.

Part of this logic is a first/last flip-flop (F/L) that toggles with each I/O operation directed to a channel register. This flip-flop controls which half of the register is affected. It is essential that the state of this flip-flop not be lost through any of the following conditions:

- Loading the mode set register when only the lower half of a channel register has been accessed,
- Clocking $\overline{CS}$ while either $\overline{I/OR}$ or $\overline{I/OW}$ is active,
- Allowing the microprocessor to be interrupted when only the lower half of a channel register has been accessed,
- Not completing both halves of a channel register read or load sequence.

LOADING DMA ADDRESS REGISTERS

Each channel is assigned a separate 16-bit DMA address register. This register is loaded with the starting memory address for the next DMA operation to be conducted on the corresponding channel.

Loading of a single DMA address register requires two I/O write operations, with the chip selected by CS and the register selected by system address lines A3-A0.

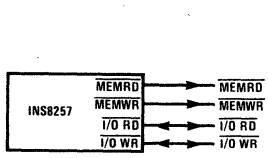
The DMA address information is presented to the INS8257 via the system data bus in the following manner:

	DMA Addr Register		
First $\overline{I/OW}$	LS Byte	←	D7-D0
Second $\overline{I/OW}$	MS Byte	←	D7-D0

LOADING TC REGISTERS

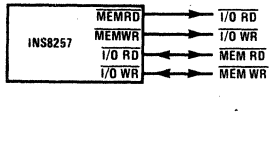
Each channel is assigned a separate TC register. This register's 14 least significant bits are loaded with a value equal to one less than the number of DMA cycles in the channel's next block transfer. For example, if the next DMA operation for channel 0 will require 32 (hex 20) DMA cycles, the value 31 (hex 1F) should be loaded into channel 0's TC register.

Bits 14 and 15 of each TC register are loaded with mode control bits for the corresponding channel. There are three possible operating modes to be specified by these bits. How they are implemented depends on whether the INS8257 is part of a standard (isolated) I/O bus structure or whether a memory-mapped I/O configuration is used. Figure 1 identifies the mode control functions of TC register bits 14 and 15 for both I/O schemes.



Isolated I/O

Function	Bit 15	Bit 14
DMA Verify	0	0
DMA Write	0	1
DMA Read	1	0
Illegal	1	1



Memory Mapped I/O

Function	Bit 15	Bit 14
DMA Verify	0	0
DMA Write	1	0
DMA Read	0	1
Illegal	1	1

Figure 1. TC Register Mode Control Bits

The DMA verify mode allows pseudo DMA cycles to be performed in which no data is transferred. In this mode, the INS8257 responds to DMA requests in the same manner as in other modes, except that $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{I/OR}}$ and $\overline{\text{I/OW}}$ are inhibited. This mode allows a peripheral to cycle through a block of data for internal control or housekeeping purposes without affecting memory.

In a DMA read cycle, the INS8257 issues $\overline{\text{MEMR}}$ in order to read the contents of the addressed memory location and I/O to write that same data byte into the selected peripheral.

In a DMA write cycle, the INS8257 issues $\overline{\text{I/OR}}$ in order to read the data byte presented by the selected peripheral and $\overline{\text{MEMW}}$ to write that same data byte into the addressed memory location.

Loading of a single TC register requires two I/O write operations, with the chip selected by $\overline{\text{CS}}$ and the register selected by system address lines A3-A0.

The terminal count information is presented to the INS8257 via the system data bus in the following manner:

	TC Register		
First $\overline{\text{I/OW}}$	LS Byte	←	D7-D0
Second $\overline{\text{I/OW}}$	MS Byte	←	D7-D0

LOADING MODE SET REGISTER

The contents of the mode set register are used to individually enable/disable the four DMA channels and to selectively implement four optional functions in the INS8257. Mode set register bit functions are identified in figure 2 and are described in the following paragraphs.

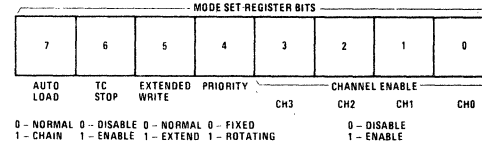


Figure 2. Mode Set Register Bit Functions

Loading the mode set register requires a single I/O write operation, with the chip selected by $\overline{\text{CS}}$ and the register selected by A3-A0.

DMA Channel Enables (Bits 3-0)

These four bits can be individually set or reset by the program in order to enable or disable their respective channels. If the TC stop bit (mode set register bit 6) is set, the channel enable bit of the currently selected channel is automatically reset after Terminal Count (TC) goes true. This assures the disabling of a channel after it completes its DMA operations. If the TC stop bit is not set, the program should reset any channel enable bit whose DMA address and TC registers are not currently valid.

Rotating Priority Option (Bit 4)

When this bit = 0 (e.g., following power on reset), the priority control logic resolves competing DMA requests according to a fixed priority scheme. In this fixed priority mode, channel 0 always has highest priority and channel 3 always has lowest priority.

When mode set register bit 4 is set, the rotating priority mode is selected. In this mode, the completion of a DMA cycle will cause the channel just serviced to be assigned lowest priority. All other channels then move up one priority level. Channel 0 will always have highest priority after a reset or mode set operation.

Extended Write (Bit 5)

The extended write option is useful when the INS8257 is accessing a high-speed memory or I/O device whose Ready response is activated by the leading edge of $\overline{\text{MEMW}}$ or $\overline{\text{I/OW}}$. Ordinarily, the late arrival of Ready would cause the INS8257 to insert a

wait state into the DMA cycle, even though the device is capable of completing the transfer without that wait state. This unnecessary wait state can be avoided by use of the extended write option.

When the extended write bit (bit 5) is set, the INS8257 generates $\overline{\text{MEMW}}$ or $\overline{\text{I/OW}}$ earlier in the DMA cycle. This permits the memory or I/O device to issue its Ready response earlier in the cycle, thereby avoiding unnecessary wait states in the INS8257.

TC Stop Bic (Bit 6)

Setting this bit assures that a channel will be disabled as soon as it performs the last DMA cycle in a programmed DMA transfer. When Terminal Count (TC) goes true at the end of a transfer sequence, the channel enable bit of the currently selected channel is automatically reset. This channel remains disabled until its channel enable bit is set again by the program.

Auto Mode (Bit 7)

This mode provides the means for automatically repeating block transfers or for chaining of multiple block transfers, without requiring direct control by the program between blocks. In this mode, the channel 2 and channel 3 registers operate in tandem. The contents of the channel 2 registers are used to control the first DMA operation.

The channel 3 registers temporarily store the parameters required for the next block to be transferred. Upon completion of the first DMA block transfer, the contents of the channel 3 registers are automatically copied into the channel 2 registers and the next block is transferred under channel 2 register control.

NOTE

The TC stop bit does not affect the channel 2 enable bit when in auto load mode.

When the auto load bit is set, writing new parameters into the channel 2 registers automatically loads those same parameters into the channel 3 registers. In this way, all parameters required for a repeat block transfer are loaded in a single channel programming sequence.

If different parameters are required for the second block transfer (for chaining block transfers), channel 3 can be programmed after channel 2.

The channel 3 register contents are copied into the channel 2 registers during an update cycle, which occurs right after the TC output goes true. Each time an update cycle begins, an update flag is set. This flag is available to the program via bit 4 of the status register. Following re-initialization of channel 2, the first DMA cycle of the new data block begins. The update flag is reset when this first DMA cycle is completed.

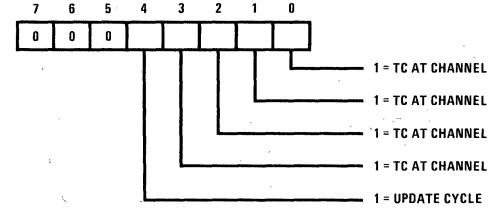
To continue a block chaining sequence, the auto load bit is left in the set state and the channel 3 registers are programmed for the next data block. Before loading new parameters into the channel 3 registers, the update flag should be tested to be certain the channel 2 update operation has been completed.

NOTE

DMA transfers can be performed on channel 3 when the auto load bit is set. However, any parameters loaded into channel 3 registers will be copied into channel 2 registers during the next update cycle.

Reading Status Register

Five status bits are available to the system at one register address.

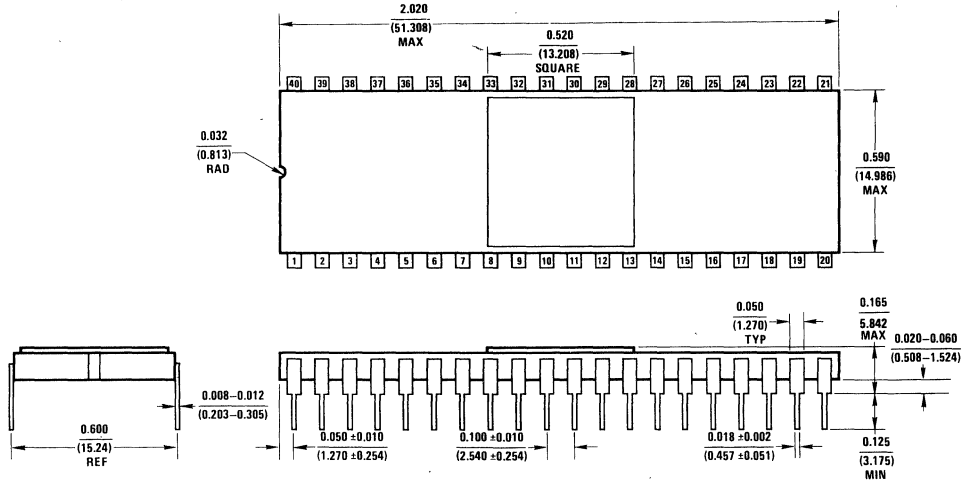


A channel's TC status bit is set when that channel is selected and the TC output is activated. Reading the status register resets all TC bits.

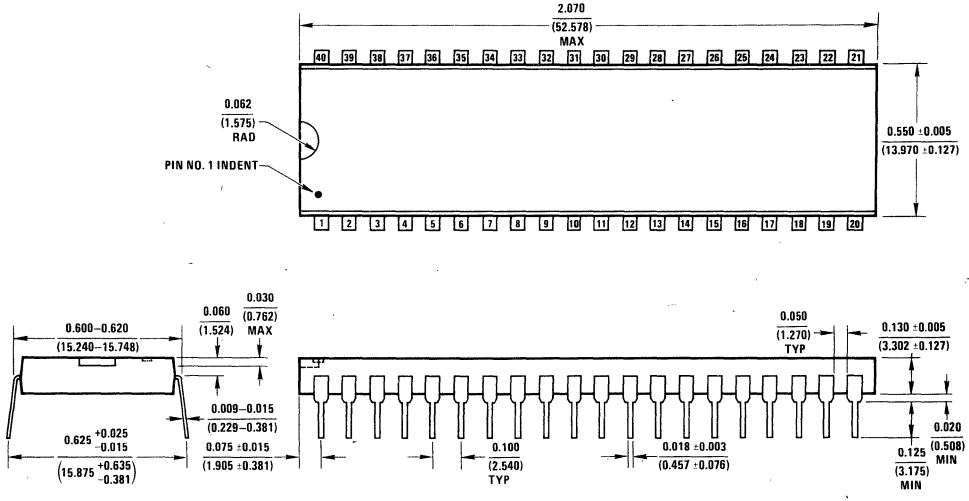
The update flag (bit 4) is set at the start of an update cycle and resets at the end of the update cycle. The update flag is also cleared by resetting the auto load bit and by resetting the INS8257. It is not cleared when the status register is read.

Reading the status register requires a single I/O read operation, with the chip selected by CS and the register selected by system address lines A3-A0.

Physical Dimensions inches (millimeters)



40-Lead Ceramic Dual-In-Line Package (D)
Order Number INS8257D
NS Package Number D40C



40-Lead Plastic Dual-In-Line Package (N)
Order Number INS8257N
NS Package Number N40A

D.3

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