National Semiconductor

Preliminary
JULY 1978

INS8259 Programmable Interrupt Controller

General Description

The INS8259 is a Programmable Interrupt Controller chip contained in a standard 28-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a versatile interrupt management device in a microcomputer system.

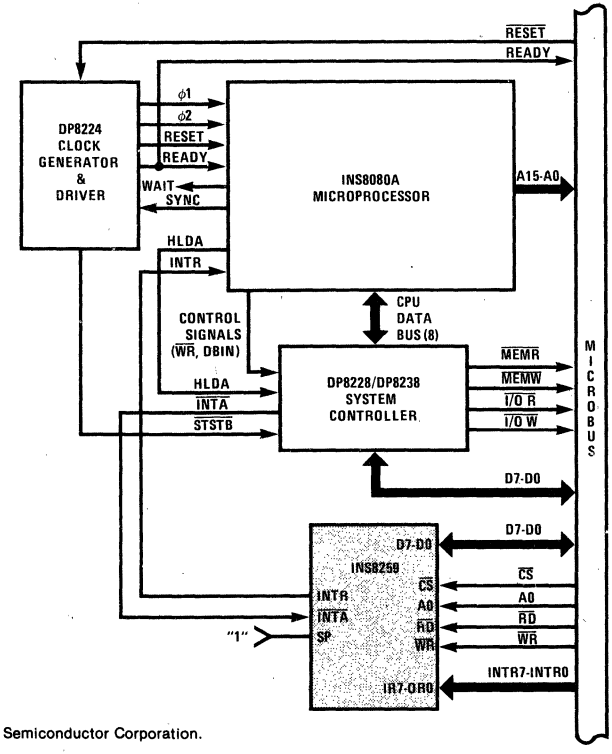
Each INS8259 resolves interrupt requests from up to eight different sources. These devices can be cascaded to provide interrupt management of up to 64 levels with no other circuitry required.

The INS8259 minimizes software and real time overhead when handling multi-level priority interrupts. Its four operating modes allow the device to satisfy diverse system requirements.

Features

- Performs Priority Control of up to Eight Interrupt Levels
- Can be Expanded to Handle up to 64 Levels Through Cascading
- Four Programmable Operating Modes
- Programmable Interrupt Vectors, Allowing Service Routines to be Located Anywhere in Memory
- Interrupt Request Inputs Can be Individually Masked
- TRI-STATE® TTL Drive Capability for Bidirectional Data and Control Buses
- Single +5 Volt Power Supply
- 28-Pin Dual-in-Line Package
- MICROBUS™* Compatible

INS8080 Family CPU Group to MICROBUS Configuration



*A trademark of National Semiconductor Corporation.

Absolute Maximum Ratings

Ambient Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = +5V ± 5%, GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400μA
V_{OH-INT}	Interrupt Output High Voltage	2.4 3.5			V V	I_{OH} = −400μA I_{OH} = −50μA
$I_{IL(IR0-7)}$	Input Leakage Current for IR_{0-7}			−300 10.	μA μA	V_{IN} = 0V V_{IN} = V_{CC}
I_{IL}	Input Leakage Current for Other Inputs			10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage			±10	μA	V_{OUT} = 0.45V to V_{CC}
I_{CC}	V_{CC} Supply Current			100	mA	

Capacitance

T_A = +25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			20	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins to ground

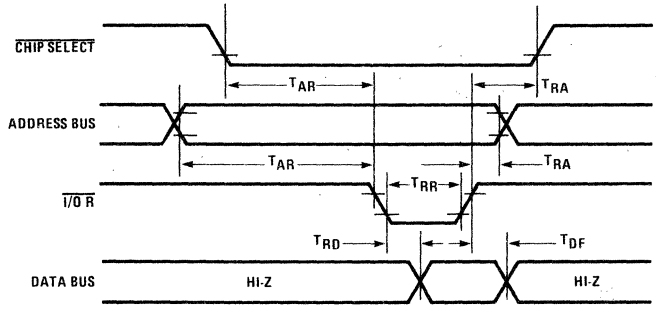
AC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = +5.0V ± 5%, GND = 0V

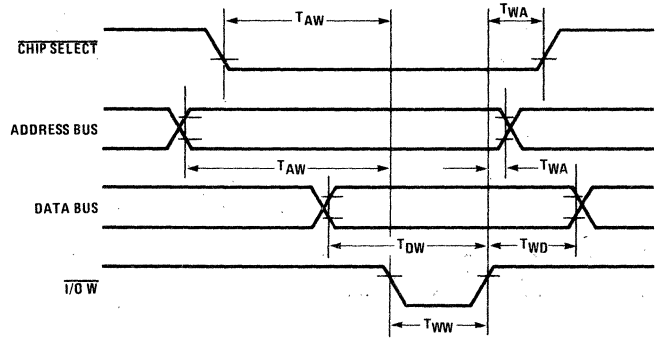
Symbol	Parameter	Min	Max	Unit	Test Conditions
BUS PARAMETERS					
READ					
t_{AR}	$\overline{CS}/A_0$ Stable before $\overline{RD}$ or $\overline{INTA}$	50		ns	
t_{RA}	$\overline{CS}/A_0$ Stable after $\overline{RD}$ or $\overline{INTA}$	5		ns	
t_{RR}	$\overline{RD}$ Pulse Width	420		ns	
t_{RD}	Data Valid from $\overline{RD}/\overline{INTA}$		300	ns	C_L = 100pF
t_{DF}	Data Float after $\overline{RD}/\overline{INTA}$		200		C_L = 100pF
t_{DF}		20		ns	C_L = 20pF
WRITE					
t_{AW}	A_0 Stable before $\overline{WR}$	50		ns	
t_{WA}	A_0 Stable after $\overline{WR}$	20		ns	
t_{WW}	$\overline{WR}$ Pulse Width	400		ns	
t_{DW}	Data Valid to $\overline{WR}$ (T.E.)	300		ns	
t_{WD}	Data Valid after $\overline{WR}$	40		ns	
OTHER TIMINGS					
t_{IW}	Width of Interrupt Request Pulse	100		ns	
t_{INT}	INT ↑ after IR ↑	400		ns	
t_{IC}	Cascade Line Stable after $\overline{INTA}$ ↑	400		ns	

Timing Waveforms

Read Timing



Write Timing



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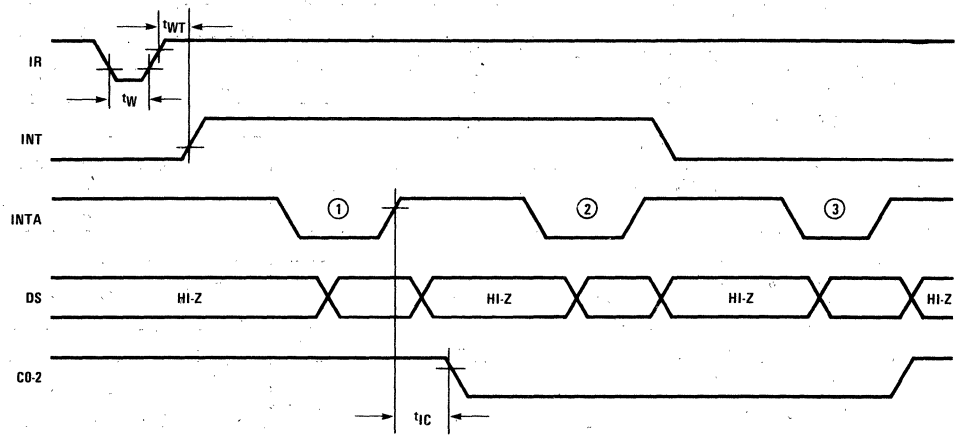
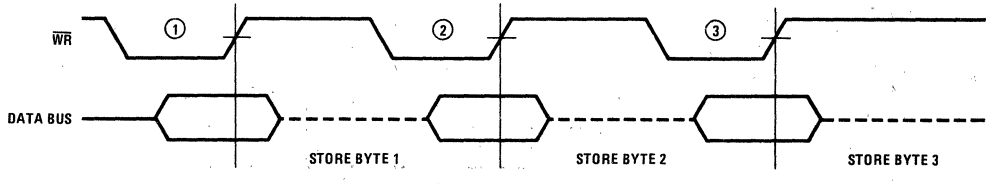
Timing Waveforms (cont'd.)

Other Timing

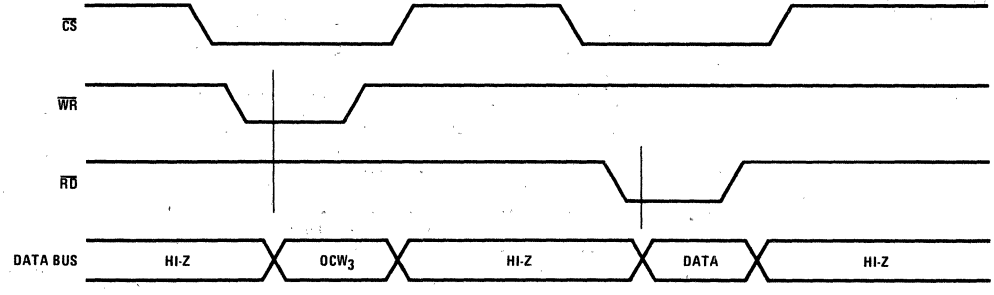


NOTE: INTERRUPT REQUEST MUST REMAIN "HIGH" (AT LEAST) UNTIL LEADING EDGE OF FIRST $\overline{INTA}$.

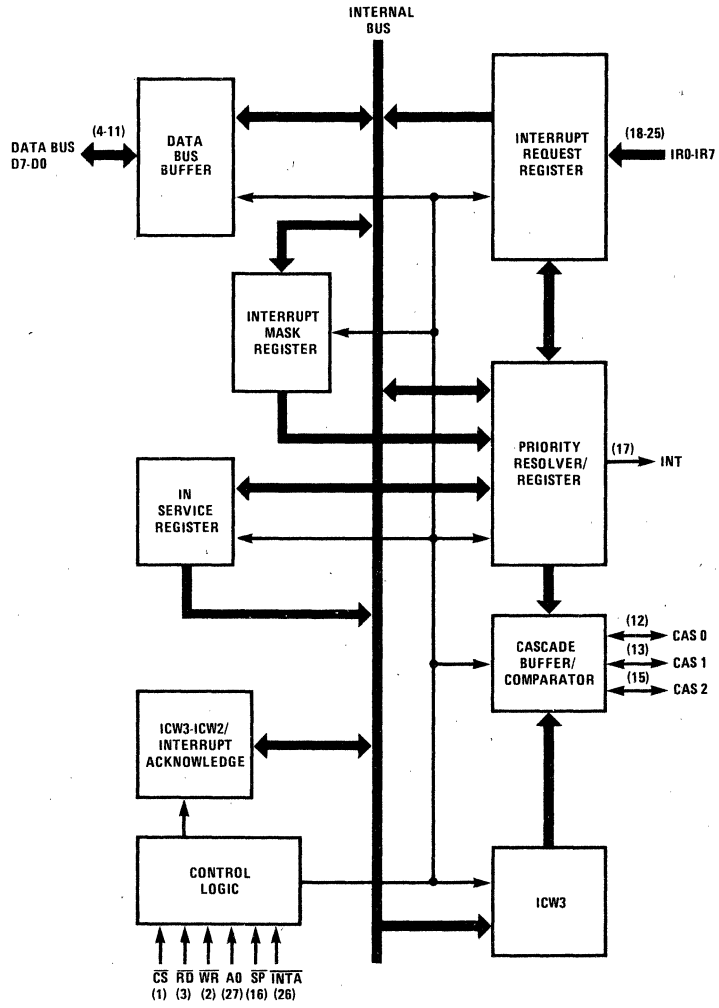
Initialization Sequence



Read Status/Poll Mode



INS8259 Block Diagram



INS8259 Functional Pin Description

The following describes the functions of all INS8259 input/output pins. Some of these descriptions refer to internal circuits.

INPUT SIGNALS

Chip Select ($\overline{CS}$): When low, the device is selected, enabling communication between the INS8259 and the microprocessor.

Read ($\overline{RD}$): When low, allows the microprocessor to read contents of Interrupt Request Register (IRR), In Service Register (ISR) or Interrupt Mask Register (IMR) or the BCD value of the current interrupt level.

Write ($\overline{WR}$): When low, allows the microprocessor to write control words (ICWs and OCWs) to the INS8259.

A0: This input is used in conjunction with the $\overline{WR}$ signal to write command words into specific command registers and with the $\overline{RD}$ signal to read specific status registers. A0 can be controlled via one of the microprocessor address lines.

Interrupt Acknowledge ($\overline{INTA}$): This input is generally provided by the CPU group's System Controller element (e.g., INS8228). Each INT is acknowledged by a sequence of three $\overline{INTA}$ pulses, which causes the INS8259 to output a three-byte CALL instruction onto the Data Bus.

Interrupt Request (IR7-IR0): These eight inputs are used by external circuits to request servicing by the CPU. A low-to-high transition on one of these lines represents a new interrupt request from the circuit controlling that line. Each positive transition on the IR lines causes the INS8259 to issue a separate interrupt to the microprocessor. The IR line must remain high through the first $\overline{INTA}$ pulse or the INT line will go low. Concurrent interrupt requests are resolved according to their relative positions in the priority scheme. Typically, an active (high) IR input is reset by the interrupt service routine associated with that line.

Slave Program ($\overline{SP}$): This control input is used in systems having cascaded INS8259s, where one INS8259 operates as the master and all others operate as slaves. A high level at the $\overline{SP}$ input appoints that INS8259 as master, while a low level assigns the role of slave.

OUTPUT SIGNALS

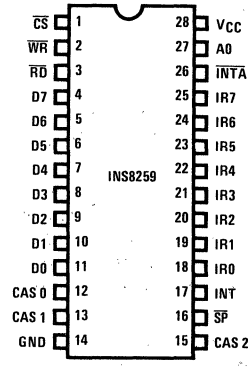
Interrupt (INT): This output is applied to the microprocessor's interrupt input (e.g., pin 14 of INS8080A).

INPUT/OUTPUT SIGNALS

Data (D7-D0) Bus: This bus, which comprises eight TRI-STATE input/output lines, provides bidirectional communication between the INS8259 and the CPU. Command words, status words and CALL instructions are transferred over these lines.

Cascade (CAS2-CAS0): These three lines are used in systems having cascaded INS8259s. The master INS8259 outputs the three-bit ID of a slave device on CAS2-CAS0 in order to select that slave for interrupt servicing.

Pin Configuration



INS8259 Programming Information

Two types of command words are used to program the INS8259. These are:

- Initialization Command Words (ICWs) — A sequence of two or three ICWs is required to prepare the INS8259 for operation. Two words are used if a single INS8259 is being initialized. A three-word sequence is used if a master/slave configuration is being initialized. See figure 1 for an illustration of this sequence. Each ICW is timed by a separate WR pulse.
- Operation Command Words (OCWs) — These command words are used to specify various operating characteristics of the INS8259 and to read the status of certain registers.

Figure 1 summarizes the bus controls needed to output command words to the INS8259 and to read INS8259 status.

A0	D4	D3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Operation
READ						
0			0	1	0	(Note 1) IRR, ISR or Interrupt Level to Data Bus
1			0	1	0	IMR to Data Bus
WRITE						
0	1	X	1	0	0	Data Bus to ICW1
0	0	0	1	0	0	Data Bus to OCW2
0	0	1	1	0	0	Data Bus to OCW3
1	X	X	1	0	0	(Note 2) Data Bus to OCW1, ICW2, ICW3
DISABLE						
X	X	X	1	1	0	Data Bus to Hi-Z
X	X	X	X	X	1	Data Bus to Hi-Z

Notes:

1. Selection of IRR, ISR or Interrupting Level controlled by OCW3 written prior to the Read operation.
2. Proper sequence set by on-chip sequencer.

Figure 1. Basic Control for INS8259 I/O Operations

INITIALIZATION COMMAND WORDS (ICWs)

Figure 2 summarizes the command format for ICW1, ICW2 and ICW3. There are two variations of the ICW3 format, one for the master device and one for the slaves.

Figure 3 describes the INS8259 initialization sequence.

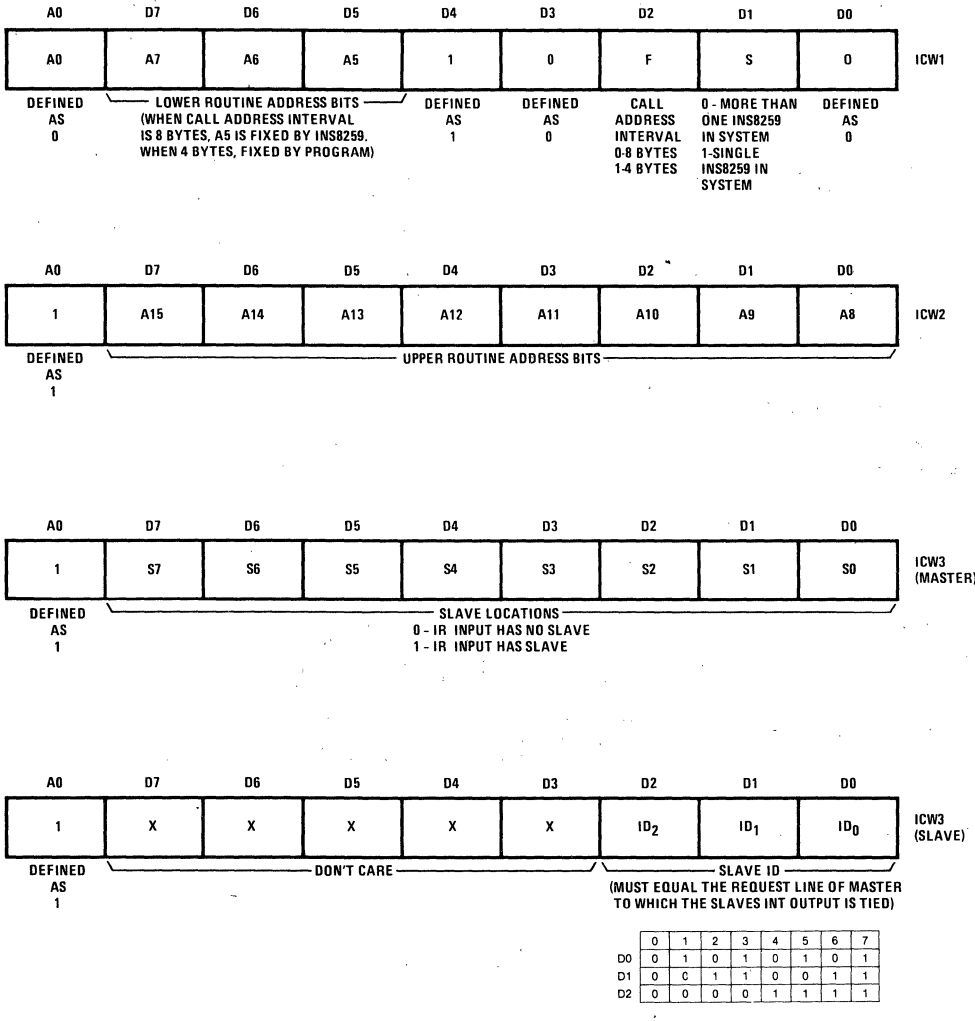


Figure 2. Initialization Command Word Format

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When an ICW1 is received, the following functions are performed in the INS8259.

- The edge sense circuit is reset, which prepares it to detect a positive transition at an IR input.
- The Interrupt Mask Register (IMR) is cleared.
- The IR7 input is assigned lowest priority (i.e., priority level 7).
- The special mask mode and status read flip-flops are reset. ICW1 also contains three types of programming information.
  - — Single INS8259 or Master with Slave(s) configuration, as set by D1 of ICW1.
  - — Four- or eight-byte CALL address interval, as set by D2 of ICW1.
  - — If the four-byte CALL interval is used, bits A5-A7 of the CALL address are specified by D5-D7 of ICW1 and bits A0-A4 are provided by the INS8259. If the eight-byte interval is used, bits A6 and A7 are specified by bits D6 and D7 of ICW1, while bits A0-A5 are provided by the INS8259. Refer to table 1.

The contents of ICW2 specify bits A8-A15 of the CALL address.

ICW3 is used only if a master/slave configuration is being initialized. The ICW3 issued to the master INS8259 identifies which IR inputs have slaves attached. Each bit position corresponds to a separate IR input (D0 = IR0 and D7 = IR7). For each IR input that has a slave attached, the corresponding ICW3 bit is set to 1. Those IR positions without a slave are identified by 0s in the corresponding ICW3 bit positions. The ICW3 is also used to assign three-bit identifiers to the slave INS8259s. A separate ICW3 is sent to each slave with a unique ID contained in bits D0-D2. The ID must correspond to which master IR line the slave's INT is connected to. Later, when a slave's interrupt request is selected for servicing, the master INS8259 automatically issues byte 1 of the CALL sequence and sets the ID assigned to that slave on the CAS2-CAS0 lines. This enables the specified slave to release bytes 2 and 3 of the CALL sequence.

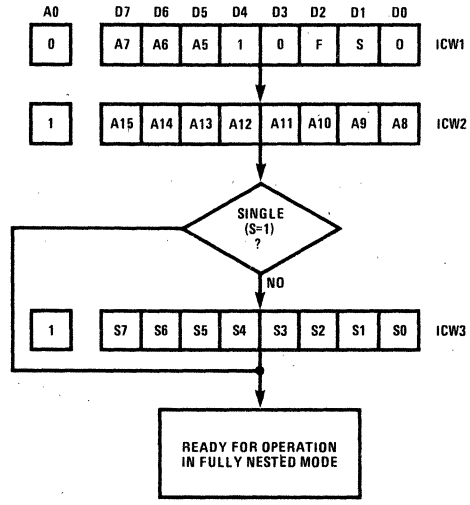

Figure 3. Initialization Sequence

Table 1.

	Interval = 4								Interval = 8							
	Lower Memory Routine Address															
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
IR7	A7	A6	A5	1	1	1	0	0	A7	A6	1	1	1	0	0	0
IR6	A7	A6	A5	1	1	0	0	0	A7	A6	1	1	0	0	0	0
IR5	A7	A6	A5	1	0	1	0	0	A7	A6	1	0	1	0	0	0
IR4	A7	A6	A5	1	0	0	0	0	A7	A6	1	0	0	0	0	0
IR3	A7	A6	A5	0	1	1	0	0	A7	A6	0	1	1	0	0	0
IR2	A7	A6	A5	0	1	0	0	0	A7	A6	0	1	0	0	0	0
IR1	A7	A6	A5	0	0	1	0	0	A7	A6	0	0	1	0	0	0
IR0	A7	A6	A5	0	0	0	0	0	A7	A6	0	0	0	0	0	0

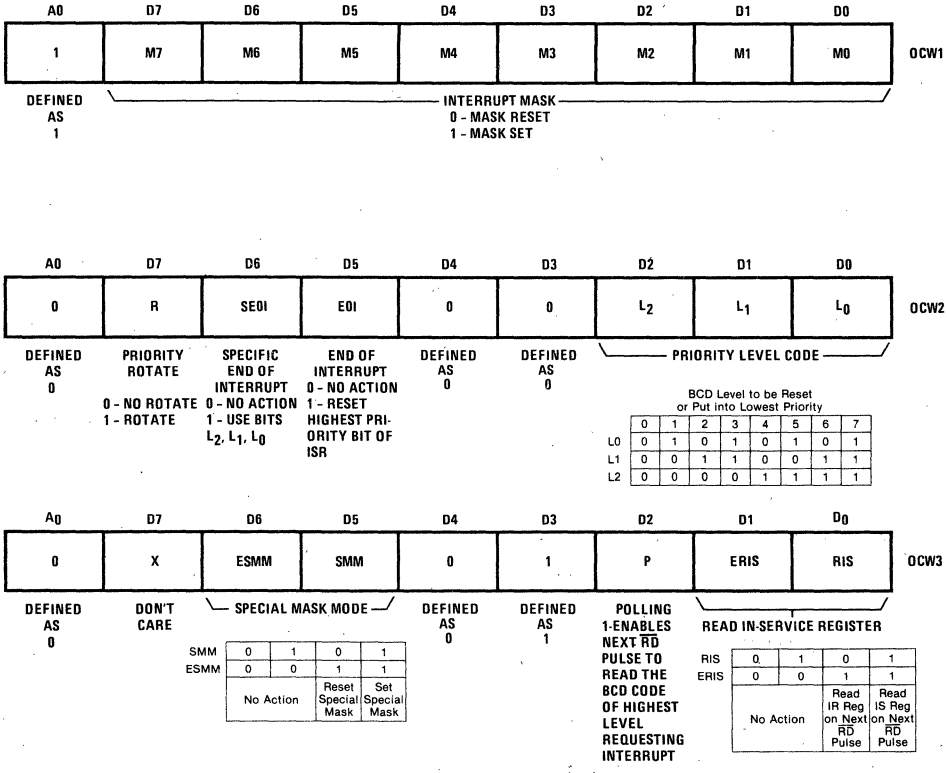

Figure 4. Operation Command Word Format

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OPERATION COMMAND WORDS (OCWs)

Figure 4 summarizes the bit functions for OCW1, OCW2 and OCW3. These command words can be issued to the INS8259 at any time after initialization to alter the device's operating mode or to read specified registers.

FULLY NESTED MODE

Immediately following the ICW sequence, the INS8259 is ready to operate in the fully nested mode, with the highest priority assigned to IR0 and the lowest priority to IR7. In this mode, processing of lower priority interrupts is nested within higher priority interrupts. That is, a new interrupt will be sent to the microprocessor whenever an interrupt request is received, if no higher priority interrupt is in service. If any lower priority interrupt is in service at this time, execution of its routine is suspended until all higher level interrupts are serviced. When the microprocessor acknowledges the new interrupt, its CALL address is released. No interrupt will be issued for an interrupt request so long as a higher level interrupt is in service.

As part of the completion of an interrupt service routine, the microprocessor must issue an End of Interrupt (EOI) command, which resets the highest level ISR bit. After an ISR bit resets, the ISR or IRR bit then having the highest priority is serviced. The EOI is issued by means of an OCW2, in which bit D5 = 1. To maintain the operating characteristics of the fully nested mode, bit D7 must equal 0.

ROTATING PRIORITY MODE

In the rotating priority mode, an interrupt level is automatically assigned lowest priority immediately after it is serviced. Highest priority then passes to the next lower interrupt level. For example, when servicing of interrupt level 3 is completed (ISR bit 3 is reset), interrupt level 3 is assigned lowest priority and interrupt level 4 assumes highest priority.

To operate in rotating priority mode, the EOI issued at the end of *each* service routine must have bit 7 and bit 5 set to 1.

The lowest priority can be program-assigned by means of an OCW2. The OCW2 used to make a specific priority assignment would need to be in the range (hex) C0-C7. For example, if the OCW2 value is C3, interrupt level 3 is assigned lowest priority and level 4 is given highest priority.

INTERRUPT MASKING AND SPECIAL MASKING

OCW1 can be used to mask off individual interrupt levels. This command is specified by A0 = 1. Each data bit in OCW1 controls a separate bit in the Interrupt Mask Register (IMR). When an IMR bit is set, the corresponding bit position is masked at the IRR and, when in special mask mode, at the ISR.

If an ISR bit is already set at the time it is masked, the lower priority interrupts will remain inhibited by the masked interrupt level. These lower priority levels can be enabled by an EOI command that resets that ISR bit or by issuing a special mask command.

The special mask command is issued by means of an OCW3, in which bit D5 = 1 and D6 = 1. This sets the special mask mode flip-flop, which enables all unmasked interrupt levels. These remain enabled until the special mask mode flip-flop is reset by an OCW3 with bit D5 = 0 and bit D6 = 1.

POLLED MODE

The polled mode is used when the program assumes full control of device servicing and does not allow processor interrupts.

In this mode, the microprocessor disables its interrupt input and, when it wishes to service a device attached to the INS8259, it issues an OCW3 with bit D2 = 1. This is followed by an $\overline{RD}$ pulse with A0 = 0. If any IRR bits are set when the $\overline{RD}$ pulse is received, the INS8259 sets the ISR bit corresponding to the highest priority level requesting service. It also identifies that priority level on the data bus in the following manner:

D7	D6	D5	D4	D3	D2	D1	D0
I	–	–	–	–	W2	W1	W0

W0-2 — BCD code of the highest priority level requesting service.

I — Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels — so that the $\overline{INTA}$ sequence is not needed (and this saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

END OF INTERRUPT (EOI) AND SPECIFIC END OF INTERRUPT (SEOI)

The EOI command is used in the fully nested mode to reset the appropriate ISR bit when that interrupt level's service routine is concluding. The non-specific EOI command always resets the highest level ISR bit that is currently set. For this reason, it is reliable only in a fixed priority scheme, such as the fully nested mode. When priority assignments are changed from the standard order (i.e., IR7 = lowest), the specific EOI command must be used. This command contains the BCD value of the interrupt level that is to be reset.

Both specific and non-specific EOI are issued by means of an OCW2. For the non-specific EOI version, bit D5 of the command is set to 1 and bit D6 is 0. For the specific EOI version, bit D5 of the command is set to 1 and bit D6 is set to 1. In the specific EOI command, the BCD value of the ISR bit to be reset is contained in command bits D0-D2.

READING INS8259 REGISTERS

Four types of status can be read from the INS8259: the contents of IRR, the contents of ISR, the contents of IMR and the BCD value of the interrupt level requesting service.

The microprocessor reads the contents of IRR by issuing an OCW3, in which bit D0 = 0 and bit D1 = 1. This is followed by a $\overline{RD}$ pulse, during which the INS8259 places the IRR status on the data bus with the IRR low order bit (0) present on D0 and the IRR high order bit (7) present on D7. The contents of ISR are read in the same manner, except that OCW3 bit D0 is set to 1 as well as bit D1. The contents of IMR can be read by setting A0 = 1 and issuing a $\overline{RD}$ pulse.

The BCD value of the interrupt level requesting service is placed on the data bus in response to a poll command. This technique was described earlier under Polled Mode.

CASCADE OPERATION

A typical cascading system is shown in figure 5.

Once a slave line is activated and later acknowledged, the INS8080 CALL code is released by the master during the first $\overline{INTA}$ pulse. The CAS lines will contain the slave address code from the trailing edge of this pulse until the trailing edge of the third $\overline{INTA}$ pulse. This allows the corresponding slave to release the two-byte service routine address during the second and third $\overline{INTA}$ pulses.

Because the CAS lines default to 000, no slave should be connected to IR0 on the master unless master request inputs IR1 through IR7 are connected to slaves.

Each INS8259 in the system must follow its own initialization sequence and can be programmed to operate in any mode. Two EOI commands must be issued: one for the master and one for the slave.

The EOI allows the respective request input to generate a new interrupt. To allow a slave to have nested interrupts, the master should be sent an EOI as soon as possible in the service routine.

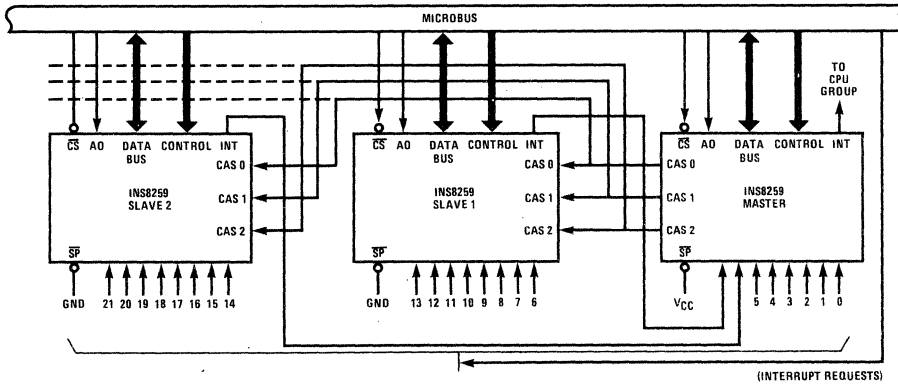


Figure 5. Cascade Operation

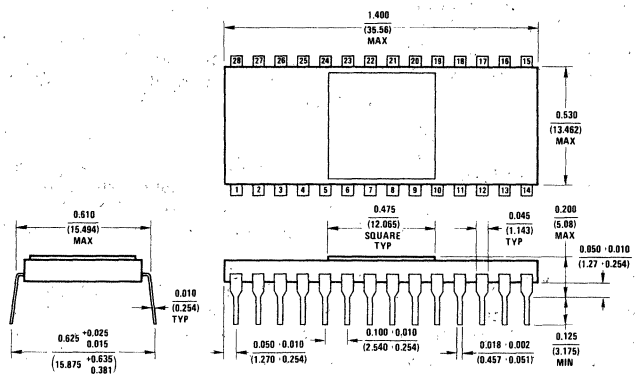
	Instruction	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description
1	ICW1 A	0	A7	A6	A5	1	0	1	1	0	Byte 1 initialization, format = 4, single.
2	ICW1 B	0	A7	A6	A5	1	0	1	0	0	Byte 1 initialization, format = 4, not single.
3	ICW1 C	0	A7	A6	A5	1	0	0	1	0	Byte 1 initialization, format = 8, single.
4	ICW1 D	0	A7	A6	A5	1	0	0	0	0	Byte 1 initialization, format = 8, not single.
5	ICW2	1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization (Address no. 2).
6	ICW3 M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization — master.
7	ICW3 S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization — slave.
8	OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask reg, read mask reg.
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non-specific EOI.
10	OCW2 SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI, L2, L1, L0 code of ISFF to be reset.
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI (Auto Mode).
12	OCW2 RSE	0	1	1	1	0	0	L2	L1	L0	Rotate at EOI (Specific Mode), L2, L1, L0, code of line to be reset and selected as bottom priority.
13	OCW2 RS	0	1	1	0	0	0	L2	L1	L0	L2, L1, L0 code of bottom priority line.
14	OCW3 P	0	—	0	0	0	1	1	0	0	Poll mode.
15	OCW3 RIS	0	—	0	0	0	1	0	1	1	Read IS register.
16	OCW3 RR	0	—	0	0	0	1	0	1	0	Read requests register.
17	OCW3 SM	0	—	1	1	0	1	0	0	0	Set special mask mode.
18	OCW3 RSM	0	—	1	0	0	1	0	0	0	Reset special mask mode.

Notes:
1. In the master mode $\overline{SP}$ pin = 1; in slave mode $\overline{SP}$ = 0.
2. (—) = don't care.

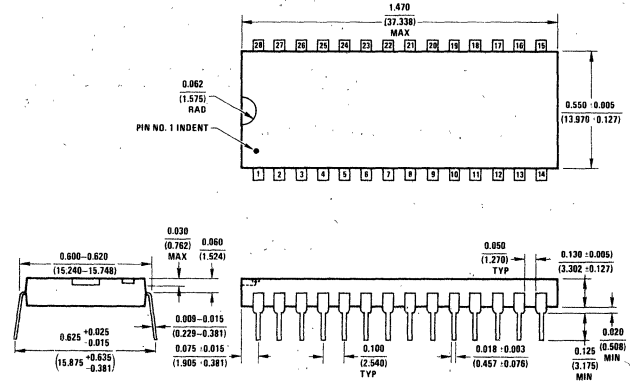
Figure 6. INS8259 Instruction Set

Physical Dimensions

inches (millimeters)



28-Lead Ceramic Dual-In-Line Package (D)
Order Number INS8259D
NS Package Number D28A



28-Lead Plastic Dual-In-Line Package (N)
Order Number INS8259N
NS Package Number N28A

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