HomePlug® AV
200Mbps PHY

TECHNICAL REFERENCE MANUAL

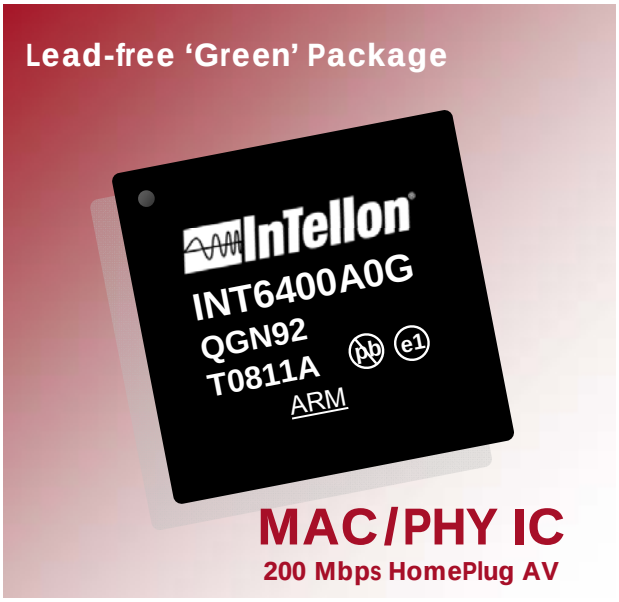
INT6400

InTellon® NO NEW WIRES.

HomePlug® AV MAC/PHY Transceiver

Features

- HomePlug® AV MAC, PHY and AFE in a 196-contact LBGA, Pb-Free package
- MII (Host & PHY) interface
- Co-existence with HomePlug® 1.0 Nodes
- HomePlug® AV PHY: 200 Mbps OFDM@1024-QAM
- Supports1024/256/64/16/8-QAM, QPSK, BPSK and ROBO Modulation Schemes
- 128-bit AES Link Encryption with key management for secure powerline communications
- Windowed OFDM with noise mitigation based on patented line synchronization techniques improves data integrity in noisy conditions
- Dynamic channel adaptation and channel estimation maximizes throughput in harsh channel conditions
- Advanced Turbo Code Forward Error Correction (*France Telecom – TDF – Groupe des Écoles des Télécommunications Turbo codes patents license)*
- HomePlug® AV MAC: TDMA and priority-based CSMA/CA channel access schemes maximize efficiency and throughput
- Integrated Quality of Service (QoS) Enhancements: contention-free access, four-level priority based contention access, and multi segment bursting
- ToS, CoS and IP Port Number Packet Classifiers
- Supports IGMP managed multicast sessions
- Green Standard (ROHS) Compliant
- Low Power Design



Applications

- High Definition (HD) and Standard Definition (SD) video distribution
- Internet Protocol Television (IPTV) Distribution
- Backbone for Wi-Fi, UWB and Wireless USB
- Higher data rate broadband sharing
- Shared broadband internet access
- Audio and video streaming and file transfer
- Voice over Internet Protocol (VoIP)
- PC files and applications sharing
- Printer and peripheral sharing
- Network and online gaming
- Security cameras

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FIGURES

1. INT6400 HomePlug AV Transceiver Overview

1.1. INT6400 Overview

The INT6400 Medium Access Controller (MAC)/Physical layer (PHY) HomePlug AV transceiver is optimized for multi-media streaming applications. It is fully compliant with the HomePlug AV standard, which is tailored to reliably deliver up to 200 Mbps PHY rate over powerline. It includes a complete HomePlug-AV MAC and PHY, an Ethernet MII (media independent interface), an external SDRAM (synchronous dynamic random access memory) interface, and an interface for 2 external SPI (serial peripheral interface) devices. In addition, the INT6400 includes the A/D (analog to digital) and D/A (digital to analog) converters required for analog interface to the communications medium.

The INT6400 is shown in Figure 1 in its simplest implementation. A standard 10/100 MII Ethernet PHY is connected to the INT6400's MII pins to complete the Ethernet interface, and the Intellon INT1400 line-driver plus some discrete components complete the interface to the powerline. In addition, a single 16-bit external SDRAM is needed for code and packet storage, and an external SPI flash can optionally be used to provide the initial code for booting the processor.

The INT6400 and the INT1400 comprise a matched chip set.

Within the INT6400, the HomePlug-AV MAC function is carried out by firmware running on an embedded ARM926EJ-S CPU (central processing unit), supported by DMA (direct memory access) hardware, two dedicated CRC (cyclic redundancy check) engines, and a large off-chip SDRAM data-store. The HomePlug-AV MAC firmware running on the CPU oversees operation of the integrated HomePlug-AV PHY via an interface that carries control/status information as well as transmits and receives data packets. General-purpose I/O pins are available to drive LEDs (light emitting diodes) directly to indicate link status, as well as to indicate user reset or network-attach events. An on-board PLL (phase locked loop) and built-in crystal oscillator driver permit generation of system clocks from a single external 37.5 MHz crystal.

The HomePlug AV MAC utilizes a mix of Contention Free Period (CFP) accesses with Time Division Multiple Access (TDMA) transmissions and priority based Contention Period (CP) accesses with Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA) transmissions. Reliable delivery of packets is ensured through the use of Selective Acknowledgement (SACK) and Automatic Repeat reQuest (ARQ).

Periodic CFP allocations provide guaranteed QoS (quality of service) for loss sensitive applications such as high-definition (HD) and standard-definition (SD) video. HomePlug AV products provide quasi-error free delivery of TDMA streams while maintaining tight control of latency and jitter. CFP allocations adapt with changing channel conditions and traffic profiles to ensure applications maintain the required QoS. TDMA transmissions during the CFP increase the MAC efficiency by eliminating collisions. CSMA/CA during the CP facilitates delivery of asynchronous traffic by avoiding collisions and by providing priority resolution for differentiated services. The HomePlug AV standard defines the normative mapping of the eight 802.1p access priority levels. These features are essential to provide efficient end-to-end delivery of broadcast quality HD and SD video streams over the harsh power-line environment.

The HomePlug AV PHY combats impairments including deep attenuation notches, noise sources, and multi-path fading by using windowed OFDM, *Turbo Convolutional Codes, precise channel adaptation, and noise mitigation based on AC line cycle synchronization.

(** France Telecom – TDF – Groupe des Écoles des Télécommunications Turbo codes patents license)*

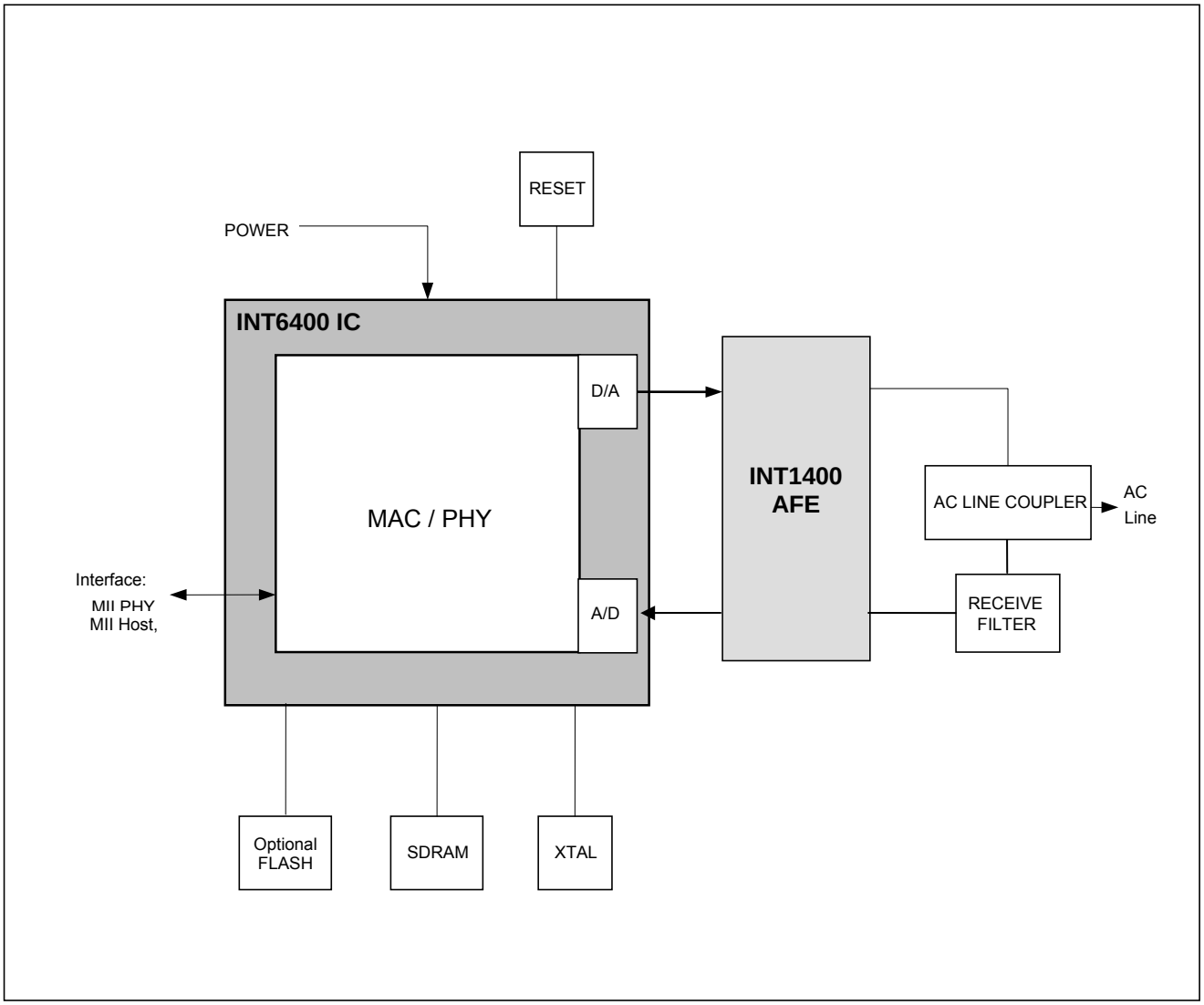


Figure 1: INT6400 Powerline Station

1.2. INT6400 Specification Summary

1.2.1. Physical

Parameter	Value	Description
Package Type	LBGA-196, Pb-Free	196 contact Low Profile Ball Grid Array, 15 X 15 array, 1mm ball pitch
Dimensions	15 mm X 15 mm	Chip package dimensions
Moisture Sensitive Level (MSL)	3	JEDEC standard level 3
Ball Composition	96.5Sn/3.0Ag/0.5Cu	Tin/Silver/Copper
Height	1.4 mm	Maximum height above seating plane
Operating Temp. Range (T_A)	0°C to 70°C	Safe package operating temperature range

1.2.2. Interfaces

Type	Description
MII (Ethernet)	Host or PHY, IEEE 802.3u Media Independent Interface
SPI	Serial Peripheral Interface to read/write INT6400 configuration and firmware image stored in external flash memory
SDRAM	SDRAM memory controller operates at 75 MHz, 100 MHz, 112.5 MHz or 150 MHz with 16-bit data bus

1.2.3. Technologies

Type	Description
Windowed OFDM	Windowed Orthogonal Frequency Division Multiplexing – provides over 1,000 narrow-band carriers each of which can be independently turned off (30-dB notch) or modulated up to 1024 QAM for optimal performance
TDMA Channel Access	Time Division Multiple Access – a means of accommodating more than one service on the channel by assigning time slots – useful for ensuring Quality of Service (QoS) for video streams
CSMA/CA Channel Access	Carrier-Sense Multiple Access/Collision Avoidance – a means of sensing the presence of a carrier before transmission is attempted to avoid network collisions or contention

1.2.4. Performance

Parameter	Value	Description
Maximum PHY Rate	200 Mbps	Maximum PHY rate including payload and overhead
Modulation	1024/256/64/16/8 QAM, QPSK, BPSK, ROBO	Each OFDM sub carrier can be independently modulated to optimize throughput for operating conditions
Encryption	128 bit AES	Matches industry standard Advanced Encryption System

1.2.5. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCORE	INT6400 Core Supply Voltage	1.00	1.05	1.10	V
VPLL_1	PLL Analog Power	1.00	1.05	1.10	V
VDDIO	INT6400 I/O Supply Voltage	3.13	3.30	3.47	V
VDDA_1	Analog Power 1V	1.00	1.05	1.10	V
VDDA_3	Analog Power 3V	3.13	3.30	3.47	V
VPLL_3	INT6400 Analog PLL Voltage	3.13	3.30	3.47	V
T_A	Ambient Operating Temperature	0		70	°C

Power supply voltages may be applied in any sequence during power up and removed in any order during power down.

1.2.6. Absolute Maximum Ratings

Operation at or above the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to these conditions for extended periods of time may affect long-term device reliability. Correct functional behavior is not implied or guaranteed when operating at or above the Absolute Maximum Ratings.	Symbol	Parameter	Min	Max	Units
	VCORE	Core Supply Voltage	-0.3	1.20	V
	VPLL_1	PLL Analog Power	-0.3	1.20	V
	VDDIO	I/O Supply Voltage	-0.3	3.63	V
	VPLL_3	Analog PLL Supply Voltage	-0.3	3.63	V
	VDDA_1	Analog Power 1V	-0.3	1.20	V
	VDDA_3	Analog Power 3V	-0.3	3.63	V
	T_{STORE}	Storage Temperature	-40	125	°C
	ESD Immunity	Human Body Model		TBD	V
		Machine Model		TBD	V
		Charged Device Model		TBD	V

1.2.7. INT6400 Power Supply Requirements

Table 1: INT6400 Typical Power Supply Requirements

Power Supply	Supply Voltage (V)	Transmit Mode Current (mA)	Receive Mode Current (mA)
VCORE	1.05	350	530
VDDIO	3.3	30	30
VDDA_3	3.3	90	77
VDDA_1	1.05	40	60
VPLL_3	3.3	3	3
VPLL_1	1.05	2	2

Table 2: INT6400 Typical Total IC Power

Device	Transmit Mode Power (mW)	Receive Mode Power (mW)
INT6400	818	985

1.2.8. DC Switching Thresholds

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Low-level input voltage			0.8	V
V_{IH}	High-level input voltage		2.0		V
V_{OL}	Low-level output voltage	I_{OL}= 4 mA, 12mA[1]		0.4	V
V_{OH}	High-level output voltage	I_{OH}=-4mA, -12mA[2]	2.4		V
I_{IL}	Low-level input current	V_I = Gnd	-1		µA
I_{IH}	High-level input current	V_I = Vdd		1	µA
I_{OZ}	High-impedance output current	Gnd ≤ V_I ≥ Vdd	-1	+1	µA

1. I_{OL} = 12 mA for all GPIOs.
   I_{OL} = 4 mA for all other interfaces except PCI and CardBus. Refer to PCI 2.2 for PCI I_{OL} specifications.
2. I_{OH} = -12 mA for all GPIOs.
   I_{OH} = -4 mA for all other interfaces except PCI and CardBus. Refer to PCI 2.2 for PCI I_{OH} specifications.
3. There is no need to connect unused GPIO pins because they have internal pull-up or pull down resistors. See Section 6.2.

1.3. INT6400 Architecture

1.3.1. MAC Hardware

The MAC hardware within the INT6400 provides a platform on which the MAC software can be run. The basis of the MAC hardware is an ARM926EJ-S 32-bit processor. This processor contains 16kb of data cache and 16kb of instruction cache, and is coupled to 128k of local instruction memory and 96k of local data memory. Since the entire MAC software cannot fit within this memory, an off-chip SDRAM interface is used to provide additional instruction and data storage; the effective use of the instruction and data cache reduces the impact of using this relatively slow off-chip storage.

In addition to the processor, the MAC also contains numerous peripherals that are essential for running an advanced Real-Time Operating System (RTOS). The MAC contains a reset/clock controller, numerous timers, a vector interrupt controller, a synchronous and an asynchronous UART (universal asynchronous receiver transmitter), GPIO (general purpose input output) support, and a complex self-diagnostic module. These peripherals allow the RTOS and MAC software to respond to system interrupts, and control the operation of the software.

Numerous on-chip busses allow unimpeded access to critical system resources – most notably, the SDRAM interface and the small on-chip SRAM (Static Random Access Memory). The on-chip SRAM is used for storing time-critical descriptor chains, while the off-chip SDRAM is used for storing the majority of the descriptor information, as well as the packet data. The descriptor engine is responsible for moving data to and from memory (either on-chip SRAM or off-chip SDRAM), for merging packets together, and for providing status and interrupt information back to the processor. A key factor here is to reduce the number of interrupts that the processor must respond to – with the high data rates that are achievable through the HomePlug-AV PHY, it is essential that a large proportion of the DMA processing is off-loaded to these descriptor engines.

In addition to the Ethernet interface, the descriptor engines are also used within the two ICV modules. The two ICV (Integrity Check Value) modules are used to read and compute a 32-bit CRC on a block or blocks of memory. Both of these are used within the HomePlug-AV MAC software to help off-load the processor.

Figure 2 shows a diagram of the MAC hardware and the various host interfaces that connect to it.

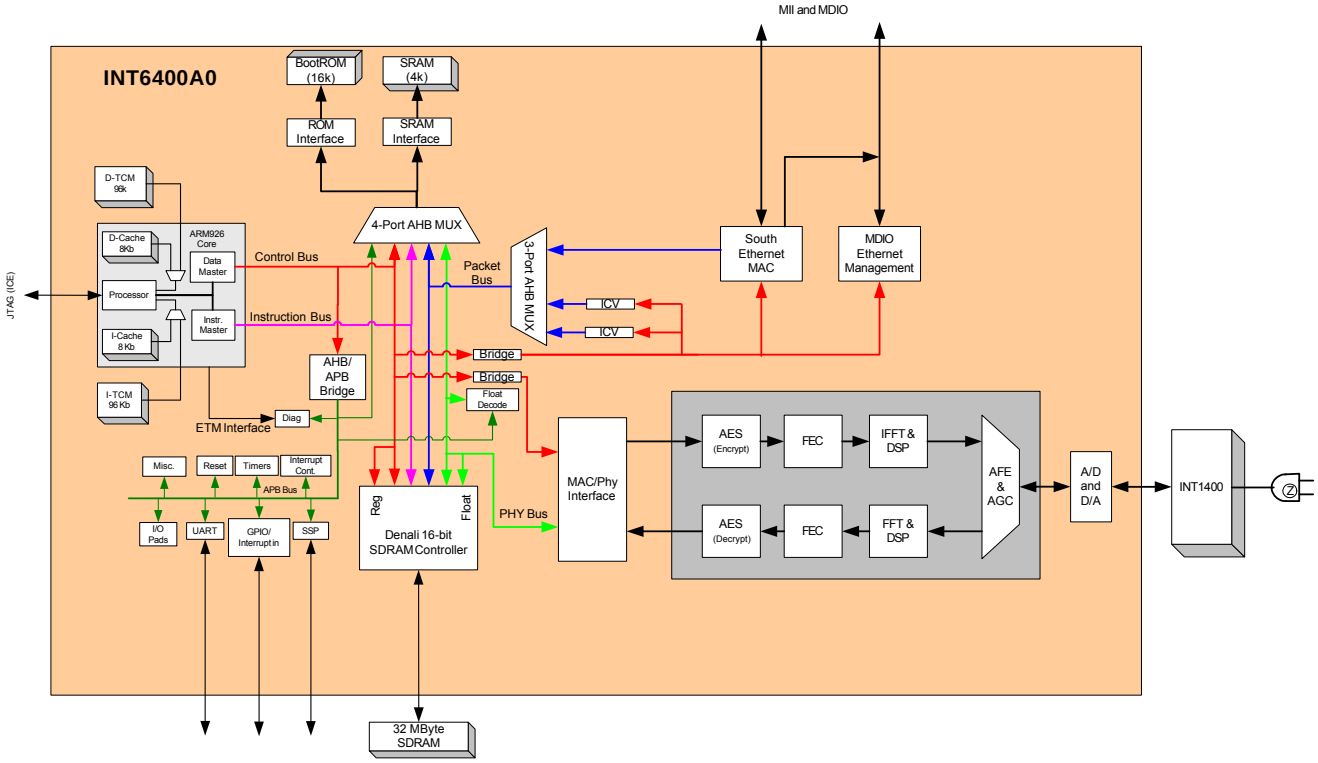


Figure 2: MAC and PHY Hardware

2. INT6400 Interfaces

2.1. Media Independent Interface

The Media Independent Interface (MII) is configured as either an Ethernet Medium Access Controller (MAC) or a Physical Medium Dependent (PMD or PHY) controller. Medium Independent Interface (MII) is an industry standard, multi-vendor interface between the MAC and PHY sub-layers. It provides a simple connection between Ethernet PHY controllers and IEEE802.3 Ethernet MACs from a variety of sources. MII consists of separate 4-bit data paths for transmit and receive data along with carrier sense and collision detection. The MII interface has a two-wire bi-directional serial Management Data Interface (MDI). This interface provides access to the status and control registers in the Ethernet PHY logic. The MII and MDI pins are shared between the MAC and PHY interfaces. Further details of the MII are available from the IEEE 802.3u Standard.

Configuration straps described in Section 6.2.2 set the MII operation to a MAC or PHY controller. The MAC and PHY configurations support 10 Mbps or 100 Mbps in half-duplex or full-duplex modes and flow control for half-duplex and full-duplex connections. The MII (Ethernet) interface includes the management data interface for both MAC and PHY controller functions. The Ethernet MAC module implements standard Ethernet MAC functionality. The Ethernet MAC is connected to an external Ethernet PHY function. The MAC configuration provides bridging between Ethernet and the powerline. The PHY configuration emulates Ethernet PHY functionality and provides HomePlug AV connectivity to devices designed to communicate over an Ethernet network.

The MII (Ethernet) interface has separate transmit and receive packet buffering. When operating as a MAC the MII transmit FIFO is 2 KB and the receive FIFO is 8 KB. When operating as a PHY controller, the MII transmit FIFO is 8 KB and the receive FIFO is 2 KB.

2.1.1. MII MAC

The MII MAC configuration operates as an IEEE 802.3 10/100-Mbps Ethernet MAC connected to an external 10/100-Mbps Ethernet PHY. The INT6400 MAC firmware configures the internal MII MAC based on firmware configuration and MMEs (message management entry). External devices do not have direct access to any MII MAC registers in the INT6400.

2.1.2. MII PHY

The MII PHY emulation hardware connects to an external 10/100-Mbps Ethernet MAC. The default PHY functionality is configured through standard management data interface communications (MDC and MDIO) and may be overridden by the INT6400 MAC firmware access to the PHY emulation registers. The interface supports the standard control and status register.

- Link speed at 10 Mbps or 100 Mbps
- Full-duplex or half-duplex operation
- Management data interface base address
- Isolate to disconnect the PHY from the MII port

2.2. SPI Interface

The INT6400 has a serial peripheral interface (SPI) bus used to configure the INT6400 and load the software image from an external serial flash. The interface has 2 device chip selects; 1 for the boot memory, and 1 for additional memory devices or other peripherals. The MAC services the SPI port interface directly. The SPI interface signals and functions are defined in Table 13

2.3. SDRAM Interface

The INT6400 uses SDRAM for run-time firmware storage, program execution support and data buffers for PLC transactions. The INT6400 SDRAM controller supports up to 64MB of SDRAM. A partial list of SDRAM devices supported by the INT6400 is shown in Table 3. Contact the Intellon Applications Support Group for additional supported devices. Depending on the application, Intellon INT6400 firmware requires a minimum of 8 Mbytes of SDRAM for proper operation. Intellon strongly recommends that the board design route all SDRAM address lines as this allows maximum flexibility to change memory size as required for a given application.

The INT6400 SDRAM controller utilizes a 16-bit data bus and operates at a SDRAM clock speed of 150MHz. SDRAM data bus width and clock frequency are controlled by firmware running on the internal ARM processor. This requires an SDRAM whose speed is at least 166 MHz.

Table 3: Supported SDRAMs

Vendor	Part Number	Speed Grades	Memory Size	Configurations 54-pin TSOP II
Etron	EM638165TS-6IG	166MHz: -6 (CL=3)	4Meg x 16	16-bit with 1 device = 8MB
Micron	MT48LC4M16A2TG-6	166MHz: -6 (CL=3)	4Meg x 16	16-bit with 1 device = 8MB
	MT48LC8M16A2TG-6A	167MHz: -6 (CL=3)	8Meg x 16	16-bit with 1 device = 16MB
	MT48LC16M16A2TG-6A	167MHz: -6 (CL=3)	16Meg x 16	16-bit with 1 device = 32MB

2.4. INT6400 AFE Interface

2.4.1. INT6400 Data Flow

The INT6400 data flow architecture is based on dedicated control and packet data buses and dedicated Direct Memory Access (DMA) controllers that provide unimpeded access to critical system resources, most notably, the external SDRAM and internal Static Random Access Memory (SRAM). An internal SRAM, which is separate from the internal processor Tightly Coupled Memories (TCMs), stores time-critical descriptor chains, while the external SDRAM stores the less time-critical descriptor chains, as well as the packet data. All of the devices connected to the control and packet data buses have dedicated DMA controllers that use firmware-controlled descriptor chains to move data to and from SDRAM and SRAM. DMA controller and descriptor chains are also used with Integrity Check Value (ICV) modules. The two ICV modules are used to read and compute a 32-bit Cyclical Redundancy Check (CRC) on a single block or multiple blocks of memory. Once the firmware initializes the MAC and PHY descriptor chains, the DMA controllers move data without processor intervention thus reducing system overhead. In addition, descriptor chaining allows for data reuse without the overhead associated with multiple data moves or data copies.

Transmit and receive data flows are inverse processes. The transmit data flows from host interface to SDRAM and SDRAM to the powerline through the PHY. The transmit process chains DMA descriptors to receive the application data from the external source device; encapsulates the application data into HomePlug AV MAC frames; calculates the ICV on the MAC frame; and segments the MAC frames for transmission on the powerline. The receive path data flows from powerline to SDRAM through the PHY and from SDRAM to the host interface. The receive process chains DMA descriptors to reassemble MAC frames received from the powerline; calculates the ICV on the MAC frame; removes the MAC frame encapsulation; and transmits the application data to the external destination device.

2.4.2. Interface to INT1400 AFE

The Analog Front End (AFE) interfaces the PHY with the companion amplifier IC, INT1400. The companion amplifier connects the INT6400 IC to the powerline network, and provides amplification and signal conditioning in both the transmit and receive directions.

This interface also provides the automatic gain control (AGC) logic to external programmable gain amplifier via GAIN[4:0] signals. The parallel Gain outputs determine the gain of both the RX and TX path depending on which is active. The TX Enable (TXEN) signal determines which path RX or TX is activated.
The figure below is a timing diagram of this interface.

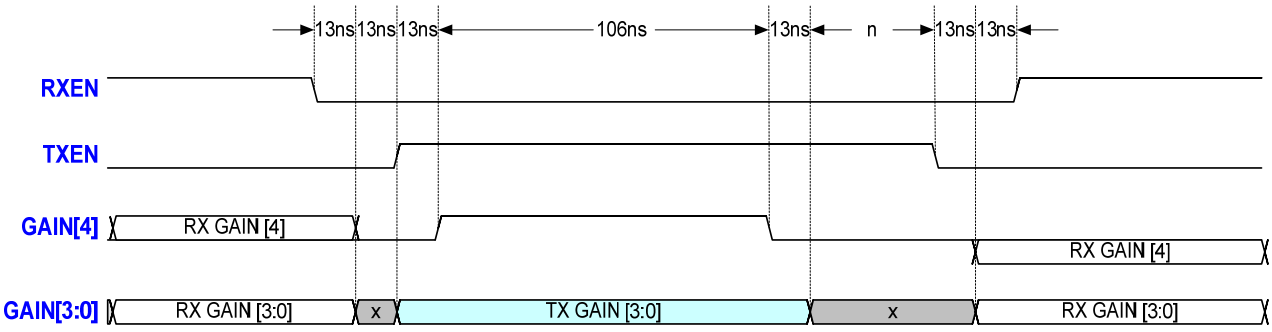


Figure 3: AFE Timing Diagram

RXEN and TXEN will not to be asserted at the same time.
RXEN de-assertion time to TXEN assertion time will be 26 ns apart or 2x75 MHz clocks.
TXEN de-assertion time to RXEN assertion time will be 26 ns apart or 2x75 MHz clocks.

GAIN[4:0] is a shared Gain Control bus that programs the transmit and receive amplifier gains.

When TXEN is asserted, GAIN[4] is used to enable GAIN[3:0] to be latched for the TX PGA. GAIN[4] will be asserted for 106 ns (8 x 75 MHz clocks). During this time, GAIN[3:0] will represent the TX GAIN to be latched into the TX PGA of the INT1400.

In the diagram above, X represents “don’t care” values.

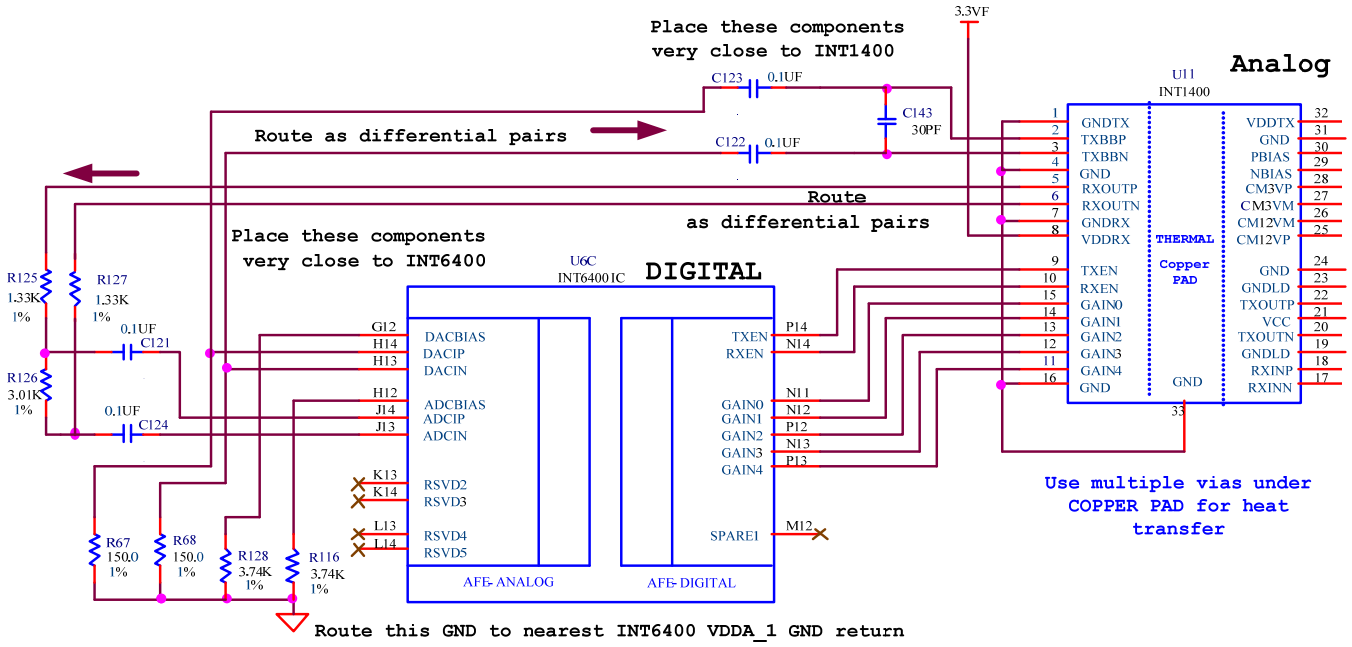


Figure 4: Typical Application Diagram

Figure 4: Typical Application Diagram illustrates the 6400/1400 chip set implementation with special notes for the PCB designer. The designer must pay particular attention to paralleled differential signal lines and component placements. See Application Note 26003872: INT6300 to INT6400 Conversion.

3. Timing Constraints

3.1. System Clock and Reset Timing

Table 4: System Clock and Reset Timing Specifications

Parameter		Min	Max	Units
37.5-MHz OSCIN Input Reference				
t_{CLKp} See Notes	OSCIN Period	26.666 - 25 ppm	26.666 + 25 ppm	ns
t_{CLKhi}	OSCIN High Time	13	13.666	ns
t_{CLKlo}	OSCIN Low Time	13	13.666	ns
GPIO configuration SETUP and Reset Timing				
t_{GPIO_SETUP} *4.	GPIO Config. SETUP	100	-	ns
t_{RSTa}	RESET# Active	100	-	ms
t_{RST_PHYa}	PHY_RST#	109	110	ms

Note 1: t_{RSTa} is measured from the time power, VDD_{CORE} and VDD_{IO}, and clock, OSCIN, are stable. RESET# is asynchronous to PLL_IN.

Note 2: All power supply voltages must be stable and within specification before the beginning of the RESET# Active time.

Note 3: Power supply voltages may be applied in any sequence during power up or removed in any order during power down.

Note 4: GPIO Configuration signals have a hold time of 5ns.

Note 5: OSCIN may be applied externally if crystal oscillator circuit is not used. Maximum OSCIN input voltage is 1.1Vpp (Nominal 0.8Vpp). If crystal is used monitor waveform at TP12.

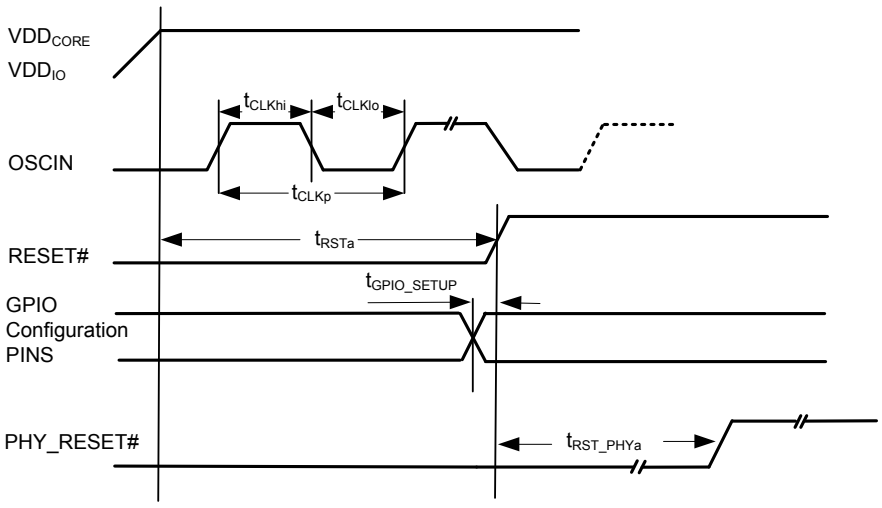


Figure 5: System Clock and Reset Timing

3.2. MII Timing

Table 5: MII Timing Specifications

Parameter		Min	Max	Units
MII Tx Bus (MTX) and Rx Bus (MRX) Timing				
t_{CLKp}	CLK Period (100 Mb/s, 10 Mb/s)	40/400	-	ns
t_{CLKhi}	CLK High Time (100 Mb/s, 10 Mb/s)	14/140	26/260	ns
t_{CLKlo}	CLK Low Time (100 Mb/s, 10 Mb/s)	14/140	26/260	ns
t_{OV}	Output Valid Time All MTX Signals	10	28	ns
t_{SU}	Input Set Up Time All MRX Signals	10	-	ns
t_{H}	Input Hold Time All MRX Signals	10	-	ns
Management Data Interface Clock (MDC) and Data (MDIO) Timing				
t_{MDCp}	MDC period (100 Mb/s, 10 Mb/s)	400	-	ns
t_{MDChi}	MDC high time (100 Mb/s, 10 Mb/s)	150	-	ns
t_{MDClo}	MDC low time (100 Mb/s, 10 Mb/s)	150	-	ns
t_{MOV}	Output Valid Time MDIO	0	300	ns
t_{MSU}	Input Set Up Time MDIO	10	-	ns
t_{MH}	Input Hold Time MDIO	10	-	ns

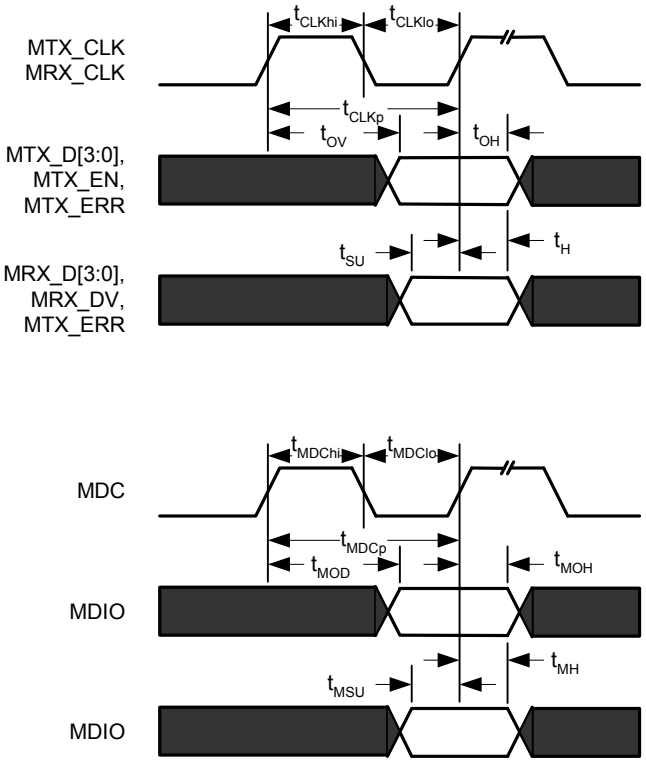


Figure 6: MII Timing

Table 6: MII PHY Timing Specifications

Parameter		Min	Max	Units
MII Tx Bus (MTX) and Rx Bus (MRX) Timing				
t_{CLKp}	CLK Period (100 Mb/s, 10 Mb/s)	40/400	-	ns
t_{CLKhi}	CLK High Time (100 Mb/s, 10 Mb/s)	14/140	26/260	ns
t_{CLKlo}	CLK Low Time (100 Mb/s, 10 Mb/s)	14/140	26/260	ns
t_{OV}	Output Valid Time All MRX Signals	-	25	ns
t_{OH}	Output Hold Time All MRX Signals	-	10	ns
t_{SU}	Input Set Up Time All MTX Signals	10	-	ns
t_{H}	Input Hold Time All MTX Signals	10	-	ns
Management Data Interface Clock (MDC) and Data (MDIO) Timing				
t_{MDCp}	MDC period (100 Mb/s, 10 Mb/s)	400	-	ns
t_{MDChi}	MDC high time (100 Mb/s, 10 Mb/s)	150	-	ns
t_{MDClo}	MDC low time (100 Mb/s, 10 Mb/s)	150	-	ns
t_{MOV}	Output Valid Time MDIO	-	300	ns
t_{MOH}	Output Hold Time MDIO	-	0	ns
t_{MSU}	Input Set Up Time MDIO	10	-	ns
t_{MH}	Input Hold Time MDIO	10	-	ns

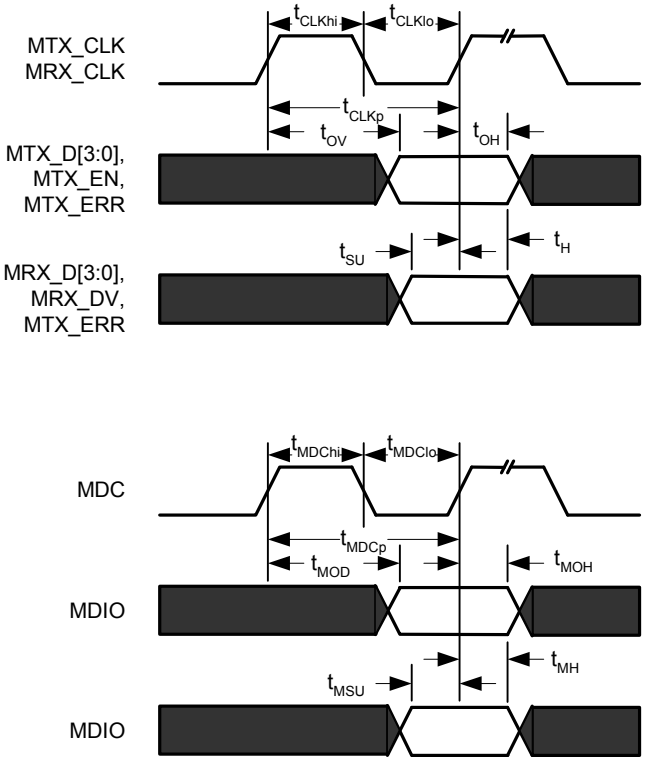


Figure 7: MII PHY Timing

3.3. SPI Timing

Table 7: SPI Timing Specifications

Parameter		Min	Max	Units
t_{CLKp}	SPI_CLK Period	25	-	ns
t_{CLKhi}	SPI_CLK High Time	11	-	ns
t_{CLKlo}	SPI_CLK Low Time	11	-	ns
t_{OV}	Output Valid Time	5	-	ns
t_{OH}	Output Hold Time	5	-	ns
t_{SU}	Input Setup Time	5	-	ns
t_H	Input Hold Time	5	-	ns

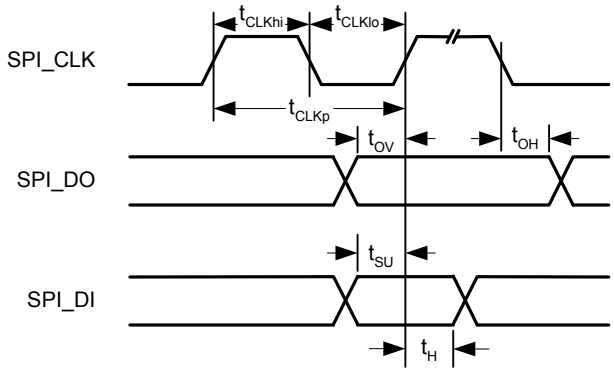


Figure 8: SPI Timing

3.4. SDRAM Timing

The output timing reference is SD_CLK and the input timing reference is SD_HCLK.

Table 8: SDRAM Timing Specifications

Parameter		Min	Max	Units
t_{CLKp}	SD_CLK and SD_HCLK Period	6.6	-	ns
t_{CLKhi}	SD_CLK and SD_HCLK High Time	3	-	ns
t_{CLKlo}	SD_CLK and SD_HCLK Low Time	3	-	ns
t_{CLKpd}	SD_HCLK Delay Relative to SD_CLK	0	3	ns
t_{OV}	Output Valid Time All Signals	1	-	ns
t_{OH}	Output Hold Time All Signals	1	-	ns
t_{SU}	Input Data Setup Time	2	-	ns
t_H	Input Data Hold Time	0	-	ns

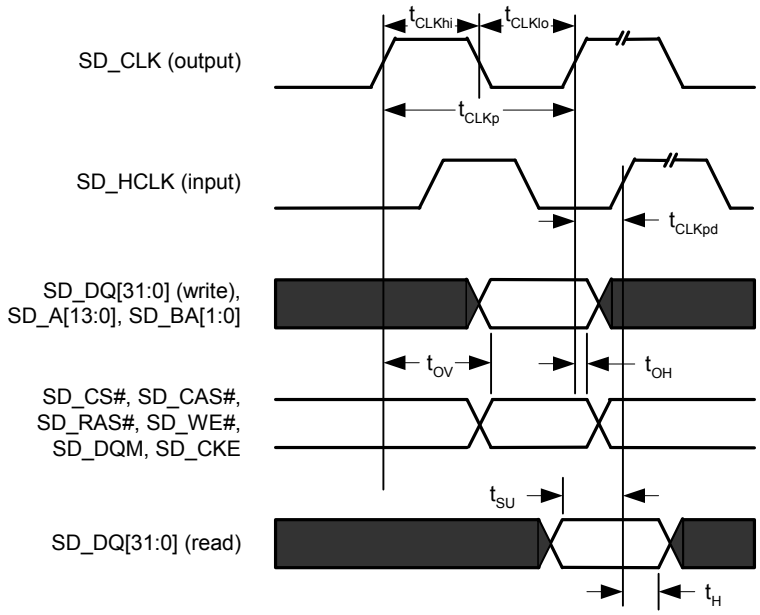
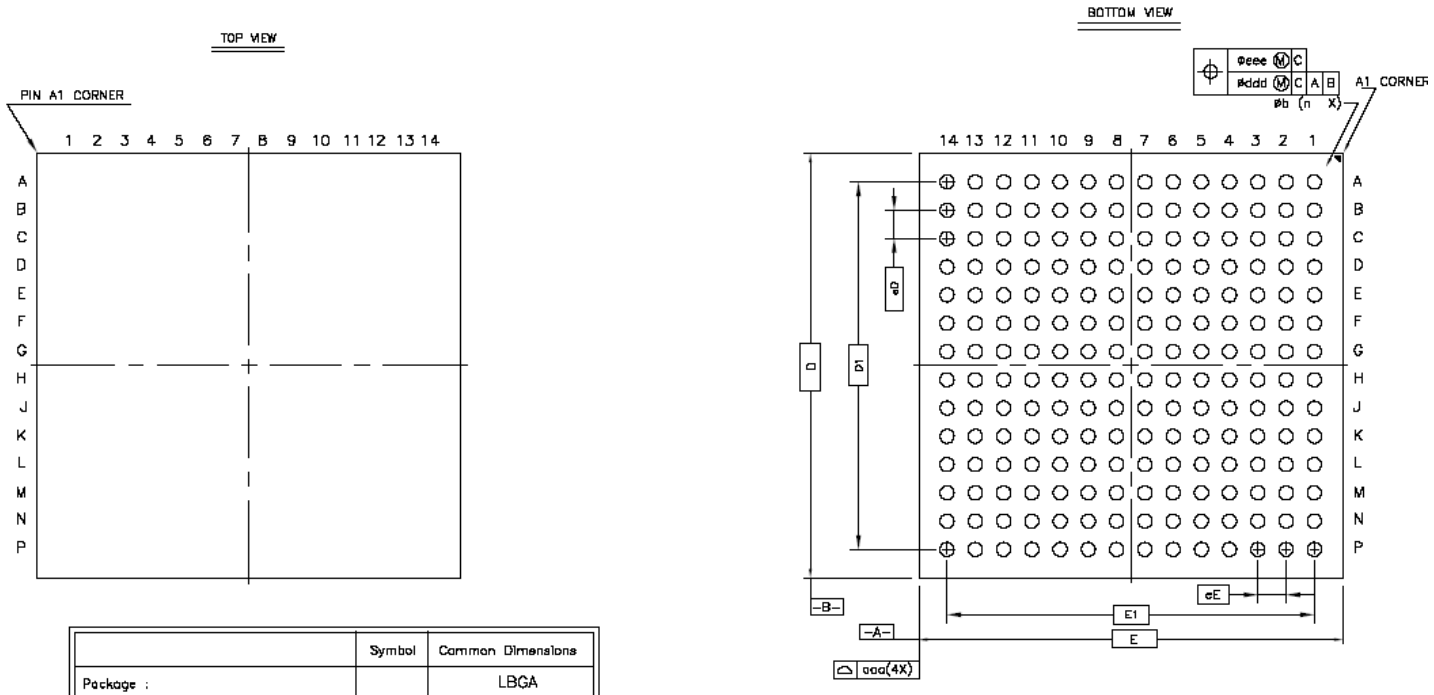


Figure 9: SDRAM Timing

4. INT6400 Package Data

4.1. Physical Dimensions



		Symbol	Common Dimensions
Package :			LBGA
Body Size:	X	E	15
	Y	D	15
Ball Pitch :	X	eE	1.000
	Y	eD	1.000
Total Thickness :		A	1.400 MAX
Mold Thickness :		M	0.530 Ref.
Substrate Thickness :		S	0.360 Ref.
Ball Diameter :			0.500
Stand Off :		A1	0.380 ~ 0.480
Ball Width :		b	0.440 ~ 0.640
Package Edge Tolerance :		aaa	0.200
Mold Flatness :		bbb	0.350
Coplanarity:		ccc	0.200
Ball Offset (Package) :		ddd	0.250
Ball Offset (Ball) :		eee	0.100
Ball Count :		n	196
Edge Ball Center to Center :	X	E1	13.000
	Y	D1	13.000

Figure 10: Detailed INT6400 Package Dimensions

This package conforms to JEDEC 95 Publiciatons Issue and JEDEC MO-205 Issue G Design Requirement".

4.2. INT6400 Package Markings

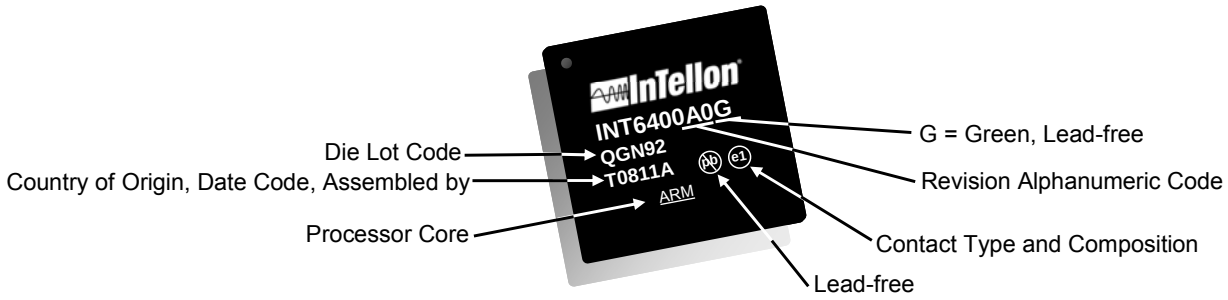


Figure 11: INT6400 Package Markings

Line 1: INT6400A0G = Part Nomenclature
(INT6400 = part number, A1 = alphanumeric revision indicator, G = Green package type = lead free)
Line 2: INT6400 die process lot number (QGN92)
Line 3: First letter = Country of Origin (T = Taiwan, S = Singapore, K = South Korea, P = Philippines, M = Malaysia)
Four-digit Date Code (YY = year, WW = week number)
Last letter indicates assembled by (A=OSE, B=Amkor, C=ASE, D=Carsem, E=STATS ChipPAC, F=Signetics)
Pb crossed circle symbol = 'no lead' = lead-free
e# circle symbol = contact composition indicator
e1 = ball contacts made of SnAgCu (96.5 Sn / 3.0 Ag / 0.5 Cu)
Line 4: ARM processor symbol

4.3. INT6400TR Ordering

Part Number: INT6400TR (lead-free on tape and reel)
Lead-free is the only package option.

4.4. INT6400 Ball Assignments

The INT6400G package is a Pb-free (G suffix), 15mm x 15mm, LBGA-196 with a 1 mm ball pitch.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	SD_A1	SD_A6	SD_A2	SD_A4	MTX_EN	RSVD13	RSVD11	MTX_CLK	RSVD12	MRX_CLK	RSVD19	MRX_D2 / AFE_QD5	MDC	MDIO	A
B	SD_A8	SD_A0	SD_A7	SD_A3	RSVD14	RSVD15	MTX_D1 / AFE_QD8	MTX_D0 / AFE_QD1	RSVD1	RSVD20	RSVD18	MRX_D1 / AFE_QD3	RSVD17	TDO	B
C	SD_A11	SD_A9	SD_A10	SD_A5	COL / AFE_QD9	RSVD16	MTX_D3	MTX_D2 / AFE_QD4	CRS / AFE_QD7	MRX_D3 / AFE_QD6	MRX_DV	MRX_D0 / AFE_QD2	MRX_ERR	RESET#	C
D	SD_BA1	SD_BA0	SD_A12	VCORE	VCORE	VDDIO	VCORE	VDDIO	RTCK	VDDIO	TRST#	TCK	TDI	OSCOUT	D
E	SD_RAS#	SD_CKE	SD_CS#	VDDIO	VCORE	VCORE	VCORE	VCORE	VCORE	TMS	VDDA_1	VDDA_3	PLL_BYP	OSCIN	E
F	RSVD6	RSVD7	SD_CAS#	VDDIO	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VDDA_1	VPLL_3	VPLL_1	F
G	SD_CLKIN	SD_CLKOUT	RSVD8	VCORE	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	DACBIAS	VSS_PLL3	VSS_PLL1	G
H	SD_DQM0	SD_DQM1	SD_WE#	VDDIO	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	ADCBIAS	DACIN	DACIP	H
J	RSVD9	RSVD10	SD_DQ8	VCORE	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VDDA_1	ADCIN	ADCIP	J
K	SD_DQ7	SD_DQ9	SD_DQ6	VDDIO	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VDDA_1	RSVD2	RSVD3	K
L	SD_DQ10	SD_DQ5	SD_DQ11	VCORE	VDDIO	VCORE	VCORE	VCORE	VCORE	VCORE	VCORE	VDDA_3	RSVD4	RSVD5	L
M	SD_DQ4	SD_DQ12	SD_DQ3	GPIO0 / IRQ0 / SYNC_DET	GPIO1 / IRQ1 / AFE_D1	GPIO4 / SPEED / AFE_D4	GPIO9 / ADI_ENA	GPIO10 / BM_SEL / AFE_D8	SPI_DI	VDDIO	VCORE	SPARE1	VSS	VSS	M
N	SD_DQ13	SD_DQ2	SD_DQ1	SPI_CS# / PHY_RST	GPIO2 / ANEN / AFE_D2	GPIO5 / MD_A3 / AFE_D5	GPIO6 / CFG_SEL / AFE_D6	SPI_DO	SPI_MEM#	RXD	GAIN0	GAIN1	GAIN3	RXEN	N
P	SD_DQ14	SD_DQ15	SD_DQ0	PHY_CLK / DACCLK / DUPLEX	GPIO11 / AFE_D9	GPIO7 / MD_A4 / AFE_D7	GPIO8 / MP_SEL	GPIO3 / ISODEF / AFE_D3	SPI_CLK	ZC_IN	TXD / ADCCLK	GAIN2	GAIN4	TXEN	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

INT6400 Ball Map

MII Host Ports	17
SDRAM Port	40
GPIO, SPI & UART	21
Chip Reset & JTAG	7
System Clock	3
AFE Control (Digital I/O)	7
AFE Analog	6

VDD DIGITAL I/O 3.3V	9
Core Voltage 1.0V	23
GROUND (VSS)	32
AFE Analog 1.0V	4
VDD I/O ANALOG 3.3V	2
PLL Analog 1.0V	1
PLL Analog 3.0V	1
GROUND (VSS_PLL1 for PLL 1V	1
GROUND (VSS_PLL3 for PLL 3V	1

SIGNAL BALLS	101
PWR AND GND	74
TRUE SPARE	1
SPARE (USED ON INT6500)	20
TOTAL BALLS	196

Figure 12: INT6400 Low-profile Flat Ball Grid Array Ball Assignments

NOTE: the package and ball assignments are subject to change.

4.5. INT6400 Thermal Data

Table 9 provides thermal resistance data for the INT6400 at maximum power dissipation. Refer to the Intellon Thermal Management Application Note for further information.

Table 9: INT6400 Thermal Resistance Data

Parameter	Value (°C/W)
ΘJA	27.1 (natural convection) 24.2 (1 m/s forced air flow)

5. INT6400 Signals

5.1. Common Signals

Table 10: System Interface Signals

Signal	Type	Function
RESET#	I	**Power on Reset.** Active-low Power-on-Reset input.
OSCIN	I	**Crystal Oscillator Inverter Input**
OSCOUT	O	**Crystal Oscillator Inverter Output**
PLL_BYP	O	**PLL Bypass**
TCK	I	Connect to GND for normal operation.
TDI	I	Connect to GND for normal operation.
RTCK	O	Leave unconnected for normal operation.
TDO	I/O	Leave unconnected for normal operation.
TMS	I	Connect to GND for normal operation.
TRST#	I	Connect to GND for normal operation.
PHY_CLK	O	**25MHz Clock Out** This output is a dedicated clock output that can be used to drive the clock input on an external Ethernet PHY. This clock output is only available when the INT6400 is configured in MAC mode, and not in PHY mode of operation. Note that if this output is used, it is strongly advised that the corresponding PHY_RST# signal also be connected to the external Ethernet PHY.

5.2. AFE Signals

Table 11: AFE Signals

Signal	Type	Function
ZC_IN	I	**Zero Cross Detector Input.** The zero cross detector provides a logic level signal with safety isolation that corresponds to the polarity of the AC power line waveform. This information synchronizes the channel adaptation of the INT6400 to the line cycle periodic noise present on the power line
ADCBIAS	Resistor	**ADC BIAS**. External reference resistor that sets bias current
ADCIN	I	**Differential In.** Negative differential input that connects to the output pin RXOUTN of INT1400
ADCIP	I	**Differential In.** Positive differential input that connects to the output pin RXOUTP of INT1400
DACBIAS	Resistor	**DAC BIAS.** External reference resistor that sets bias current.
DACIN	O	**Differential Out.** Negative differential output that connects to the input pin TXBBN of INT1400
DACIP	O	**Differential Out.** Positive differential output that connects to the input pin TXBBP of INT1400
GAIN[4:0]	O	**Analog Front Gain Control.** GAIN [4:0] is 4-bit transmit amplifier gain control and 5-bit receiver gain control.
TXEN		**Analog Front End Transmit Enable.** TXEN is used to enable the input latch on the INT1400.
RXEN		**Analog Front End Receive Enable.**

5.3. SDRAM Signals

Table 12: SDRAM Signals

Signal	Type	Function
SD_A[12:0]	O	**SDRAM Address.** The 13-bit bus contains the memory address for SDRAM accesses
SD_BA[1:0]	O	**SDRAM Bank Select.** The 2-bit bus, SD_B[1:0] contains the bank select for SDRAM accesses.
SD_CS#	O	**SDRAM Chip Select.** SD_CS# is the chip select for the SDRAM.
SD_RAS#	O	**SDRAM Row Address Strobe.** SD_RAS# is the row address strobe for the SDRAM.
SD_CAS#	O	**SDRAM Column Address Strobe.** SD_CAS# is the column address strobe for the SDRAM.
SD_WE#	O	**SDRAM Write Enable.** SD_WE# is the write enable for the SDRAM.
SD_CKE	O	**SDRAM Clock Enable.** If low, this signal indicates to the SDRAM to enter the power-down state.
SD_CLKOUT	O	**SDRAM Clock.** SD_CLK is the clock source for the SDRAM. SD_CLK is equal in frequency to the internal system bus clock.
SD_DQM[1:0]	O	**SDRAM Data Mask.** SD_DQM[1:0] are the data masks for SD_DQ[15:0] during SDRAM read and write accesses. SD_DQM[1] corresponds to SD_DQ[15:8] SD_DQM[0] corresponds to SD_DQ[7:0]
SD_DQ[15:0]	I/O	**SDRAM Data.** The 16-bit bus contains the memory read/write data for SDRAM accesses.
SD_CLKIN	I	**SDRAM Return Clock**

5.4. GPIO and SPI Signals

Table 13: GPIO and Serial Interfaces

Signal	Type	Function
SPI_MEM#	O	**SPI Memory Chip Select**. SPI_MEM# is the chip select used to enable the serial boot flash.
SPI_CS# PHY_RST#	O	**SPI Chip Select.** SPI_CS# is the chip select used to enable additional SPI devices. Leave unconnected if unused. If used as PHY_RST, connect to an external Ethernet PHY. This reset output is a stretched version of the RESET# input.
SPI_CLK	O	**SPI Clock**. SPI_CLK provides the SPI interface timing. Instructions, addresses, or data present at SPI_DI are latched on the rising edge of SPI_CLK. Data on SPI_DO changes after the falling edge of SPI_CLK.
SPI_DI	I	**SPI Data In.** The SPI_DI is used to transfer serial data into the **INT6400**. SPI_DI is latched on the rising edge of SPI_CLK.
SPI_DO	O	**SPI Data Out.** SPI_DO is used to transfer serial data out of the **INT6400**. SPI_DO is shifted out on the falling edge of SPI_CLK.
RXD	I	**Receive Serial Data.** RXD receives serial data from the UART. Connect to GND if the UART is unused.
TXD	O	**Transmit Serial Data.** TXD transmits serial data to the UART. Leave unconnected if the UART is unused.
GPIO[11:0]	I/O	**General Purpose I/O**. Software programmable inputs or outputs, which can also be used as an external interrupt source. Note that these GPIO signals also have additional functionality as straps – refer to section 6.2.1for details.

5.5. MII Signals

Table 14: MII MAC and PHY Mode Signals

Signal	Type		Function
	MAC	PHY	
MTX_CLK	I	O	**MII Transmit Clock.** TX_CLK is a continuous clock that provides a timing reference for the transfer of the TX_EN and TX_D[3:0] signals from the MAC core to the PHY controller. The PHY controller sources TXCLK. The operating frequency of TXCLK is 25 MHz when operating at 100 Mbps and 2.5 MHz when operating at 10 Mbps. The PHY controller tri-states TX_CLK in isolate mode.
MTX_D[3:0]	O	I	**MII Transmit Data.** The MAC core drives TX_D[3:0] and the PHY controller receives TX_D[3:0]. TX_D[3:0] transitions synchronously with respect to TX_CLK. For each TX_CLK period in which TX_EN is asserted, TX_D[3:0] is valid. TX_D0 is the least-significant bit. The PHY controller ignores TX_D[3:0] in isolate mode.
MTX_EN	O	I	**MII Transmit Enable.** A high assertion on TXEN indicates that the MAC core is presenting nibbles to the PHY controller for transmission. The INT6400 MAC core asserts TX_EN with the first nibble of the preamble and keeps TX_EN asserted while all nibbles to be transmitted are presented to the MII. TX_EN is de-asserted prior to the first TX_CLK following the final nibble of the frame. TX_EN transitions synchronously with respect to TX_CLK. The PHY controller ignores TX_EN in isolate mode.
MRX_CLK	I	O	**MII Receive Clock.** RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV and RX_D[3:0] signals from the PHY controller to the MAC core. The PHY controller sources RX_CLK. RX_CLK frequency is equal to 25% of the data rate of the received signal on the Ethernet cable. The PHY controller tri-states RX_CLK in isolate mode.

Signal	Type		Function
	MAC	PHY	
MRX_D[3:0]	I	O	**MII Receive Data.** The PHY controller drives RX_D[3:0] and the MAC core receives RX_D[3:0]. RX_D[3:0] transition synchronously with respect to RX_CLK. For each RXCLK period in which RX_DV is asserted, RX_D[3:0] is valid. RX_D0 is the least-significant bit. The PHY controller tri-states RX_D[3:0] in isolate mode.
MRX_DV	I	O	**MII Receive Data Valid.** The PHY controller asserts RX_DV to indicate to the MAC core that it is presenting the recovered and decoded data bits on RX_D[3:0] and that the data on RX_D[3:0] is synchronous to RX_CLK. RX_DV transitions synchronously with respect to RX_CLK. RX_DV remains asserted continuously from the first recovered nibble of the frame through the final recovered nibble, and is de-asserted prior to the first RX_CLK that follows the final nibble. The PHY controller tri-states RX_DV in isolate mode.
MRX_ERR	I	O	**MII Receive Error.** The PHY controller asserts RX_ERR high for one or more RX_CLK periods to indicate to the MAC core that an error (a coding error or any error that the PHY is capable of detecting that is otherwise undetectable by the MAC) was detected somewhere in the current frame. RX_ERR transitions synchronously with respect to RX_CLK. While RX_DV is de-asserted, RX_ERR has no effect on the MAC core. The PHY controller tri-states RX_ERR in isolate mode.
COL	I	O	**MII Collision Detected.** The PHY controller asserts COL when it detects a collision on the medium. COL remains asserted while the collision condition persists. COL signal transitions are not synchronous to either the TX_CLK or the RX_CLK. The MAC core ignores the COL signal when operating in the full-duplex mode. The PHY controller tri-states COL in isolate mode.
CRS	I	O	**MII Carrier Sense.** The PHY controller asserts CRS when either transmit or receive medium is non-idle. The PHY de-asserts CRS when both transmit and receive medium are idle. The PHY must ensure that CRS remains asserted throughout the duration of a collision condition. The transitions on the CRS signal are not synchronous to either the TX_CLK or the RX_CLK. The PHY controller tri-states CRS in isolate mode.
MDC	O	I	**MII Management Data Clock.** The MAC core sources MDC as the timing reference for transfer of information on the MDI/MDO signals. MDC signal has no maximum high or low times. MDC minimum high and low times are 160 ns each, and the minimum period for MDC is 400 ns.
MDIO	I/O	I/O	**MII Management Data In/Out.** This is the data input signal from the PHY controller. The PHY drives the Read Data synchronously with respect to the MDC clock during the read cycles. This is also the data output signal from the MAC core that drives the control information during the Read/Write cycles to the PHY controller. The MAC core drives the MDO signal synchronously with respect to the MDC.

5.6. Internal Pull-Up/Down

The following signals have an internal pull-up or pull-down within their I/O pad.

Table 15: Internal Pull-Up/Down

Signal Name	Pull Up/Down
GPIO[11]	Down
GPIO[10]	Down
GPIO[9]	Down
GPIO[8]	Up
GPIO[7]	Down
GPIO[6]	Down
GPIO[5]	Up
GPIO[4]	Up
GPIO[3]	Up
GPIO[2]	Up
GPIO[1]	Up
GPIO[0]	Up
UART_RXD	Up
SPI_DI	Down
PHY_CLK	Up

6. Design Considerations

6.1. Layout, Layering and Soldering

6.1.1. INT6400 Layout Recommendations

Table 16 and Table 17 present Intellon's layout recommendations for an INT6400 printed circuit board. The main design concerns are the LBGA pad size, trace width, etch spacing, routing grid, via diameter, and surface finish that occur under the INT6400. Also included are the recommended stack-ups for a 4-layer and 6-layer printed circuit board.

Table 16: INT6400 Pad Sizes

Parameter	Size
LBGA pad size	0.40mm (16mil)
Pad mask opening	0.50mm (20mil)
LBGA VIA O.D.	0.43mm (17mil)
LBGA VIA I.D.	0.254mm (10mil)
Via mask opening	none
Minimum etch spacing	0.10mm on 0.10 (4mil on 4mil)

Table 17: Circuit Board Considerations

Parameter	Value
Routing Grid	0.10mm (4mil)
Board starting copper	0.5oz (outer layers)
Board starting copper	1.0oz (inner layers)
Board surface finish	Electroless Nickel (EN) 50>250uin, followed By Immersion Gold 4>12uin

6.1.2. INT6400 Board Layering

6.1.2.1. INT6400 4 layer stack-up:

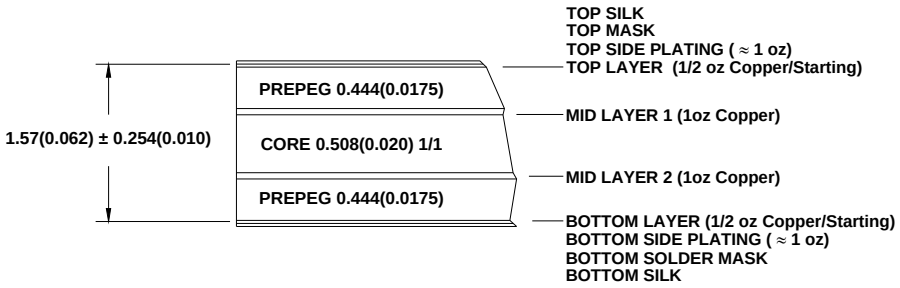


Figure 13: 4-Layer Circuit Board Stack

6.1.2.2. INT6400 6 layer stack-up:

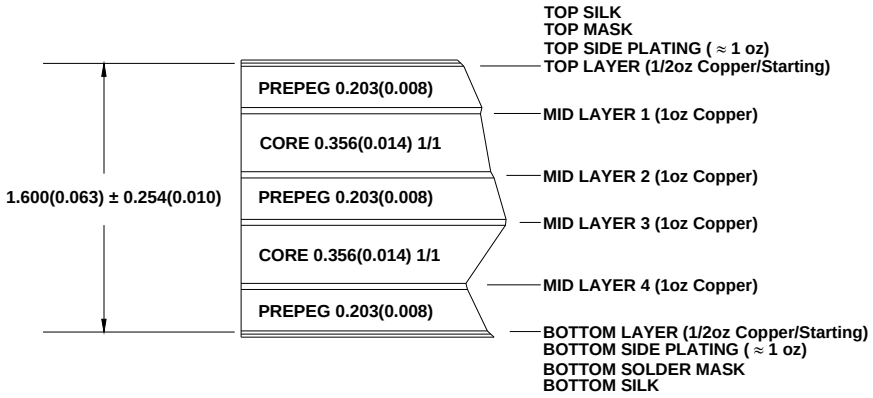


Figure 14: 6-Layer Circuit Board Stack

6.1.3. INT6400 Soldering Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	260 °C
Time within 5 °C of actual Peak Temperature (tp)	20-40 seconds
Ramp-Down Rate	6 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.

Note: All temperatures are measured on the top surface of the package.

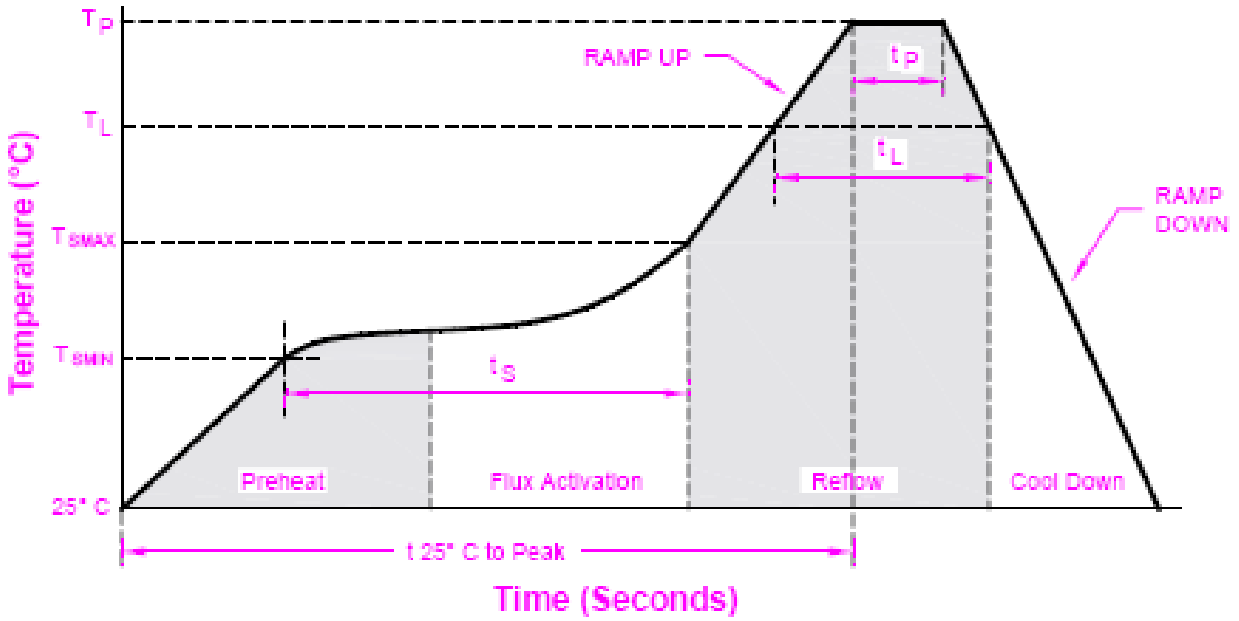


Figure 15: INT6400 Soldering Profile – Tp = 260° C

Note: Reflow cycling at the maximum temperature is limited to 3 cycles.

6.2. INT6400 Configuration Options

6.2.1. GPIO Strapping

The INT6400 mode and boot options are selected by the initial condition of GPIO pins. If a GPIO pin is not used and its internal strapping resistor sets the booting option correctly, then the pin may be left unconnected. If a GPIO pin is not used but the internal strapping resistor sets the booting option incorrectly, then the pin must be pulled high or low to the correct booting option by an external resistor. This resistor can be 10 k-Ohms down to a few hundred Ohms. 3.3 k-Ohms is typical. Many GPIO pins are driven by firmware for LED output immediately after boot up so connecting these GPIO directly to ground or VDDIO is unacceptable. See Table 18: Internal GPIO Strapping.

Table 18: Internal GPIO Strapping

Ball Name	Strap Function	Default Strap	Default Function
GPIO0	N/A	Pull-Up	N/A
GPIO1	N/A	Pull-Up	N/A
GPIO2	N/A	Pull-Up	N/A
GPIO3	ISODEF	Pull-Up	PHY Mode: Hi-Z MII Interface
GPIO4	SPEED	Pull-Up	PHY Mode: 100Mbps
GPIO5	MD_A3	Pull-Up	PHY Mode: PHY Address 0x0100
GPIO6	CFG_SEL	Pull-Down	Boot: SDRAM Parameters from Host
GPIO7	MD_A4	Pull-Down	PHY Mode: PHY Address 0x0100
GPIO8	MP_SEL	Pull-Up	Host: MAC Mode
GPIO9	N/A	Pull-Down	Pull down.
GPIO10	BM_SEL	Pull-Down	Boot: Firmware from Host
PHY_CLK	DUPLEX	Pull-Up	PHY Mode: Full Duplex

6.2.2. Host Mode Select

The **MP_SEL** (MAC/PHY) strap is used to specify whether the chip is configured for MII MAC mode, or in MII PHY mode (i.e. reverse-MII mode). The encoding of this signal is shown in Table 19.

Table 19: MII Mode Selection

MP_SEL	Mode
0	MII PHY
1	MII MAC

In MII PHY mode, there are additional configuration straps that are unique to this mode of operation.

Table 20: MII PHY Mode Speed Selection

SPEED	MII Speed
0	10 Mbps
1	100Mbps

Table 21: MII PHY Mode Duplex Selection

DUPLEX	MII Duplex
0	Half Duplex
1	Full Duplex

Table 22: MII PHY Mode Isolate Selection

ISODEF	Isolation
0	Normal Operation
1	Isolated

Table 23: MII PHY Mode MII Management Address Selection

MD_A[4:3]	MII Management Address
00	0x00
01	0x08
10	0x10
11	0x18

6.2.3. Boot Straps

The **BM_SEL** strap is used to determine the source of the boot code for the embedded ARM processor. Similarly, the **CFG_SEL** strap is used to determine the source of the SDRAM configuration applet. The encodings for these two signals is shown in Table 24.

Table 24: Boot and SDRAM Configuration Straps

BM_SEL	CFG_SEL	Meaning
0	0	Load SDRAM configuration and boot code from external host
0	1	Load SDRAM configuration applet from flash, and then load boot code from external host.
1	0	Load SDRAM configuration
1	1	Load SDRAM configuration and boot code from flash.

6.3. Reset

The main chip reset is the active low RESET# input. This reset input is first passed through a Schmidt trigger input, and then goes through a small digital filter before it actually becomes the on-chip reset. While this power-on-reset signal is asserted, all clocks on all flops in the chip are active, and all on-chip registers are reset to a default state. To reduce the peak power used during this period of time, the frequency of all clocks is 8x lower than normal. Once RESET# is de-asserted, the on-chip reset is further extended by a ~4000 clocks to allow the on-chip PLL to lock. At the end of this delay, the internal clocks are brought up to their normal operating frequency, and then the majority of them are gated off. Once the ARM processor is brought out of reset, the processor jumps to address 0xFFFF0000 and the Boot ROM software takes over.

In addition to these hardware initiated resets, there are also numerous sources of software controlled reset within the INT6400. In MII PHY mode, the RESET bit in EPHY_CONTROL can reset the entire chip as well – an external Ethernet MAC that sets this bit either causes an interrupt to be given to the ARM processor, or causes an internal reset to occur. This option is again selected through a software configuration register.

Internal to the INT6400, there are also numerous sources of reset. The processor can write to internal registers to take individual modules in or out of reset, as well as it can initiate an entire chip reset. Furthermore, to recover from system problems, a watchdog reset circuit is available that can initiate a reset if the software or system have crashed.

6.4. Boot Procedure

When the INT6400 first powers-up, based upon the setting of the BM_SEL strap, the Boot ROM will attempt to either download code from an external NVRAM (non-volatile random access memory) across the SPI interface, or it will immediately go into host-boot mode.

In flash-based boot, the INT6400 will read a series of descriptors from the SPI NVRAM (a subset of the supported devices are listed in Table 25) that indicate where to fetch data from the NVRAM, and where to put it in the INT6400's internal memory or external SDRAM. Software descriptors in the NVRAM are used to specify where program code and data are located within the NVRAM, and where they should be copied within the INT6400. It is also possible to specify multiple programs – or applets – that must be downloaded and executed sequentially. If there are any errors while parsing the NVRAM descriptors, the Boot ROM will fail-over to host-mode so that a host-based application can fix the errors. Finally, if the Boot ROM gets to the end of the NVRAM's descriptor chain, it also fails-over to the host-mode.

Table 25: Supported NVMs

NVM SO8W .208mil Package Manufacturer Ordering Part Number*	NVM Organization (8-Bits)	JEDEC Code
Numonyx		
M25P80-VMW6TP	1024K x 8	20h14h
M25P16-VMW6TP	2048K x 8	20h15h
Atmel		
AT26DF161-SU	2048k x 8	46h00h
AT26DF161A-SU	2048k x 8	46h01h
Eon Silicon Solutions		
EN25F16-75HCP	2048K x 8	ID = 14h
Macronix International		
MX25L8005M2I-12G	1048k x 8	20h14h
MX25L1605DM2I-12G	2048k x 8	20h15h
MX25L3205DM2I-12G	4096k x 8	20h16h
Silicon Storage Technology		
SST25VF016B-50-4IS2AF SST25VF016B-50-4CS2AF **	2048k x 8	25h41h
Spansion LLC		
S25FL016AOLMFI01	2048k x 8	02h14h

* List show only last date tested.
** Many temperature and speed variations exist. All above 10MHz clk and Commercial are compatible.

To boot in host mode, the INT6400 first configures the host interface. For an Ethernet-MAC system, if the external Ethernet PHY is configured for auto-negotiation, the Boot ROM will perform auto-negotiation if the link isn't already established. If the link is established, or if the external PHY is configured without auto-negotiation, the Boot ROM will simply read the PHY's registers and program the INT6400's Ethernet MAC accordingly. Similarly, for Ethernet-PHY configurations, the Boot ROM will configure itself just based upon the INT6400's own straps.

Once the host interface is configured, the Boot ROM will broadcast a periodic Host Action Request MME packet from its host interface. An external application (e.g. the Intellon Device Manager) will respond to this with a series of MME packets that are used to download the firmware. The Boot ROM understands the MMEs outlined in Table 26.

Table 26: Boot ROM MMEs

MME	Comments
Host Action Request	Used by the Boot ROM to request a Firmware download from the host
Get Device/SW Version Request	Query the Boot ROM to determine chip ID, chip mask version, and chip's mode of operation.
Set SDRAM Configuration Request	Set the SDRAM controller's configuration parameters
Reset MAC Request	Reset the device
Write MAC Memory Request	Write up to 1kbyte of data into the MAC memory
Start MAC Request	Validate the checksum of a region of memory and start the
Write and Execute Applet	Write an applet to MAC memory and execute.

6.4.1. NVRAM Boot

6.4.1.1. NVM Layout

The layout of the NVM allows various memory segments to be loaded by the Boot ROM. NVM headers define memory images contained in the NVM and the location that they should be placed in the target IC's memory.

The Boot ROM will process a linked list of NVM headers. Each header will contain parameters for the location of the image in NVM and the destination address in various memory regions in the INT6400 IC. Each header will point to the location in NVM of the next header. The Boot ROM stops processing NVM memory images when the location of the next header = 0x00000000 at which point the Boot ROM will initialize the host interface and will start processing MMEs.

6.4.1.2. NVM Header Structure

There will be only one layout defined. The Boot ROM will always process the data stored in the NVM starting at address 0x00000000 and attempt to verify the validity of each NVM Header. Not only the section checksums but also the section versions of the header will be verified.

6.4.1.3. NVM Header Layout

Table 27: NVM Header

OFFSET	Field Name and Type	Description
Section 1. INT6400 Header		
0x0000	UINT32 headerVersion	Header Version number, 0x6000_0000
0x0004	UINT32 imgRomAddr	Image ROM address is the location of the INT6400 configuration image in the NVM.
0x0008	UINT32 imgAddr	Image address is internal memory location at which the image should be loaded.
0x000C	UINT32 imgLength	Image length is used to indicate the length of the image in NVM in bytes.
0x0010	UINT32 imgChecksum	Image checksum is the inverted 32-bit XOR checksum of the downloadable image.

OFFSET	Field Name and Type	Description
0x0014	UINT32 iEntryPointFnPtr	Runtime starting address of the image. Following validation of the loaded image from NVM via imgChecksum, the Boot ROM will start the image via this address.
0x0018	{Mask[15:0], MinorVersion[15:0]}	The Mask specifies which devices should skip loading this section, and the MinorVersion specifies the minor version of this image format.
0x001C	Reserved	Must be zero
0x0020	Reserved	Must be zero
0x0024	UINT32 iNextHeader	Location in NVM of the next header.
0x0028	UINT32 hdrChecksum	Header checksum is the inverted 32-bit XOR checksum of the section of the NVM header (excluding the header checksum itself).

6.4.2. NVM Images

6.4.2.1. Boot ROM Configuration Image

If the NVM image contains an INT6000/INT6300-style SDRAM configuration block, the Mask bits should be set to prevent the INT6400's Boot ROM from loading this field. Native support for configuring the SDRAM controller has been removed from the Boot ROM due to the complexity of providing a complete solution for the memory controller. The memory controller must now be initialized by downloading an SDRAM Configuration applet either through the flash or via the host interface.

6.4.2.2. Image Errors

On any NVRAM image error (CHECKSUM errors, invalid header, etc.) the NVRAM boot will be abandoned and the Boot ROM will start the boot from host process.

Note that if the MinorVersion is set to zero, this indicates to the Boot ROM that the image is a INT6000/INT6300-style image, and as such, is incompatible with the INT6400. If this type of image is detected, the Boot ROM will fail-over to host mode.

Finally, if a NVM descriptor specifies that the corresponding data buffer should be loaded into SDRAM and the SDRAM has not previously been configured, then the Boot ROM will fail-over to host-mode.

6.4.2.3. Skipping Descriptors

The Mask[15:0] is used to specify which versions of the Boot ROM should skip loading the corresponding buffer. If the bit corresponding to the chip is set, then that descriptor should not be loaded by the Boot ROM.

- Bit 0 – INT6000
- Bit 1 – INT6300
- Bit 2 – INT6400
- Bit [15:3] – Reserved

6.4.3. Host Boot

6.4.3.1. Supported Interfaces

The Boot ROM will be capable of booting across the following interfaces:

- MII (MAC Mode)
- MII (PHY Mode)

6.4.3.2. Interface Configuration

These sections describe how the Boot ROM will configure the various host interfaces.

6.4.3.3. MII MAC Mode

When the Boot ROM attempts to configure the MII MAC interface, it will first scan all external MII PHY's starting from PHY #0 and will select the first PHY that responds with valid register contents. The PHY's Link Status register will be read, and if the link is up, auto-negotiation will not be performed. If the PHY's status indicates that auto-negotiation is not supported, auto-negotiation will also not be performed.

Based upon the results of the PHY's status registers, or auto-negotiation results, the PHY will be configured in an operational mode (i.e. no loopback, no collision test, not in isolate, etc.). The MII MAC within the INT6400 will be configured for the same speed and duplex.

6.4.3.4. MII PHY Mode

In MII -PHY mode, auto-negotiation is not supported. Straps on the INT6400 will determine the desired configuration, and these straps will be reflected in the default settings in the MII PHY Emulation registers. The software will read these bits and will configure the MII MAC accordingly.

The Ethernet LEDs will not be enabled while in the Boot ROM.

6.5. Oscillator

6.5.1. Crystal Specifications

Table 28: Crystal Specifications

Frequency	37.500 MHz	Shunt Capacitance	7 pF Max.
Frequency Tolerance @+25°C	± 10 ppm Max.	Mode of Operation	Fundamental
Frequency Stability -10 to +70°C	± 10 ppm Max.	Aging	± 3 ppm/year Max.
Crystal Cut	AT Strip	Storage Temperature	-30 to +85°C
Load Capacitance (CL)	12 pF	Operating Temperature	-10 to +70°C
Recommended Drive Level	650 µW Typ.	Package Type	HC-49/S
Effective Series Resistance	40 ohms Max.	Recommended part	TXC Corp 9B37500028

6.5.2. CMOS Inverter Characteristics

Special consideration must be given to the design of crystal oscillators using the INT6400 internal CMOS oscillator. This is especially true when designing third overtone oscillators where crystal power dissipation and negative resistance at start-up are a few issues to consider. For this reason, Intellon strongly recommends a 37.5 MHz fundamental mode crystal for use with the INT6400.

The CMOS inverter device characteristics are listed below. It is recommended that the customer consult with the crystal manufacturer to ensure a robust oscillator design.

Table 29: CMOS Inverter Device Characteristics

Internal DC feedback resistor	1.2 MΩ ±25%	Input Capacitance	3.0 pF ±25%.
Transconductance	17 mA/V ±20% @ VDD/2	Output Capacitance	3.0 pF ±25%.
Output Impedance	1.6 KΩ ±50% @ VDD/2	Oscillator Duty Cycle	45 to 55% required

6.5.3. PLL Power Filtering

The INT6400 incorporates Phase-Locked Loop (PLL) circuitry that multiplies the master 37.5-MHz system clock in order to generate higher-frequency clocks required for digital processing. The PLL power supply and return are brought out to dedicated pins so external filtering can be applied to minimize system noise coupling into the PLL. It is important to provide the cleanest possible power to the PLL power pins in order to minimize the jitter produced in clocks generated by the PLL. The recommended filter circuit is shown in Figure 16. The capacitors used must be ceramic, X5R or better.

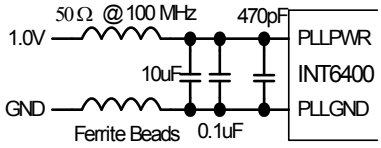


Figure 16: Recommended PLL Power Filtering

6.6. LED Controls

The INT6400 includes a set of four status LED indicators that are available in all interface modes. Connection and function of these LED indicators are described in the following sections.

6.6.1. INT6400 System Status LED Indicators

The system status LED indicators are controlled by routines in the MAC firmware.

Table 30: System Status LEDs

Status LED	INT6400 Signal	Status LED State		
		On	Flash	Off
Power	GPIO[11] LED_PWR	Ready	Load Firmware	Not Ready
Powerline Mode	GPIO[10] LED_PLM/BM_SEL	HomePlug 1.0 Traffic Detected	N/A	Silence
Host/Ethernet Link	GPIO[9] LED_ELNK	Ethernet Link Detected	Transmit or Receive Activity	No Link Detected
Powerline Link	GPIO[8] LED_PLNK/MP_SEL	Powerline Link Detected	See Note Below	Not Detected

Note: The Powerline Link LED indicator turns "ON" when powerline link is detected. If the INT6400 device is serving as a STATION (STA), the LED indicator will flash to indicate transmit or receive powerline activity. If the INT6400 device is serving as a CCO (central coordinator) , the LED indicator will light steadily ON, even in the presence of powerline activity.

The GPIO[8]/MP_SEL, GPIO[9], GPIO[10]/BM_SEL, GPIO[11] are used to determine INT6400 power-up configuration parameters as well as to provide LED status indication. LED indicator connections to these signals (pulled up to 3.3V or pulled down to ground) depend on the power-up parameters chosen. Figure 17 and Figure 18 illustrate how a pull-up or pull-down resistor can be connected to control each LED and provide the appropriate power-up configuration.

Component values in these figures are typical. The value of the series current limiting resistor is selected based on the desired LED current. Note that the maximum LED current must be limited to 12 milliamps.

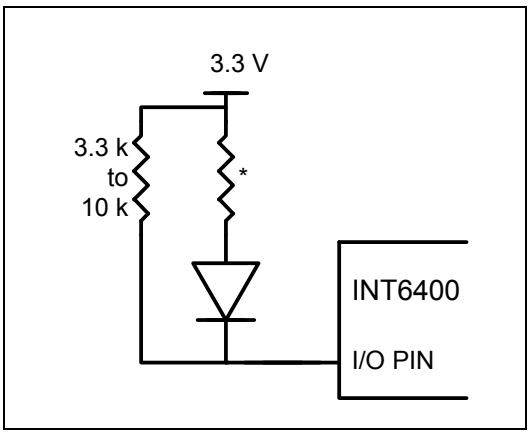


Figure 17: Pull-up LED Strapping

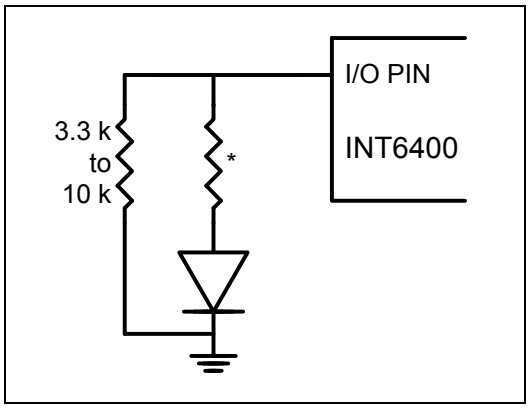


Figure 18: Pull-down LED Strapping

*Select the LED resistor value for the desired LED current.

6.7. Security Pushbutton Configuration

A schematic of the pushbutton circuitry appears in Figure 19 below. The INT6400 GPIO pin (GPIO1/IRQ1) and typical component values are listed in Table 31. R1 serves to pull the GPIO pin to the supply voltage (Logic “1”) when the pushbutton switch is not depressed. When the pushbutton is depressed, the GPIO pin is pulled to ground (Logic “0”) through R2. The INT6400 firmware provides de-bounce and state decode for the pushbutton switch.

Table 31: INT6400 Security Pushbutton GPIO and Component Identification

Component	Value
INT6400 GPIO Pin	GPIO1/IRQ1 – Ball M5 GPIO2 - Ball N5
R1	10 kΩ
R2	100 Ω
C1	100 pF

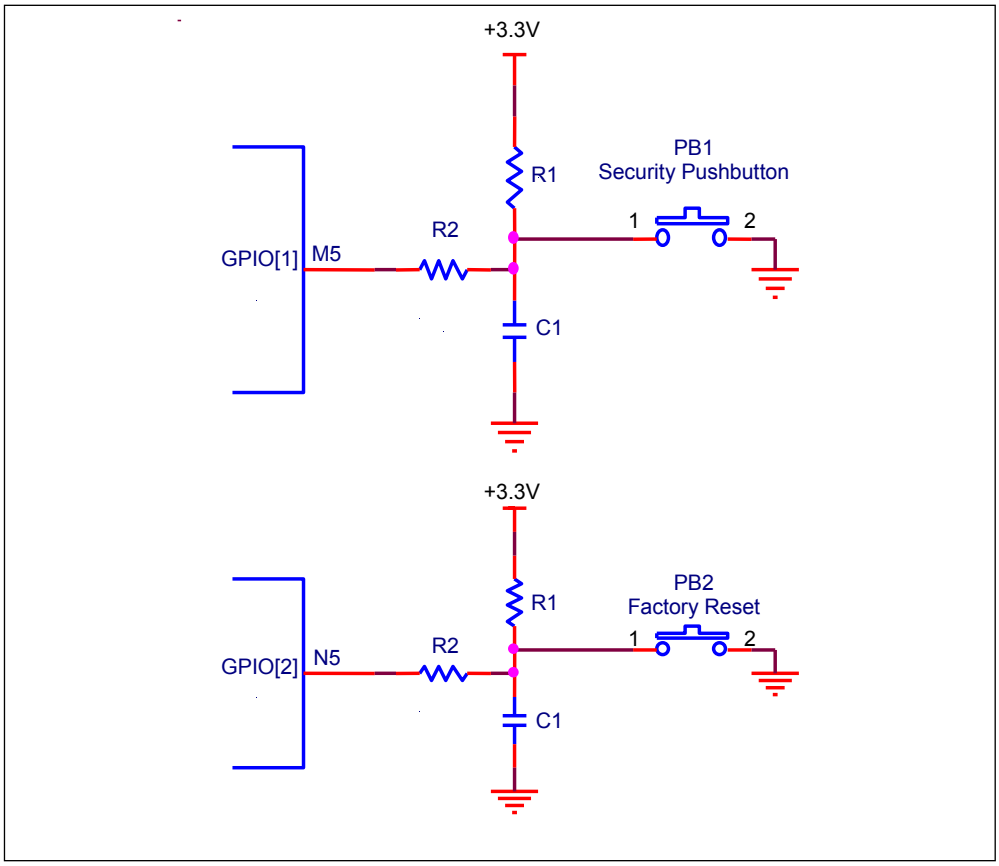


Figure 19: INT6400 Security and Factory Reset Pushbutton Typical Circuits

6.8. Zero-cross Detection

The zero-crossing synchronization circuitry within the INT6400 requires a logic-level pulse on ZC_IN to identify the zero-crossing point. Though not detectable in Figure 20, there is a small and consistent offset that exists between the zero-cross point on the AC waveform and the positive rise of the logic signal. In a practical circuit, as shown in Figure 21, the zero-cross signal will have an offset from the true zero cross. The amount of offset is no concern for the INT6400 as long as the offset for the zero-cross signal occurs consistently between cycles of the AC waveform. Variation of that offset from unit to unit does not matter either.

The zero-cross pulse applied to ZC_IN must be at least 400 µs wide. The positive-going edge of this pulse is used to identify the zero-crossing point. Figure 21 shows the zero-cross detection circuit used in the RD6400-ETH reference design.

NOTE: The power line frequency must be 50Hz ±3.0% or 60Hz ±3.5%. This is required to comply with the HomePlug AV specification. Power line frequencies outside of this range will cause the firmware to reboot the device. For applications which do not meet this criterion, do not use the zero crossing feature. Install 10 k Ohm pullup resistor only. The INT6400 will synthesize a 50 Hz internal clock synchronized to the CCO beacon.

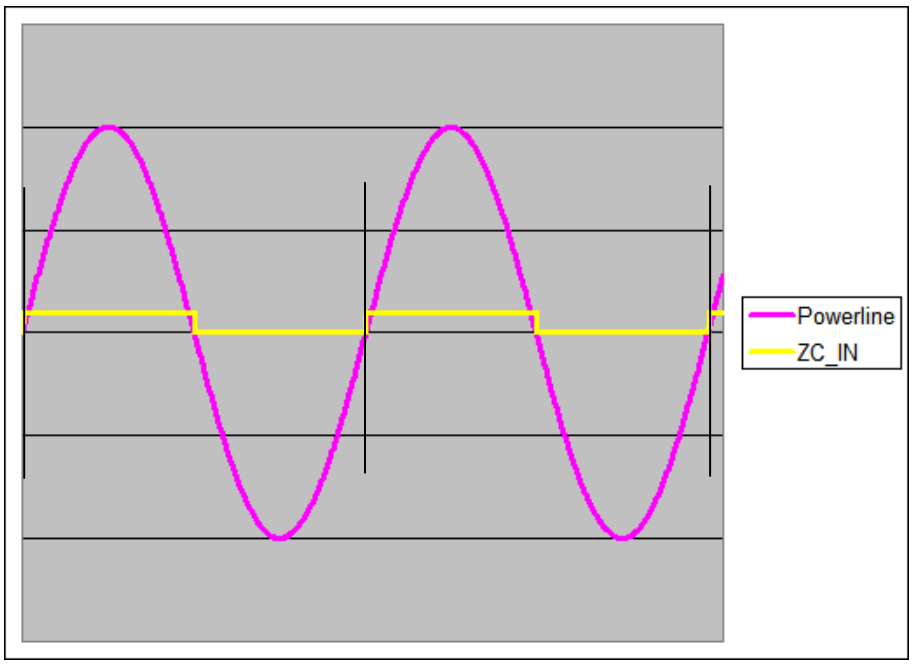


Figure 20: Zero-cross Detection

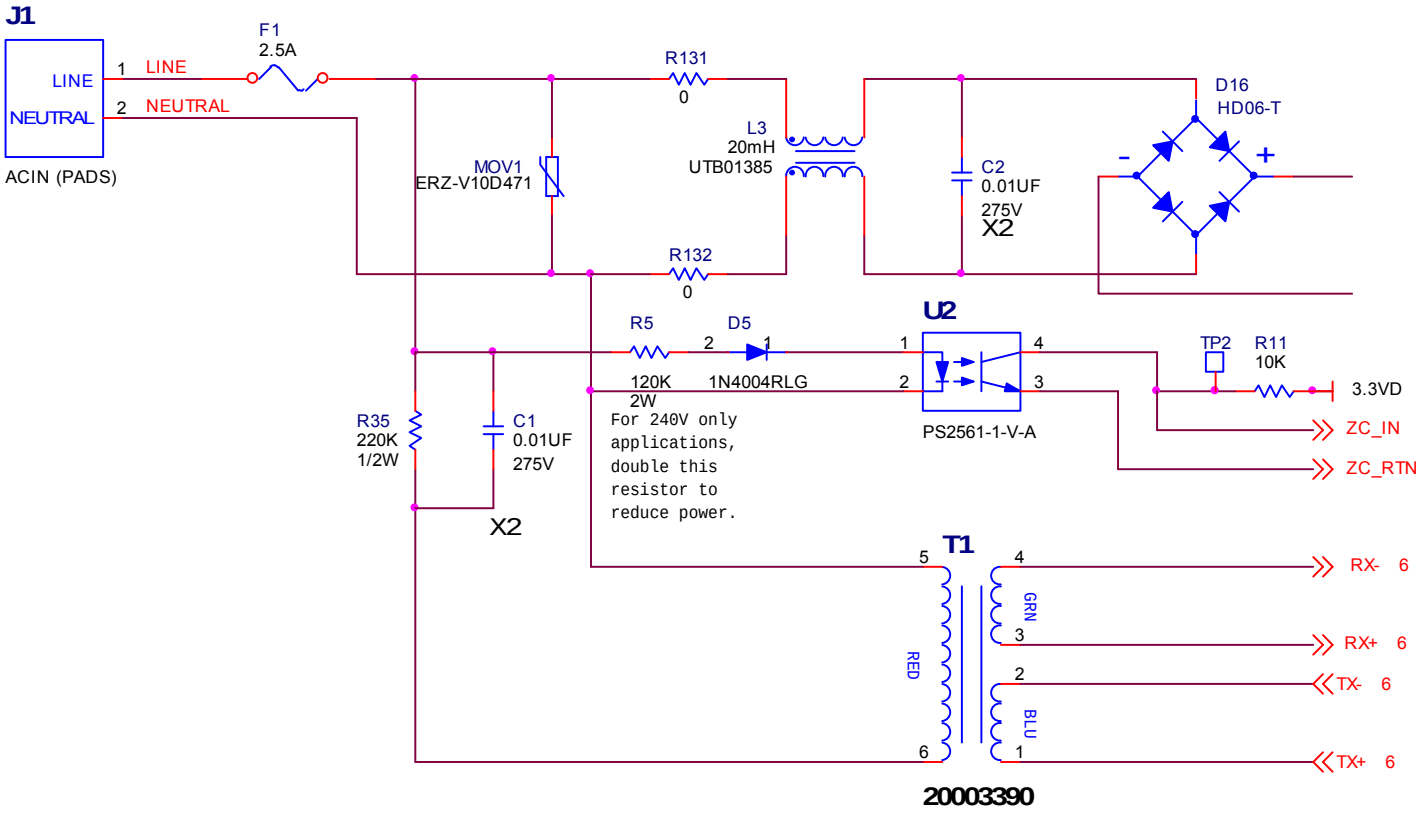


Figure 21: Zero-cross Detection Circuit on AC Line Ahead of PLC Filtering/Coupling

7. Application Considerations

7.1. Packet Classifiers and QoS Parameters

HomePlug AV powerline communications technology is designed to support multimedia and data services with differentiated QoS. The INT6400 uses configurable packet classifiers to define the QoS for powerline traffic. Statically configurable classifiers and QoS parameters are used to simplify integration of Intellon HomePlug AV products with network enabled multimedia products. Equipment manufacturers do not need to integrate QoS management or Application Programming Interface (API) components to take advantage of the advanced HomePlug AV QoS features.

7.1.1. INT6400 Packet Classifiers

The INT6400 manages the QoS for Ethernet-to-Ethernet: Ethernet source device to Ethernet destination device(s).

The INT6400 MAC classification algorithm uses a combination of classifiers and connection rules to manage transmissions between HomePlug AV stations. The Ethernet packet classifier inspects L3 and L2 fields to determine QoS parameters for ingress packets. Universal connection rules provide a mechanism to specify the same level of QoS for all Ethernet ingress traffic through a device and the universal rules determine the QoS for traffic that cannot be categorized by any L3 or L2 Ethernet classifier.

The L3 Ethernet classifiers inspect the protocol type and IP precedence fields in the IP header of ingress packets. The protocol classifier identifies Internet Group Management Protocol (IGMP), Transmission Control Protocol (TCP) and User Datagram Protocol (UDP) packets. A single CSMA priority is defined for all IGMP frames. For TCP and UDP packets, the precedence bits, which are contained in the Type of Service (ToS) field, may be used to set the QoS. The ToS precedence classifier may be enabled or disabled for unicast traffic and multicast Ethernet traffic. All other IP protocols that are not IGMP, UDP or TCP use a common CSMA priority.

The L2 Ethernet classifiers inspect the Ethernet Source Address (SA), Ethernet Destination Address (DA) and Ethernet VLAN (virtual local area network) tag priority of ingress packets. QoS parameters may be defined for all multicast traffic, unicast traffic identified by a specific SA/DA combination and/or the VLAN priority when enabled and present. The INT6400 uses the universal Ethernet connection rules to set QoS parameters when L2 packet classifiers are disabled or the classification algorithm does not match any of the L2 classifiers to fields in the ingress packet.

The equipment manufacturer defines the QoS parameter tables as part of the configuration information loaded at start up and the tables may be loaded and/or updated using MAC MME at run time.

7.1.2. INT6400 Bridging and Classification

The INT6400 inspects Ethernet frames to ensure proper bridging between powerline stations and to manage QoS for Ethernet-to-Ethernet connections. Broadcast packets are transmitted on the powerline in robust mode (ROBO). Multicast packets are transmitted as multiple unicast packets on the powerline. IGMP logic maps multicast DAs to the appropriate unicast DAs based on IGMP messages from devices in the powerline network.

When the INT6400 receives an Ethernet frame, it checks for a valid Ethernet SA/DA bridge address including the local station's Ethernet MAC address in the DA field. It checks the EtherType field of valid frames to determine if the packet is an MME for the local station or a packet to forward over the powerline network. MME message parsing takes precedence.

Ethernet frames with a valid SA/DA that must be bridged pass through to the classification logic. If the frame is not a broadcast packet, an IGMP message, or a multicast packet, the INT6400 attempts to match the SA and/or DA to table entries for Ethernet-to-Ethernet connections. If the logic does not find a valid match for an Ethernet-to-Ethernet connection, it makes decisions based on the universal QoS parameters. If the logic locates an SA/DA match, it makes decisions based on the SA/DA specific QoS parameters. Entries in the match parameters indicate whether or not to inspect the VLAN priority and ToS precedence fields.

If VLAN priority inspection is enabled and the Ethernet frame includes a VLAN tag, the INT6400 transmits the frame using the VLAN connection rules associated with the priority field. If the VLAN priority inspection is disabled or a VLAN tag is not included, the classification logic checks the ToS precedence classifier configuration. If enabled, the classifier uses the ToS precedence connection rules otherwise it uses the QoS parameters for the SA/DA pair to transmit the frame.

The QoS parameters are specific to the type of channel access, CSMA/CA or TDMA. CSMA/CA priority and Time-To-Live (TTL) values apply to packets sent in the CSMA/CA contention period. Stream rate, delay, jitter and no activity timeout values apply to packets sent in the TDMA contention free period. The INT6400 transmits CSMA/CA frames as soon as possible at the access priority specified by the QoS table entry. The INT6400 transmits TDMA frames during the allocated timeslot; it queues ingress packets while the TDMA connection is negotiated and established between stations. If the INT6400 cannot acquire an adequate timeslot to support the TDMA connection, it discards the queued packets and updates the connection status to indicate the failure.

7.1.3. INT6400 QoS Parameters

7.1.3.1. Classifiers and QoS Options

The packet classifiers use several parameters to control and manage the QoS for each connection. CSMA or TDMA QoS parameters may be set. ToS precedence and VLAN priority may be enabled for TCP and UDP traffic for specific SA/DA combinations, Multicast sessions and/or universal connections. IGMP messages and packets that use protocols other than IGMP, TCP or UDP may be sent during the CSMA/CA contention period only. When CSMA/CA is enabled for a particular classifier or connection type, only the CSMA/CA channel access priority (CAP) may include a valid entry; the TDMA-specific entries are not accessible if the channel access is CSMA/CA. If the channel access is TDMA, the TDMA parameters may have valid entries and CSMA/CA parameters are not accessible. Table 32 provides summary of the classifiers and connections type and the corresponding configurable parameters.

Table 32: Summary of Classifiers and Configurable Parameters

Parameters	Classifier or Connection Type						
	IGMP	Default	ToS	VLAN	SA/DA	Multicast	Universal
Source MAC Address	-	-	-	-	X	-	-
Destination MAC Address	-	-	-	-	X	-	-
VLAN Priority	-	-	-	-	X	X	X
TOS Precedence	-	-	-	-	X	X	X
Channel Access Type	-	-	X	X	X	X	X
CSMA/CA Priority	X	X	X	X	X	X	X
TDMA Stream Rate	-	-	X	X	X	X	X
TDMA Maximum Delay	-	-	X	X	X	X	X
TDMA Delay Jitter	-	-	X	X	X	X	X
TDMA Protocol	-	-	X	X	X	X	X
TDMA No Activity Timeout	-		X	X	X	X	X
Encapsulation Header Length	-	-	-	-	-	-	-

IGMP messages are infrequent short control messages that are sent during the CSMA contention period only. All IGMP messages use the same CSMA/CA priority, which is a configurable parameter.

The Default CSMA/CA priority is used to send packets with IP protocols types that are not IGMP, TCP or UDP.

ToS precedence and VLAN priority have eight possible levels and parameters for each of the eight priority levels can be configured. There is one set of eight parameters available for each, and both the ToS precedence and VLAN priority classification can be configured to functional in parallel, with the VLAN priority taking precedence. This allows for 16 possible levels if both the ToS precedence and VLAN priority classification are enabled.

All Multicast sessions use a common set of QoS parameters.

Each SA/DA combination that requires a specific QoS level has a separate set of parameters. The maximum number of SA/DA specific parameters is eight. All others use the Universal QoS parameters.

7.1.3.2. QoS Parameter Descriptions

The programmable parameters are described below and include the valid range of values for each parameter.

Source Address: Ethernet MAC address of the source device.

Destination Address: Ethernet MAC address of the destination device.

VLAN Priority Classifier: Enables (On) and disables (Off) VLAN priority tag classification for the connection. If enabled, directs the classifier to use the attached VLAN tag priority to set the connection & QoS parameters. There are 8 possible VLAN priorities and each priority has a set of QoS parameters.

Type of Service (ToS) Precedence Classifier: Enables (On) and disables (Off) IP Precedence classification for the connection. If enabled, directs the classifier to use the attached ToS field in the IP header to set the connection & QoS parameters. There are 8 possible ToS IP precedence levels and each level has a set of QoS parameters. The VLAN tag inspection has priority when both are enabled.

Channel Access Type: Controls the HomePlug AV channel access method, CSMA/CA or TDMA.

CSMA/CA Priority Level: HomePlug AV CSMA/CA priority level 0-3; implementation specific and may be limited to or mapped to fewer channel access priority levels. The parameter is valid for CSMA/CA channel accesses only.

CSMA/CA Time-to-Live: The time-to-live for CSMA packets is based on global settings, one for each of the four CSMA/CA channel access priorities (CAP0-3).

TDMA Stream Rate: Maximum connection data or stream rate; values range from 1 Kbps to 65,535 Kbps in 1 Kbps steps. The parameter is valid for TDMA channel accesses only.

TDMA Maximum Delay: TDMA latency from sending station to receiving station; values range from 1 μs to 4,294,967,296 μs in 1 μs steps. The parameter is valid for TDMA channel accesses only.

TDMA Delay Jitter: TDMA delay jitter from sending station to receiving station; values range from 1 μs to 4,294,967,296 μs in 1 μs steps. A non-zero value implies smoothing is active and timestamps must be used to ensure the guaranteed delivery time is equal to Fixed Delay +/- Delay Jitter. A value of 0 disables smoothing (timestamp activation) and the delivery time to the receive node will be within the Fixed Delay time. The parameter is valid for TDMA channel accesses only.

TDMA TCP Protocol: Protocol stack – TCP or UDP is valid for all Ethernet-to-Ethernet connections. TCP is connection oriented and may require reverse grant or TDMA allocation in the reverse direction so the destination device has an opportunity to send TCP ACKs to the source device. The parameter is valid for TDMA channel accesses only.

TDMA No Activity Timer Value: Optional no activity timeout timer; when the timer expires, the sending or source station terminates the session. It is most applicable to TDMA connections; expected values range from 1 μs to 4,294,967,296 μs in 1 μs steps. The parameter is valid for TDMA channel accesses only

TDMA Header Length: The nominal value assuming UDP is 42 bytes with a range from 1 to 255 bytes. The parameter is valid for CSMA/CA and TDMA channel accesses.

8. Ethernet Management Registers

The Ethernet Management registers are visible when the chip is configured in Ethernet PHY mode. These registers are accessed by the host through the MDIO (data) and MDC (clock) pins.

8.1. Ethernet PHY Control Register

Register: EPHY_CONTROL **MII Management Address: 0**

Bits	Function							
	7	6	5	4	3	2	1	0
31:24								
23:16								
15:8	RESET	LOOPBACK	SPDSEL	ANEN	PD	ISO	RESTART	DPLX
7:0	COLL							

Register Description

Name	Type	Reset State	Function
RESET	R/W	1	PHY Reset – The external MAC can write this bit, and the ARM can read it and perform the appropriate action to reset the internal logic which is emulating the Ethernet PHY. A write to this register can optionally trigger a full-chip reset, or just an interrupt to the embedded ARM processor.
LOOPBACK	R/W	0	Enables a hardware loopback function using the logic in the Static MII Mux logic. 1'b1 – Loopback enabled 1'b0 – Normal operation
SPDSEL	R/W	SPD100 Pin	Writing this bit has no direct hardware implications. Both the MAC and the ARM have access to this bit, and can read or write it as needed. The bit does have the following standardized meanings. 1'b1 = 100Mbps 1'b0 = 10Mbps
ANEN	R/W	N/A	**The INT6400 does not support Ethernet auto-negotiation in PHY mode. The value of this register is not used by the chip or the firmware.**
PD	R/W	0	Writing this bit has no direct hardware implications. Both the MAC and the ARM have access to this bit, and can read or write it as needed. The bit does have the following standardized meanings. 1'b1 = Power-down 1'b0 = Normal operation
ISO	R/W	ISODEF Pin	1'b1 = electrically isolate the INT6400 from MII 1'b0 = normal operation
RESTART	R/W	0	Writing this bit has no direct hardware implications. Both the MAC and the ARM have access to this bit, and can read or write it as needed. The bit does have the following standardized meanings. 1'b1 = Restart Auto-negotiate 1'b0 = Normal operation
DPLX	R/W	DUPLEX Pin	1'b1 = Full Duplex 1'b0 = Half Duplex
COLL	R/W	0	1'b1 = Force COL high regardless of duplex mode when TX_EN is active 1'b0 = Normal operation

8.2. Ethernet PHY Status Register

Register: EPHY_STATUS **MII Management Address: 1**

Bits	Function							
	7	6	5	4	3	2	1	0
31:24								
23:16								
15:8	100BASE-T4	100BASETX-FD	100BASETX HD	10BASE-T FD	10BASE-T HD			
7:0		PREAMBLE	ANCOMP	RMTFLT	AUTONEG	LINK	JABBER	EXTENDED

Register Description

Name	Type	Reset State	Function
100BASE-T4	R	0	Not Supported
100BASETX-FD	R	Spd100 && duplex	1 = 100FD capable **0 = NOT 100FD CAPABLE**
100BASETX HD	R	Spd100 && !duplex	1 = 100HD capable 0 = not 100HD capable
10BASE-T FD	R	duplex && !spd100	1 = 10 FD capable 0 = not 10 FD capable
10BASE-T HD	R	(!spd100 && !duplex)	1 = 10 HD capable 0 = not 10 HD capable
PREAMBLE	R	0	PHY is not able to perform management transaction w/o MDIO preamble. The management interface needs a minimum of 32 bits of preamble every management frame. **This bit must never be changed.**
ANCOMP	R	0	1 = auto-negotiation complete. Registers 4 and 5 are valid 0 = auto-negotiation not complete
RMTFLT	R	0	1 = Remote Fault 0 = Normal
AUTONEG	R	0	**The INT6400 does not support Ethernet auto-negotiation in PHY mode. The value of this register is not used by the chip or the firmware.**
LINK	R	0	1 = Link up 0 = Link down
JABBER	R	0	1 = Jabber detected 0 = Link down
EXTENDED	R	0	No extended capability. **This bit must never be changed.**

8.3. Ethernet PHY ID1 Register

Register: EPHY_ID1 **MII Management Address: 2**

Bits	Function							
	7	6	5	4	3	2	1	0
31:24								
23:16								
15:8	OUI							
7:0	OUI							

Register Description

Name	Type	Reset State	Function
OUI[15:0]	R	0x2834	3rd through 18th bits of Organizational Unique Identifier (OUI)

8.4. Ethernet PHY ID2 Register

Register: EPHY_ID2 **MII Management Address: 3**

Bits	Function							
	7	6	5	4	3	2	1	0
31:24								
23:16								
15:8	OUI						MODEL	
7:0	MODEL				REVISION			

Register Description

Name	Type	Reset State	Function
OUI[15:10]	R	0	19th through 24th bits of Organizational Unique Identifier (OUI)
MODEL[9:4]	R	001100b	6-bit manufacturer's model number
REVISION[3:0]	R	0010b	4-bit manufacturer's revision number

8.5. Ethernet PHY Auto-negotiate ADV Register

Register: EPHY_AUTONEG_ADV **MII Management Address: 4**

Bits	Function							
	7	6	5	4	3	2	1	0
31:24								
23:16								
15:8	NEXT	ACK				FDFC	100BASE-T4	100BASE-TX FD
7:0	100BASE-TX HD	10BASE-T FD	10BASE-T HD	SELECTOR				

Register Description

Name	Type	Reset State	Function
NEXT	R	0	Not Supported **Always read only by external MAC.**
ACK	R	0	1 = "3 FLP bursts received" 0 = not received **Always read only by external MAC.**
FDFC	R/W	0	1 = External MAC Full duplex Flow control supported 0 = External MAC Full duplex Flow control not supported
100BASE-T4	R	0	Not supported **Always read only by external MAC.**
100BASE-TX FD	R/W	Spd100 && duplex	1 = 100FD capable 0 = not 100FD capable
100BASE-TX HD	R/W	Spd100 && !duplex	1 = 100HD capable 0 = not 100HD capable
10BASE-T FD	R/W	duplex && !spd100	1 = 10 FD capable 0 = not 10 FD capable
10BASE-T HD	R/W	(!spd100 && !duplex)	1 = 10 HD capable 0 = not 10 HD capable
Selector Field	R	00001	Protocol Select 00001 = 802.3 **Always read only by external MAC.**

- Speed/Duplex Mode determined at reset by STRAP pins
- External MAC can override and restart auto-negotiation via control bit R0.12.
- Bits 4.15, 4.[13:11], 4.[4:0] should not be changed by ARM from default values.
- After reset, MAC may change Bits 4.[8:5] from 1 to 0 and back to 1, but not from 0 to1. Therefore, the hardware has priority over software.

8.6. Ethernet PHY Auto-negotiate Link Register

Register: EPHY_AUTONEG_LINK **MII Management Address: 5**

Bits	Function							
	7	6	5	4	3	2	1	0
31:24								
23:16								
15:8	NEXT	ACK					100BASE-T4	100BASE-TX FD
7:0	100BASE-TX HD	10BASE-T FD	10BASE-T HD	SELECTOR				

Register Description

Name	Type	Reset State	Function
NEXT	R	0	Not Supported
ACK	R	0	1 = “Link partner: 3 FLP bursts received” 0 = not received
100BASE-T4	R	0	Link Partner Not supported
100BASE-TX FD	R	0	Link Partner 1 = 100FD capable 0 = not 100FD capable
100BASE-TX HD	R	0	Link Partner 1 = 100HD capable 0 = not 100HD capable
10BASE-T FD	R	0	Link Partner 1 = 10 FD capable 0 = not 10 FD capable
10BASE-T HD	R	0	Link Partner 1 = 10 HD capable 0 = not 10 HD capable
Selector Field	R	00001	Link Partner Protocol Select 00001 = 802.3

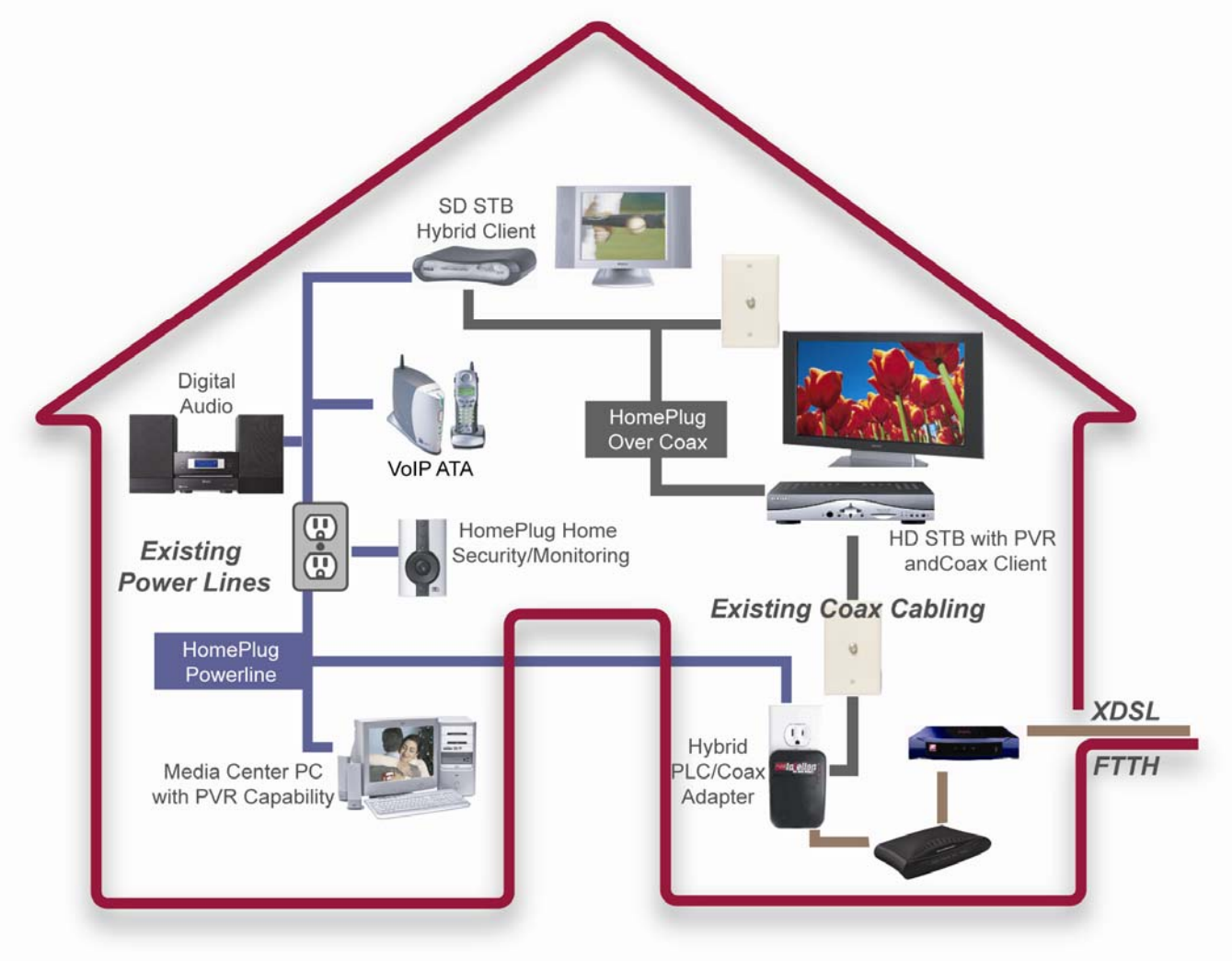
- If external MAC restarts auto-neg, then hardware will update this register
- If external MAC restarts auto-neg, then ARM S/W may override this register
- After reset, Bits 5.15, 5.[13:10], 5.[4:0] will be updated by ARM from default values to reflect “link partner” capabilities based on network conditions, etc.

9. Revision History

Table 33: Revision History

Revision	Modifications
1	Original Issue – Preliminary Hardware-only Version
2	Section 4.4 updated Ball table Section 3.1 updated entire section Figure 4 Replaced schematic
3	Section 1.2.6 ESD Immunity Section 2.3 and Table 1 SDRAM speed Figure 12 ball ID callouts Figure 21 transient protection location
4	Section 2.3 Corrected SDRAM information; Removed Section 7.2 SDRAM Requirements Section 1.2.7: Revised chip typical power requirements – based on actual measurements
5	Section 2.3 SDRAM Interface,updated Table 3 with Etron data. Section 6.4 Supported NVMs, updated Table 25 with new flash data.

10. Disclaimer



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