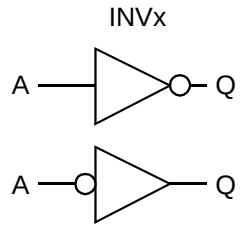
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

INVx is a family of inverters which perform the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

HDL Syntax

Verilog ..... INVx *inst_name* (Q, A);

VHDL..... *inst_name*: INVx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads					
	INV1	INV2	INV3	INV4	INV5	INV6
A	1.0	2.1	3.2	4.2	5.2	6.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
INV1	1.0	TBD	0.6
INV2	1.0	TBD	0.6
INV3	2.0	TBD	1.2
INV4	2.0	TBD	1.2
INV5	3.0	TBD	1.8
INV6	3.0	TBD	1.8

a. See page 2-15 power equation

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

INV1	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.03 0.12	0.16 0.22	0.29 0.33	0.44 0.45	0.55 0.55
INV2	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.08 0.09	0.20 0.23	0.30 0.33	0.39 0.42	0.49 0.54
INV3	**Number of Equivalent Loads**		**1**	**11**	**22**	**32**	**43 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.04 0.08	0.18 0.22	0.28 0.33	0.37 0.41	0.46 0.49
INV4	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.05 0.08	0.16 0.20	0.26 0.31	0.34 0.41	0.41 0.50
INV5	**Number of Equivalent Loads**		**1**	**18**	**35**	**52**	**70 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.03 0.05	0.17 0.19	0.26 0.30	0.32 0.39	0.38 0.49
INV6	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.06 0.10	0.14 0.19	0.23 0.30	0.33 0.38	0.41 0.46

Delay will vary with input conditions. See page 2-17 for interconnect estimates.