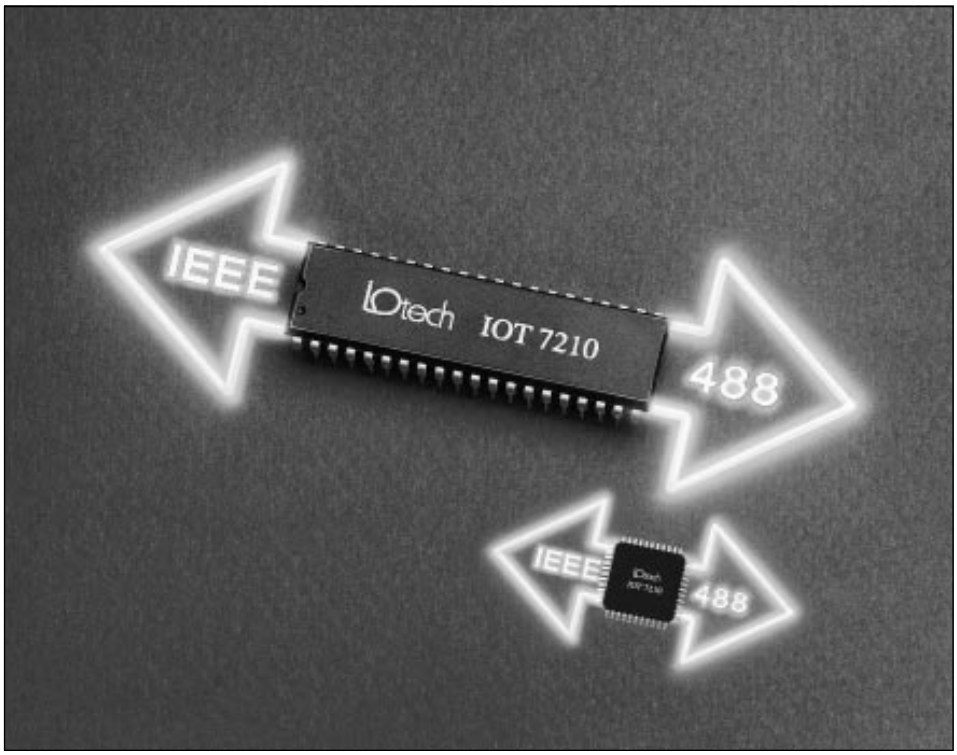
IOT7210

Low-Power CMOS IEEE 488 Controller Device

NEW

Features

- **Completely meets IEEE Standard 488-1978:**
  - **SH1, source handshake**
  - **AH1, acceptor handshake**
  - **T5 or TE5, talker or extended talker**
  - **L3 or LE3, listener or extended listener**
  - **SR1, service request**
  - **RL1, remote local**
  - **PP1 or PP2, parallel poll, remote, or local configuration**
  - **DC1, device clear**
  - **DT1, device trigger**
  - **C1-C5, controller, all functions**
- **Programmable data transfer rate**
- **16 registers, 8 read/8 write**
- **2 address registers: detect MTA, MLA, MSA (my talk/my listen/my secondary addresses) and provide 2 device addresses**
- **End-of-string (EOS) message automatic detection**
- **Automatic (IEEE Standard 488-78) command processing and undefined command read capability**
- **DMA-capable**
- **Programmable bus transceiver I/O specification, Texas Instruments/ Motorola/Intel-compatible**
- **1 MHz to 8 MHz clock range**
- **TTL-compatible**
- **CMOS**
- **+5V single power supply**
- **40-pin plastic DIP or 44-pin plastic TQFP**
- **8080/85/86-compatible**



The IOT7210 is an enhanced replacement for the NEC µPD7210 IEEE 488 controller device

The IOT7210 low-power CMOS intelligent IEEE 488 controller meets all the functional requirements for talkers, listeners, and controllers as specified by the IEEE Standard 488-1978. It completely duplicates the NEC µPD7210's function and provides enhancements such as lower power consumption and increased speed. Fully compatible with most processor architectures, the IOT7210 requires only the addition of the bus driver/receiver components to implement any IEEE 488 interface.

In its 40-pin plastic DIP package, the IOT7210 provides users with a drop-in replacement for the µPD7210 and eliminates the need for either software or hardware modifications. It is also available in a 44-pin, 1.27 mm thick plastic TQFP package for surface-mount applications.

IOT7210 Operation on the IEEE 488 Bus

Since its introduction in the 1970s, the IEEE 488 standard has become the most popular means of interconnecting instruments and controllers. This highly sophisticated standard has been refined over the years to provide a great degree of flexibility, permitting it to meet most instrumentation requirements.

The IEEE 488 bus uses a common set of data and control lines to interconnect up to 15 devices. The device's capabilities are classified as a combination of talker, listener, and/or controller. Devices that incorporate the IOT7210 can perform all three functions—talker, listener, and controller.

Data is transferred on the IEEE 488 bus in a bit-parallel, byte-serial fashion over eight bidirectional data lines. A 3-wire handshake ensures synchronization of transmission and reception and allows more than one device to receive data at the same time, with the slowest device controlling the data rate. Other control lines perform a variety of functions, such as device addressing and interrupt generation. In addition to providing all the control and data lines necessary for IEEE 488 operation, the IOT7210 provides a flexible interface to the standard IEEE 488 transceivers.

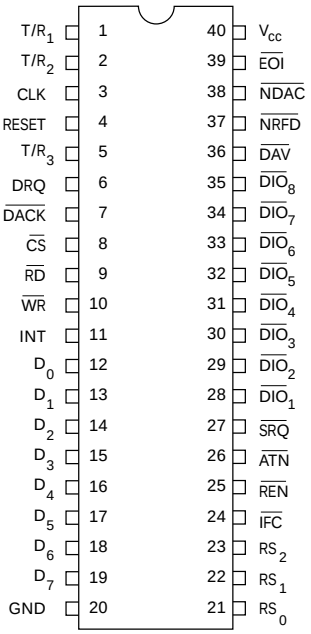
The IOT7210 implements all the functions (including timing) that are required to interface to the IEEE 488 bus and provides high-level bus protocol management, which frees the host processor for other tasks. By performing these functions in dedicated hardware, the IOT7210 ensures bus compatibility with other IEEE 488 devices.

The IOT7210 is controlled by its 16 internal registers. To reduce CPU overhead, bus data bytes can be transferred to and from the IOT7210 using DMA. The IOT7210's DMA feature is generic enough that it can be used to interface to most processors and buses.

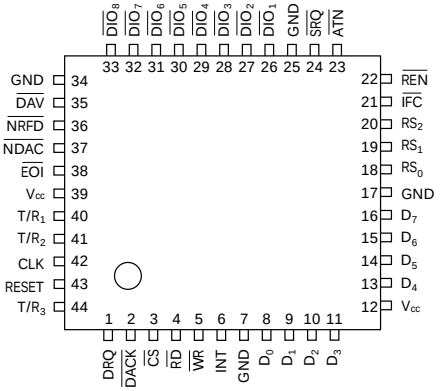
Pin Configurations

Pin No. DIP	Pin No. (TQFP)	Symbol	I/O	Functions
1	(40)	T/R_1	O	*Transmit/Receive Control.* Input/output control signal for the IEEE 488 bus transceivers.
2	(41)	T/R_2	O	*Transmit/Receive Control.* The values of TRM1and TRM0 of the address mode register control the functions of T/R_2 and T/R_3.
3	(42)	CLK	I	*Clock.* 1 MHz to 8 MHz reference clock for generating the state change prohibit times T_1, T_6, T_7, T_8, specified in IEEE Standard 488-1978.
4	(43)	RESET	I	*Reset.* Resets the IOT7210 to an idle state when high (active high).
5	(44)	T/R_3	O	*Transmit/Receive Control.* See T/R_2.
6	(1)	DRQ	O	*DMA Request.* Requests data transfer. Becomes low on input of DMA acknowledge signal DACK.
7	(2)	$\overline{DACK}$	I	*DMA Acknowledge.* Active low. Connects the data bus (D_0 - D_7) to the byte in or data out register of the IOT7210.
8	(3)	$\overline{CS}$	I	*Chip Select.* Active low. Enables access to the register selected by RS_0 - RS_2 (read or write operation).
9	(4)	$\overline{RD}$	I	*Read.* Active low. Places contents of read register specified RS_0 - RS_2 on D_0 - D_7 (computer bus).
10	(5)	$\overline{WR}$	I	*Write.* Active low. Writes data on D_0 - D_7 into the write register specified by RS_0 - RS_2.
11	(6)	INT, $\overline{INT}$	O	*Interrupt Request.* Active high/low. Becomes active due to any 1 of 13 internal interrupt conditions (unmasked). Active state software configurable. Active high on chip reset.
12-19	(8-11, 13-16)	D_0 - D_7	I/O	*Data Bus.* 8-bit bidirectional data bus for interface to the computer system.
20	(7, 17, 25, 34)	GND		*Ground.*
21-23	(18-20)	RS_0 - RS_2	I	*Register Select.* Select one of eight read (write) registers during a read (write) operation.
24	(21)	$\overline{IFC}$	I/O	*Interface Clear.* IEEE 488 control line. Clears the interface functions.
25	(22)	$\overline{REN}$	I/O	*Remote Enable.* IEEE 488 control line. Selects remote or local control of the devices.
26	(23)	$\overline{ATN}$	I/O	*Attention.* IEEE 488 control line. Indicates whether data on DIO lines is an interface message or device dependent message.
27	(24)	$\overline{SRQ}$	I/O	*Service Request.* IEEE 488 control line. Requests the service from the controller.
28-35	(26-33)	$\overline{DIO_1}$ - $\overline{DIO_8}$	I/O	*Data Input/Output.* IEEE 488 8-bit bi-directional bus for transfer of message.
36	(35)	$\overline{DAV}$	I/O	*Data Valid.* IEEE 488 handshake line. Indicates that data on DIO lines is valid.
37	(36)	$\overline{NRFD}$	I/O	*Ready for Data.* IEEE 488 handshake line. Indicates that device is ready for data.
38	(37)	$\overline{NDAC}$	I/O	*Data Accepted.* IEEE 488 handshake line. Indicates completion of message reception.
39	(38)	$\overline{EOI}$	I/O	*End or Identify.* IEEE 488 control line. Indicates the end of multiple byte transfer sequence or signals a parallel poll in conjunction with ATN.
40	(12, 39)	V_{CC}	I/O	+5V DC.

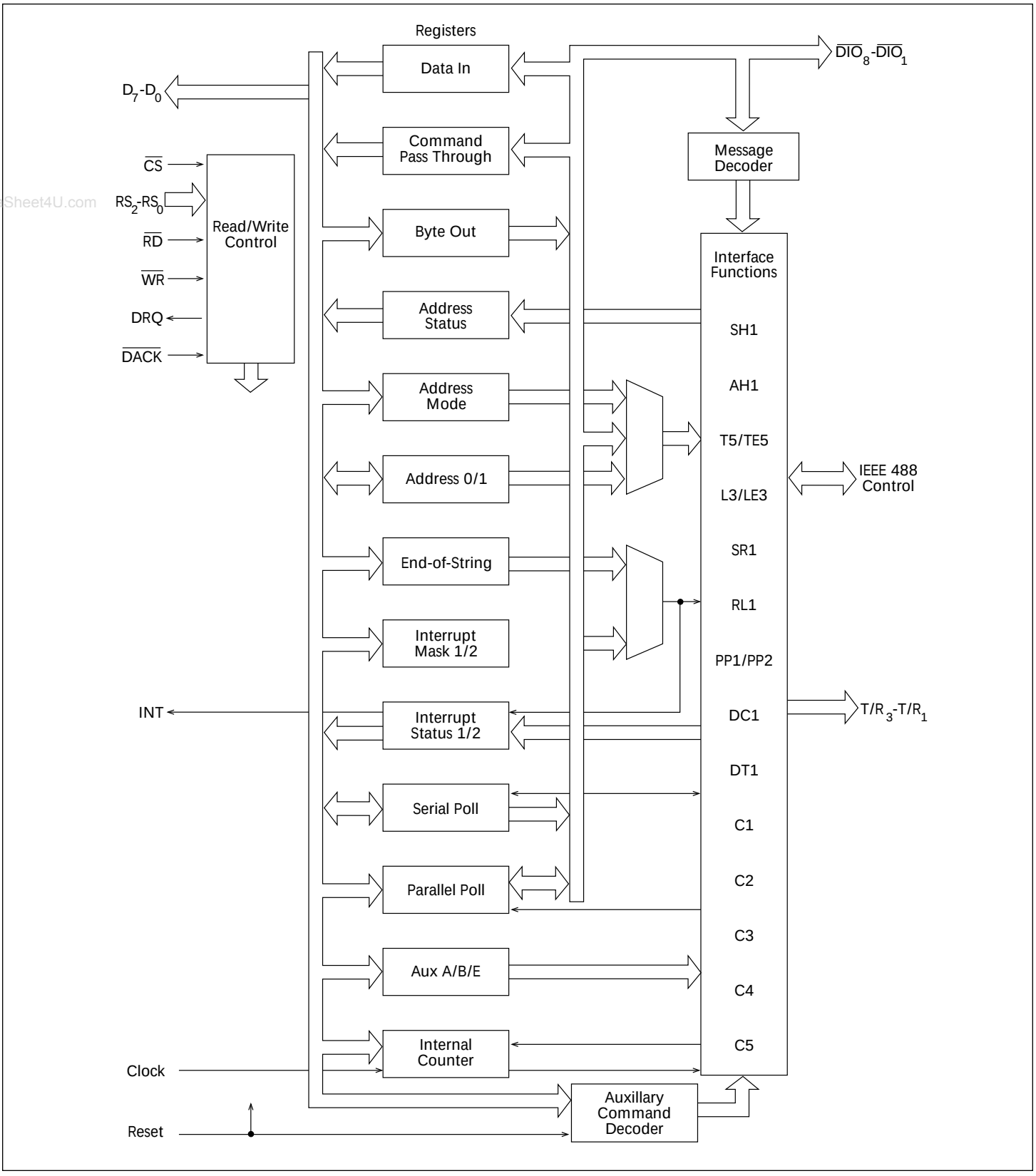
IOT7210P



IOT7210T



Functional Block Diagram



Electrical Characteristics

Absolute Maximum Ratings

Exposing the device to stresses above those listed here could cause permanent damage to the IOT7210. The device is not meant to be operated under conditions outside the limits described in this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T_A = 25C	
Supply Voltage, V_{cc}	-0.3V to +7.0V
Input Voltage, V_I	-0.3V to V_{cc} +0.3V
Output Voltage, V_o	-0.3V to V_{cc} +0.3V
Operating Temperature, T_{OPR}	0C to +70C
Storage Temperature, T_{STG}	-55C to 125C

Capacitance

T_A = 25C; V_{CC} = GND = 0V				
Symbol	**Min**	**Max**	**Unit**	**Test Conditions**
C_{IN}		15	pF	F = 1 MHz
C_{OUT}		15	pF	All pins except pin under test tied to AC ground
$C_{I/O}$		15	pF	

AC/DC Characteristics

AC Characteristics

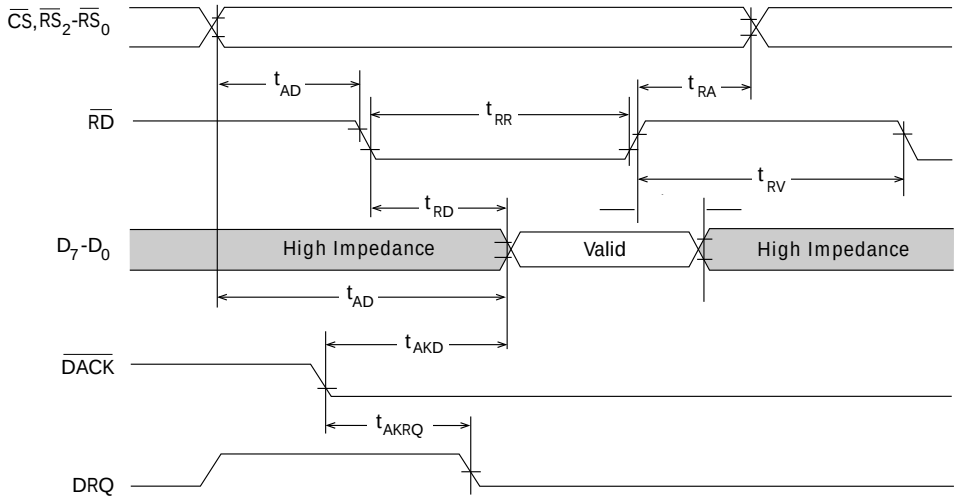
T_A = 0C to 70C; V_{cc} = 5V ± 10%					
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{EOI}\downarrow \rightarrow$ DIO	t_{EODI}		35	ns	PPSS → PPAS, ATN = True
$\overline{EOI}\downarrow \rightarrow T/R_1\uparrow$	t_{EOTI1}		20	ns	PPSS → PPAS, ATN = True
$\overline{EOI}\uparrow \rightarrow T/R_1\downarrow$	t_{EOTI2}		25	ns	PPAS → PPSS, ATN = False
$\overline{ATN}\downarrow \rightarrow \overline{NDAC}\downarrow$	t_{ATN0}		35	ns	AIDS → ANRS, LIDS
$\overline{ATN}\downarrow \rightarrow T/R_1\downarrow$	t_{ATT1}		30	ns	TACS + SPAS → TADS, CIDS
$\overline{ATN}\downarrow \rightarrow T/R_2\downarrow$	t_{ATT2}		30	ns	TACS + SPAS → TADS, CIDS
$\overline{DAV}\downarrow \rightarrow DRQ\uparrow$	t_{DVRQ}		25	ns	ACRS → ACDS, LACS
$\overline{DAV}\downarrow \rightarrow \overline{NRFD}\downarrow$	t_{DVNR1}		30	ns	ACRS → ACDS
$\overline{DAV}\downarrow \rightarrow \overline{NDAC}\uparrow$	t_{DVND1}		40	ns	ACRS → ACDS → AWNS
$\overline{DAV}\uparrow \rightarrow \overline{NDAC}\downarrow$	t_{DVND2}		45	ns	AWNS → ANRS
$\overline{DAV}\uparrow \rightarrow \overline{NRFD}\uparrow$	t_{DVNR2}		35	ns	AWNS → ANRS → ACRS
$\overline{RD}\uparrow \rightarrow \overline{NRFD}\uparrow$	t_{RNR}		30	ns	ANRS → ACRS → LACS, DI register selected
$\overline{NDAC}\uparrow \rightarrow DRQ\uparrow$	t_{NDRQ}		25	ns	STRS → SWNS → SGNS, TACS
$\overline{NDAC}\uparrow \rightarrow \overline{DAV}\uparrow$	t_{NDDV}		25	ns	STRS → SWNS → SGNS
$\overline{WR}\uparrow \rightarrow \overline{DIO}$	t_{WDI}		30	ns	SGNS → SDYS BO register selected
$\overline{NRFD}\uparrow \rightarrow \overline{DAV}\downarrow$	t_{NRDV}		30	ns	SDYS → STRS, T_1 = True
$\overline{WR}\uparrow \rightarrow \overline{DAV}\downarrow$	t_{WDV}		550 +t_{SYNC}	ns	SGNS → SDYS → STRS BO register selected; RFD = True; N + fc = 8MHz; T_1 (high speed)
TRIG Pulse Width	t_{TRIG}	50		ns	
Address Setup to $\overline{RD}$	t_{AR}	0		ns	RS_0 to RS_2
		0		ns	$\overline{CS}$
Address Hold from RD	t_{RA}	0		ns	
RD Pulse Width	t_{RR}	55		ns	
Data Delay from Address	t_{AD}		35	ns	
Data Delay from RD ↓	t_{RD}		35	ns	
Output Float Delay from $\overline{RD}\uparrow$	t_{DF}	0	10	ns	
$\overline{RD}$ Recovery Time	t_{RV}	50		ns	
Address Setup to $\overline{WR}$	t_{AW}	0		ns	
Address Hold from WR	t_{WA}	0		ns	
WR Pulse Width	t_{WW}	55		ns	
Data Setup to $\overline{WR}$	t_{DW}	10		ns	
Data Hold from $\overline{WR}$	t_{WD}	0		ns	
$\overline{WR}$ Recovery Time	t_{RV}	50		ns	
DRQ ↓ Delay from $\overline{DACK}\downarrow$	t_{AKRQ}		25	ns	
Data Delay from $\overline{DACK}$	t_{AKD}		35	ns	
$\overline{DACK}$ hold time from $\overline{WR}\uparrow$	t_{DH}	5		ns	

DC Characteristics

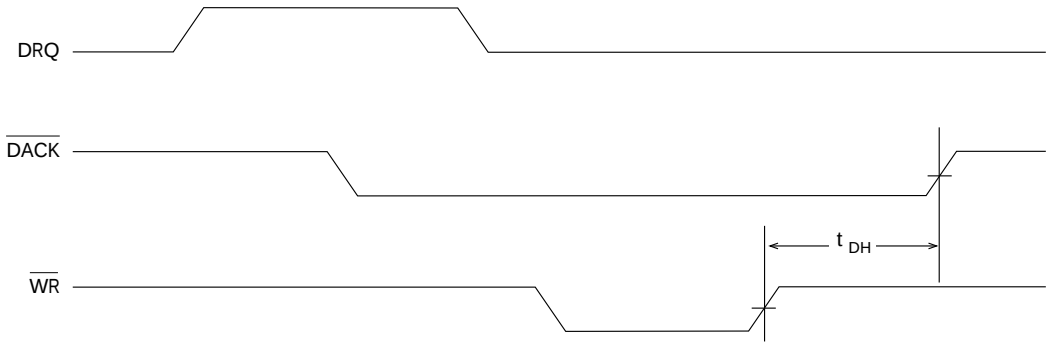
T_A = 0C to 70C; V_{cc} = 5V ± 10%					
Input Low Voltage (except RESET)	V_{IL}	-0.3	+.08	V	
Input High Voltage (except RESET)	V_{IH}	+2.0	V_{CC} +0.3	V	
Input Low Voltage (RESET)	-0.3	0.7	V		
Input High Voltage (RESET)	+2.1	V_{CC} +0.3	V		
Low-Level Output Voltage	V_{OL}		+0.4	V	
High-Level Output Voltage (except INT)	V_{OH1}	+2.4		V	I_{OH} = 1mA
High-Level Output Voltage (INT)	V_{OH2}	+2.4		V	I_{OH} = 1mA
		+3.5		V	I_{OH} = 50 µA
Input Leakage Current	I_{IL}	-1	+1	µA	V_{IN} = 0V to V_{CC}
Output Leakage Current	I_{OL}	-10	+10	µA	V_{OUT} = 0 to V_{CC}
Supply Current	I_{CC}		2	mA	Outputs Open

Timing Waveforms

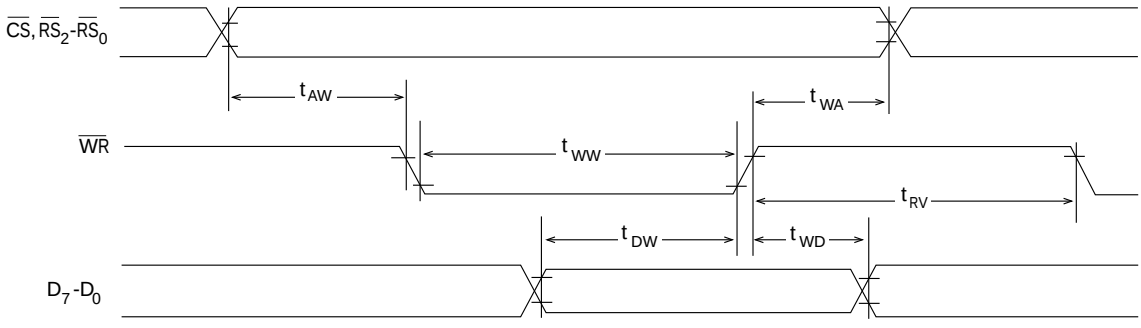
CPU / DMA Read



DMA Write Timing



CPU Write Timing



Registers

Internal Registers

The IOT7210 has 16 registers: 8 read and 8 write.

Register Name	Addressing						Specification							
	RS2	RS1	RS0	$\overline{W}$R	$\overline{R}$D	$\overline{C}$S								
Data In [0R]	0	0	0	1	0	0	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Interrupt Status 1 [1R]	0	0	1	1	0	0	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Status 2 [2R]	0	1	0	1	0	0	INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC
Serial Poll Status [3R]	0	1	1	1	0	0	S8	PEND	S6	S5	S4	S3	S2	S1
Address Status [4R]	1	0	0	1	0	0	CIC	$\overline{ATN}$	SPMS	LPAS	TPAS	LA	TA	MJMN
Command Pass Through [5R]	1	0	1	1	0	0	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0
Address 0 [6R]	1	1	0	1	0	0	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
Address 1 [7R]	1	1	1	1	0	0	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
Byte Out [0W]	0	0	0	0	1	0	BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0
Interrupt Mask 1 [1W]	0	0	1	0	1	0	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Mask 2 [2W]	0	1	0	0	1	0	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC
Serial Poll Mode [3W]	0	1	1	0	1	0	S8	rsv	S6	S5	S4	S3	S2	S1
Address Mode [4W]	1	0	0	0	1	0	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0
Auxiliary Mode [5W]	1	0	1	0	1	0	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0
Address 0/1 [6W]	1	1	0	0	1	0	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
End of String [7W]	1	1	1	0	1	0	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Data Registers

The data registers are used for data and command transfers between the IEEE 488 and the computer. The Data In register holds data sent from the IEEE 488 to the computer; the Byte Out register holds information written into it for transfer to the IEEE 488 bus.

Data In [0R]

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Byte Out [0W]

BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0

Interrupt Registers

The interrupt registers consist of interrupt status bits, interrupt mask bits, and some other non-interrupt bits.

Read

Interrupt Status 1 [1R]

CPT	APT	DET	END	DEC	ERR	DO	DI

Interrupt Status 2 [2R]

INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC

Write

Interrupt Mask 1 [1W]

CPT	APT	DET	END	DEC	ERR	DO	DI

Interrupt Mask 2 [2W]

0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC

Thirteen factors can generate an interrupt from the IOT7210, each with its own status bit and mask bit.

The interrupt status bits are always set to 1 if the interrupt condition is met. The interrupt mask bits decide whether or not the INT bit and the interrupt pin will be active for that condition.

Interrupt Status Bits

INT	OR of All Unmasked Interrupt Status Bits
CPT	Command Pass Through
APT	Address Pass Through
DET	Device Trigger
END	End (END or EOS Message Received)
DEC	Device Clear
ERR	Error
DO	Data Out
DI	Data In
SRQI	Service Request Input
LOKC	Lockout Change
REMC	Remote Change
ADSC	Address Status Change
CO	Command Output

Noninterrupt Related Bits

LOK	Lockout
REM	Remote/Local
DMAO	Enable/Disable DMA Out
DMAI	Enable/Disable DMA In

Serial Poll Registers

The serial poll mode register holds the STB (status byte: S8, S6-S1) sent over the IEEE 488 bus and the local message rsv (request service). The serial poll mode register may be read through the serial poll status register. The PEND is set by rsv = 1 and cleared by NPRS•$\overline{rsv}$ = 1 (NPRS = negative poll response state).

Read

Serial Poll Status [3R]

S8	PEND	S6	S5	S4	S3	S2	S1

Write

Serial Poll Mode [3W]

S8	rsv	S6	S5	S4	S3	S2	S1

Registers

Address Status/Address Mode Registers

The address mode register selects the address mode of the device and also sets the mode for the transceiver control lines, T/R_3 and T/R_2.

Address Status [4R]

CIC	ATN	SPMS	LPAS	TPAS	LA	TA	MJMN

Address Mode [4W]

ton	lon	TRM1	TRM0	0	0	AMD1	ADM0

The TRM1 and TRM0 values of the address mode register determine the functions of the T/R_2 and T/R_3 pins.

T/R_2	T/R_3	TRM1	TRM0
EOIOE	TRIG	0	0
CIC	TRIG	0	1
CIC	EOIOE	1	0
CIC	PE	1	1

EOIOE = TACS + SPAS + CIC • $\overline{CSBS}$
EOI pin output enable.
When 1: output
When 0: input

CIC = $\overline{CIDS + CADS}$
Controller in charge.
When 1: $\overline{ATN}$ = output, $\overline{SRQ}$ = input
When 0: $\overline{ATN}$ = input, $\overline{SRQ}$ = output

PE = CIC + PPAS
Pull-up enable for DIO_8 - DIO_1 and DAV lines.
When 1: Three-state
When 0: Open-collector

TRIG
Pulses high when DTAS state is initiated or when a trigger auxiliary command is issued.

Upon reset, TRM0 and TRM1 become 0 (TRM0 = TRM1 = 0) so that T/R_2 and T/R_3 both become low.

Address Status Bits

$\overline{ATN}$	Data Transfer Cycle (Device in CSBS)
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
CIC	Controller Active
LA	Listener Addressed
TA	Talker Addressed
MJMN	Set = Minor T/L Address, Reset = Major T/L Address
SPMS	Serial Poll Mode State

Address Modes

ton	lon	ADM1	ADM0	Address Mode	Contents of Address 0 Register	Contents of Address 1 Register
1	0	0	0	Talk only mode	Address identification necessary (no controller on the IEEE 488 bus)	
0	1	0	0	Listen only mode	Not used	
0	0	0	1	Address mode 1[1]	Major talk address or major listen address	Minor talk address or minor listen address
0	0	1	0	Address mode 2[2]	Primary address (talk or listen)	Secondary address (talk or listen)
0	0	1	1	Address mode 3[3]	Primary address (major talk or major listen)	Primary address (minor talk or minor listen)

Notes: Combinations other than those indicated are prohibited.
1 Either MTA or MLA reception is indicated by coincidence of either address with the received address; interface function T or L
2 Address register 0 = primary: address register 1 = secondary; interface function TE or LE
3 CPU must read secondary address via Command Pass Through register; interface function (TE or LE)

Address Registers

The IOT7210 is able to automatically detect two addresses that are held in address registers 0 and 1, as specified by the address mode register.

Address 0 [6R]

X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0

Address 1 [7R]

EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1

Address 0/1 [6W]

ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

The addresses are set by writing into the address 0/1 register.

Address 0/1 Register Bit Selections

ARS	Selects either address register 0 or 1
DT	Permits or prohibits address to be detected as Talk
DL	Permits or prohibits address to be detected as Listen
AD_5-AD_1	Device address value
EOI	Holds the value of EOI line when data is received

Command Pass Through Register

The CPT register enables the CPU to read the DIO lines in the cases of undefined command, secondary address, or parallel poll response.

Command Pass Through [5R]

CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

Registers

End of String Register

This register holds either a 7- or 8- bit EOS message byte used in the IEEE 488 system to detect the end of a data block. Auxiliary Mode register A controls the specific use of this register.

End of String [7W]

EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Auxiliary Mode Register

This is a multipurpose register.

Auxiliary Mode [5W]

CNT2	CNT1	CNT0	COM4	C0M3	COM2	COM1	COM0

A write to this register generates one of the following operations according to the values of the CNT bits.

CNT			COM					Function
2	1	0	4	3	2	1	0	
0	0	0	C_4	C_3	C_2	C_1	C_0	Issues an auxiliary command specified by C_4 to C_0
0	0	1	0	F_3	F_2	F_1	F_0	The reference clock frequency determines T_1, T_6, T_7, & T_9
0	1	1	U	S	P_3	P_2	P_1	Sets the parallel poll register
1	0	0	A_4	A_3	A_2	A_1	A_0	Sets the auxiliary A register
1	0	1	B_4	B_3	B_2	B_1	B_0	Sets the auxiliary B register
1	1	0	0	0	0	E_1	E_0	Sets the auxiliary E register

Auxiliary Commands

Auxiliary Commands

0	0	0	C_4	C_3	C_2	C_1	C_0

Command C_4	C_3	C_2	C_1	C_0	Aux Comm	Function
0	0	0	0	0	iepon	Immediate Execute pon, Generate Local pon message
0	0	0	1	0	crst	Chip Reset (Same as External Reset)
0	0	0	1	1	rrfd	Release RFD
0	0	1	0	0	trig	Trigger
0	0	1	0	1	rtl	Return to Local
0	0	1	1	0	seoi	Send EOI message
0	0	1	1	1	nvld	Nonvalid (OSA Reception), Release DAC Holdoff
0	1	1	1	1	vld	Valid (MSA Reception, CPT, DEC, DET), Release DAC Holdoff
0	X	0	0	1	sppf	Set/Reset Parallel Poll Flag
1	0	0	0	0	gts	Go To Standby
1	0	0	0	1	tca	Take Control Asynchronously
1	0	0	1	0	tcs	Take Control Synchronously
1	1	0	1	0	tcse	Take Control Synchronously on End
1	0	0	1	1	ltn	Listen
1	1	0	1	1	ltnc	Listen with Continuous Mode
1	1	1	0	0	lun	Local Unlisten
1	1	1	0	1	epp	Execute Parallel Poll
1	X	1	1	0	sifc	Set/Reset IFC
1	X	1	1	1	sren	Set/Reset REN
1	0	1	0	0	dsc	Disable System Control

Internal Counter

The internal counter generates the state change prohibit times (T_1, T_6, T_7, T_9) specified in the IEEE Standard 488-1978 with reference to the clock frequency. F_3-F_0 specify the clock frequency from 1 to 8 MHz.

Internal Counter

0	0	1	0	F_3	F_2	F_1	F_0

Auxiliary A Register

Of the 5 bits that may be specified as part of its access word, two bits control the IEEE 488 data receiving modes of the IOT7210 and 3 bits control how the EOS message is used.

Auxiliary A Register

1	0	0	A_4	A_3	A_2	A_1	A_0

A_1	A_0	Data Receiving Mode
0	0	Normal Handshake Mode
0	1	RFD Holdoff on All Data Modes
1	0	RFD Holdoff on End Mode
1	1	Continuous Mode

A_2	0 Prohibit 1 Permit	Permits (prohibits) the setting of the END bit by reception of the EOS message
A_3	0 Prohibit 1 Permit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message (TACS)
A_1	0 7-bit EOS 0 8-bit EOS	Makes the 8 bits (7 bits) of the EOS register the valid EOS message

Registers

Auxiliary B Register

The auxiliary B register is much like the A register in that it controls the special operating features of the device.

Auxiliary B Register

1	0	1	B_4	B_3	B_2	B_1	B_0

B_0	1 Permit 0 Prohibit	Permits (prohibits) the setting of the CPT bit on receipt of an undefined command
B_1	1 Permit 0 Prohibit	Permits (prohibits) the transmission of the END message when in serial poll active state (SPAS)
B_2	1 T_1 (high-speed)	T_1 in source handshake function after transmission of second byte following data transmission
	1 T_1 (low-speed)	Sets T_1 in all cases
B_3	1 $\overline{\text{INT}}$ 0 INT	Specifies the active level of the INT pin
B_4	1 *ist* = SRQS	SRQS indicates the value of the ist level local message (the value of the parallel poll flag is ignored) SRQS = 1…ist = 1 SRQS = 0…ist = 0
	0 *ist* = Parallel Poll Flag	The value of the parallel poll flag is taken as the *ist* local message

Auxiliary E Register

The register controls the IOT7210's Data Acceptance modes.

Auxiliary E Register

1	1	0	0	0	0	E_1	E_0

E_0	1 Enable 0 Disable	DAC holdoff by initiation of DCAS
E_1	1 Enable 0 Disable	DAC holdoff by initiation of DTAS

Parallel Poll Register

The Parallel Poll register defines the IOT7210's parallel poll response.

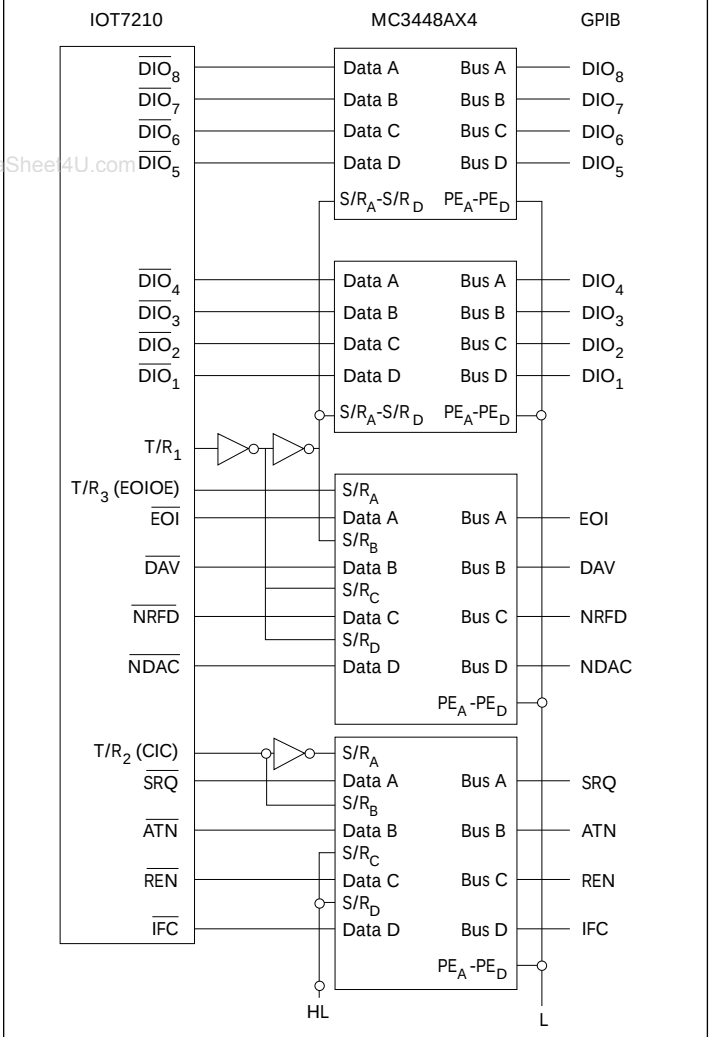
Parallel Poll Register

0	1	1	U	S	P_3	P_2	P_1

U	1 = No Parallel Poll Response 0 = Parallel Poll Response
S	Specify Status Bit Polarity 1 = In Phase 0 = Reverse Phase
P_3 P_2 P_1	Specify Status Bit Output Line (DIO_1-DIO_8)

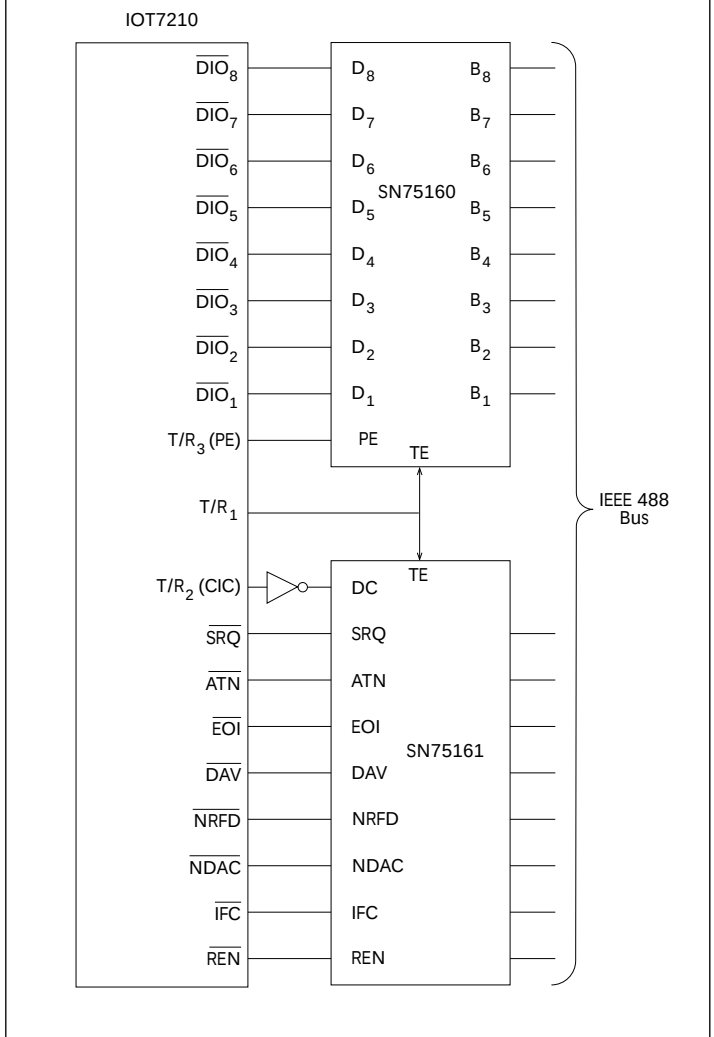
IEEE 488 Transceiver Examples

Low-Speed



In this example, a high-speed data transfer cannot be made since the bus transceiver is of the open-collector type (set B_2 = 0)

High-Speed

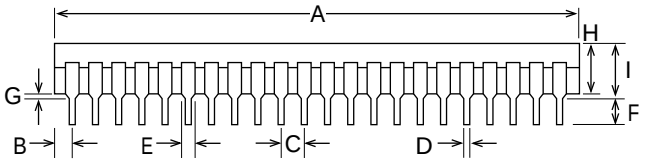


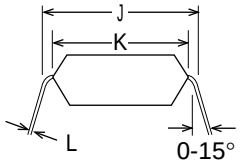
In the case of low-speed data transfer (B_2 = 0), the TR_3 pin can be used as a TRIG output; the PE input of SN75160 should be cleared to 0

Package Outlines

Package Outline for IOT7210P

Item	Millimeters
A	51.94-52.71
B	1.90-2.42
C	2.54 BSC
D	0.38-0.56
E	1.14-1.66
F	3.04-3.56
G	0.38-1.15
H	3.68-3.94
I	4.19-5.59
J	15.24-15.88
K	13.46-14.10
L	0.20-0.36

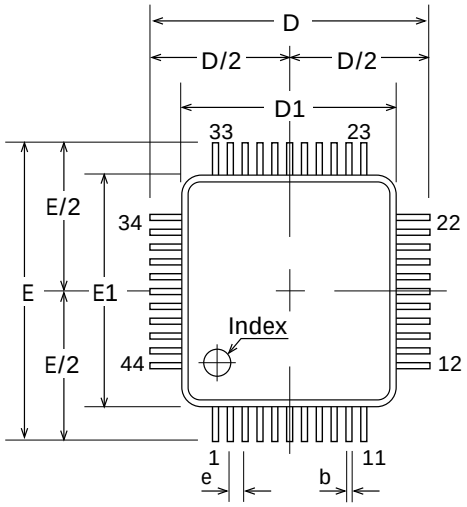


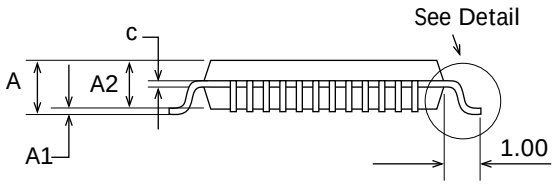


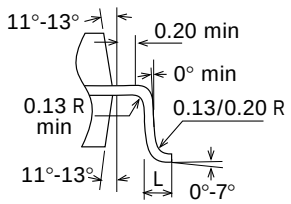
Side View

Package Outline for IOT7210T

Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.27
A1	0.05	0.10	0.15
A2	0.95	1.00	1.12
D		12.00 BSC	
D/2		6.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E/2		6.00 BSC	
E1		10.00 BSC	
L	0.45	0.60	0.75
e		0.80 BSC	
b	0.30	0.37	0.45
c	0.09	-	0.18







Detail

Ordering Information

Ordering Information

Description	Part No.
Low-power CMOS IEEE 488 controller device in a 40-pin plastic DIP	IOT7210P
Low-power CMOS IEEE 488 controller device in a 44-pin plastic TQFP	IOT7210T

Printed in the U.S.A.