Single port 10/100 Fast Ethernet Transceiver

Features

- 10/100Mbps TX
- Full-duplex or half-duplex
- Supports Auto MDI/MDIX function
- Fully compliant with IEEE 802.3/802.3u
- Supports IEEE 802.3u auto-negotiation
- Supports MII interface
- IEEE 802.3 full duplex control specification
- Supports Automatic Power Saving mode
- Supports BaseLine Wander (BLW) compensation
- Supports Interrupt function
- Supports repeater mode
- Single 3.3V power supply with built-in 2.5V regulator
- DSP-based PHY Transceiver technology
- Flexible LED display for speed, duplex, link, activity and collision
- Supports flow control to communicate with other MAC through MDC and MDIO
- 0.25u, CMOS technology
- 48-pin LQFP
- Support Lead Free package (Please refer to the Order Information)

General Description

IP101 LF is an IEEE 802.3/802.3u compliant single-port Fast Ethernet Transceiver for both 100Mbps and 10Mbps operations. It supports Auto MDI/MDIX function to simplify the network installation and reduce the system maintenance cost. To improve the system performance, IP101 LF provides a hardware interrupt pin to indicate the link, speed and duplex status change. IP101 LF provides Media Independent Interface (MII) to connect with different types of 10/100Mb Media Access Controller (MAC). IP101 LF is designed to use category 5 unshielded twisted-pair cable connecting to other LAN devices.

IP101 LF Transceiver is fabricated with advanced CMOS technology, which the chip only requires 3.3V as power supply and consumes very low power in the Auto Power Saving mode. IP101 LF can be implemented as Network Interface Adapter with RJ-45 for twisted-pair connection. It can also be easily implemented into HUB, Switch, Router, Access Point.

Revision History

Revision #	Change Description
IP101 LF-DS-R01	Initial release.
IP101 LF-DS-R02	
IP101 LF-DS-R03	Remove RMII, SNI function. Add digital loopback requirement.
IP101 LF-DS-R04	Add reset timing description to Pin 42 RESET_N in page 9
IP101 LF-DS-R05	Add input voltage swing limit to pin46 X1 and corresponding application circuit. Please refer to page 9, 27 and 29
IP101 LF-DS-R06	Add Crystal Specification and MII Timing.
IP101 LF-DS-R07	Add the order information for lead free package.
IP101 LF-DS-R08	Revise the general description & modify the application diagram.

Transmit and Receive Data Path Block Diagram

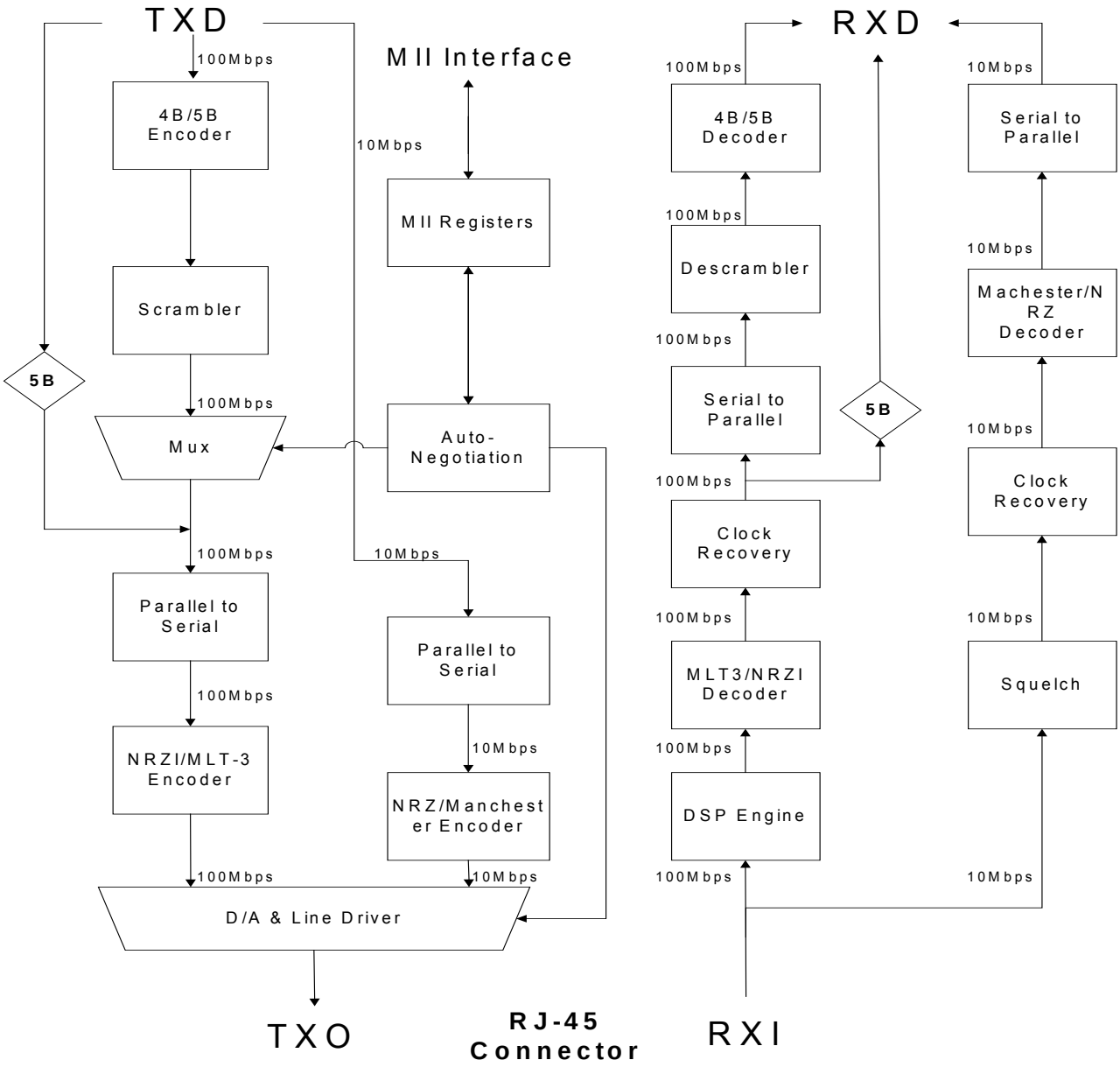


Figure 1: Flow chart of IP101 LF

Pin Assignments

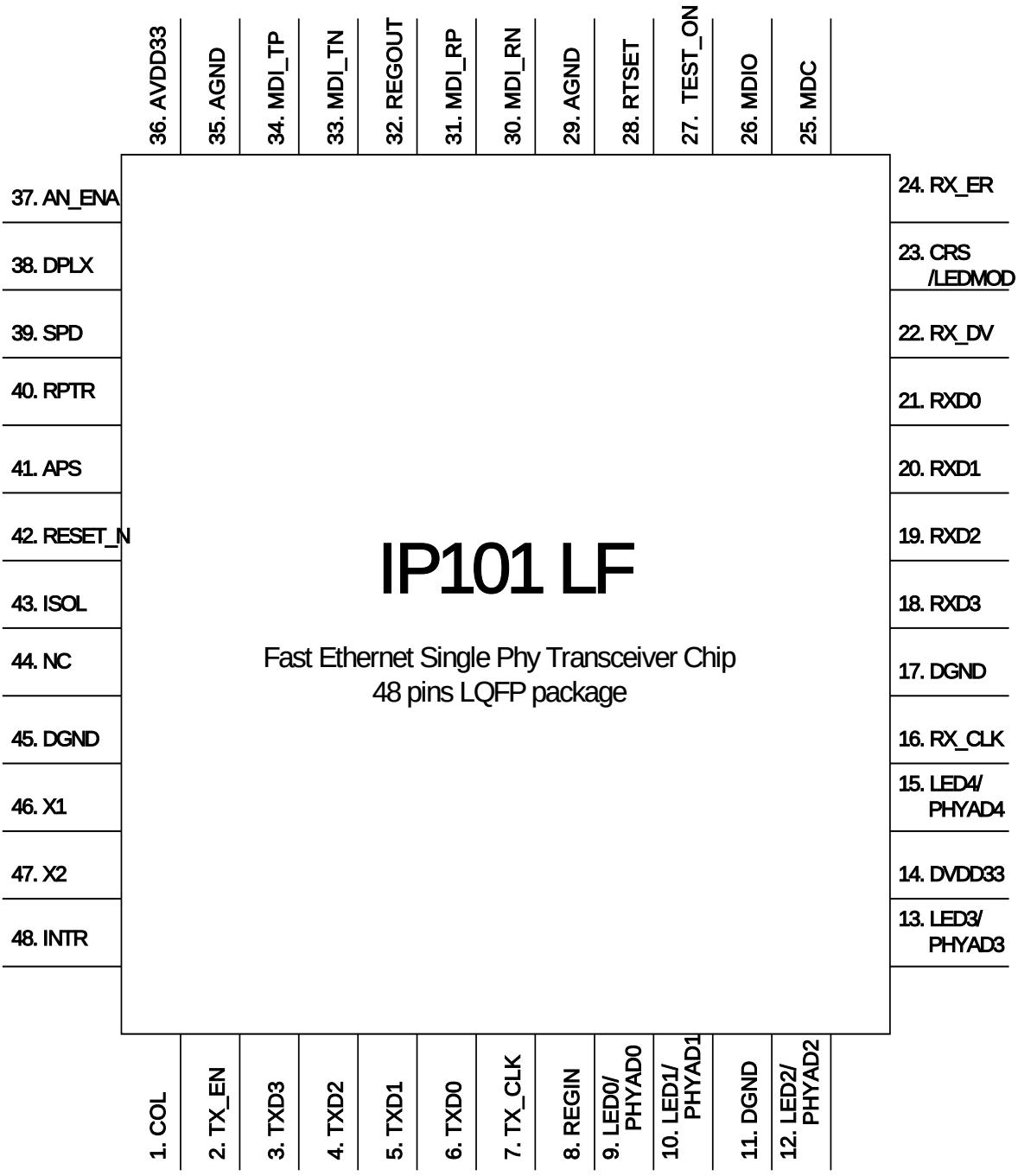


Figure 2 : IP101 LF pins assignment

1 Pin Descriptions

Type	Description
LI	Latched Input in power up or reset
I/O	Bi-directional input and output
I	Input
O	Output

Type	Description
PD	Internal Pull-Down
PU	Internal Pull-Up
P	Power
OD	Open Drain

Pin no.	Label	Type	Description
MII and PCS Interface - Management Interface Pins			
25	MDC	I	**Management Data Interface Clock:** This pin provides a clock reference to MDIO. The clock rate can be up to 10MHz.
26	MDIO	I/O	**Management Data interface Input/Output:** The function of this pin is to transfer management information between PHY and MAC.
MII and PCS Interface – Media Independent Interface (MII) Pins			
2	TX_EN	I (PD)	**Transmit Enable:** This pin is an active high input. At high status, it indicates the nibble data in TXD[3:0] is valid.
7	TX_CLK	O	**Transmit Clock:** This pin provides a continuous 25MHz clock at 100BT and 2.5Mbps at 10BT as timing reference for TXD[3:0] and TX_EN when the chip operates under MII.
3, 4, 5, 6	TXD[3:0]	I	**Transmit Data:** When TX_EN is set high, MAC will transmit data through these 4 lines to PHY which the transmission is synchronizing with TX_CLK.
22	RX_DV	O	**Receive Data Valid:** At high status stands for data flow is present within RXD[0:3] lines and low means no data exchange occurred.
16	RX_CLK	O	**Receive Clock:** This pin provides 25MHz for 100BT or 2.5Mhz for 10BT and RX_DV pin uses this pin as its reference under MII.
18, 19, 20, 21	RXD[3:0]	O	**Receive Data:** These 4 data lines are transmission path for PHY to send data to MAC and they are synchronizing with RX_CLK.

Pin Descriptions (continued)

Pin no.	Label	Type	Description
MII and PCS Interface – Media Independent Interface (MII) Pins			
24	RX_ER	O (PD)	**Receive error:** This pin outputs a high status when errors occurred in the decoded data in the reception. (**Notice:** This pin is pulled down internally)
1	COL	O/LI (PD)	**Collision Detected:** When this pin outputs a high status signal it means collision is detected. (**Notice:** This pin is pulled down internally)
23	CRS/LEDMOD	O (PD)	**Carrier Sense:** When signal output from this pin is high indicates the transmission or reception is in process and at low status means the line is in idle state. **LEDMOD:** During power on reset, this pin status is latched to determine at which LED mode to operate, please refer to the LED pins description. (**Notice:** This pin is pulled down internally)

Pin Descriptions (continued)

Pin no.	Label	Type	Description
Cable Transmission Interface			
34 33	MDI_TP MDI_TN	I/O I/O	**Transmit Output Pair:** Differential pair shared by 100Base-TX, and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 10Base-TX, the output is Manchester code.
31 30	MDI_RP MDI_RN	I/O I/O	**Receive Input Pair:** Differential pair shared by 100Base-TX, and 10Base-T modes.
IC Configuration Options			
43	ISOL	I (PD)	Set high to this pin will isolate IP101 LF from other MAC. This action will also isolate the MDC/MDIO management interface. The power usage is at minimum when this pin is activated. This pin can be directly connected to GND or VCC. (An internal weak pulled-down is used to be inactive as a default)
40	RPTR	I (PD)	Enable this pin to high will put the IP101 LF into repeater mode. This pin can be directly connected to GND or VCC. (An internal weak pulled-down is used to be inactive as a default)
39	SPD	LI/O (PU)	This pin is latched to input during a power on or reset condition. Set high to put the IP101 LF into 100Mbps operation. This pin can be directly connected to GND or VCC. (An internal weak pulled-up is used to set 100Mbps as a default)
38	DPLX	LI/O (PU)	This pin is latched to input during a power on or reset condition. Set high to enable full duplex. This pin can be directly connected to GND or VCC. (An internal weak pulled-up is used to set full duplex as a default)
37	AN_ENA	LI/O (PU)	This pin is latched to input during a power on or reset condition. Set high to enable auto-negotiation mode, set low to force mode. This pin can be directly connected to GND or VCC. (An internal weak pulled-up is used to enable N-WAY as a default)
41	APS	I (PU)	Set high to put the IP101 LF into APS mode. This pin can be directly connected to GND or VCC. Refer to Section 7 for more information. (An internal weak pulled-up is used to enable APS mode as a default)
44	NC	(PU)	This pin should be left open or pull up (Internal pull up.)

Pin Descriptions (continued)

<table>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">LED and PHY Address Configuration</td></tr>
<tr><td colspan="4">These five pins are latched into the IP101 LF during power up reset to configure PHY address [4:0] used for MII management register interface. And then, in normal operation after initial reset, they are used as driving pins for status indication LED. The driving polarity, active low or active high, is determined by each latched status of the PHY address [4:0] during power-up reset. If latched status is high then it will be active low, and if latched status is Low then it will be active high. Moreover, IP101 LF provides 2 LED operation modes. If 2nd LED mode is selected by pulling up pin CRS, only 3 LEDs are needed for status indication. Default is first LED mode.
<table>
<tr><td></td><td>LED mode 1</td><td>LED mode 2</td></tr>
<tr><td>LED0</td><td>LINK</td><td>LINK /ACT(blinking)</td></tr>
<tr><td>LED1</td><td>FULL DUPLEX</td><td>FULL DUPLEX /COL(blinking)</td></tr>
<tr><td>LED2</td><td>10BT /ACT(blinking)</td><td>10BT</td></tr>
<tr><td>LED3</td><td>100BT /ACT(blinking)</td><td>100BT</td></tr>
<tr><td>LED4</td><td>COL</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>9</td><td>PHYAD0/
LED0</td><td>LI/O</td><td>PHY Address [0]
Status:
Mode1: Active when linked.
Mode2: Active when linked and blinking when transmitting or receiving data.</td></tr>
<tr><td>10</td><td>PHYAD1/
LED1</td><td>LI/O</td><td>PHY Address [1]
Status:
Mode1: Active when in Full Duplex operation.
Mode2: Active when in Full Duplex operation and blinking when collisions occur.</td></tr>
<tr><td>12</td><td>PHYAD2/
LED2</td><td>LI/O</td><td>PHY Address [2]
Status:
Mode1: Active when linked in 10Base-T mode, and blinking when transmitting or receiving data.
Mode2: Active when linked in 10Base-T mode.</td></tr>
<tr><td>13</td><td>PHYAD3/
LED3</td><td>LI/O</td><td>PHY Address [3]
Status:
Mode1: Active when linked in 100Base-TX and blinking when transmitting or receiving data.
Mode2: Active when linked in 100Base-TX mode.</td></tr>
<tr><td>15</td><td>PHYAD4/
LED4</td><td>LI/O</td><td>PHY Address [4]
Status:
Mode1: Active when collisions occur.
Mode2: Reserved.</td></tr>
</table>

Pin Descriptions (continued)

Pin no.	Label	Type	Description
Clock and Miscellaneous - Crystal Input/Output Pins			
47	X2	O	**25MHz Crystal Output:** Connects to crystal to provide the 25MHz output. It must be left open when X1 is driven with an external 25MHz oscillator or set to low with a pull down resistor.
46	X1	I	**25MHz Crystal Input:** Connects to crystal to provide the 25MHz crystal input. If a 25MHz oscillator is used, connect X1 to the oscillator output. The input voltage of this pin should not exceed 2.75v. A voltage divider formed by 2 resistors is recommended if the output voltage of oscillator is over 2.75v. Please refer to the application circuit in page 27 and 29
Clock and Miscellaneous - Miscellaneous Pins			
42	RESET_N	I	**RESET_N:** Enable a low status signal will reset the chip. For a complete reset function. 25MHz clock (x1) must be active for a minimum of 10 clock cycles before the rising edge of RESET_N. Chip will be able to operate after 2.5ms delay of the rising edge of RESET_N. The 2.5ms extention is to ensure the stability of system power.
48	INTR	O (OD)	**Interrupt Pin:** When the MII register 17:<15> is set to high, this pin is used as an interrupt pin (Notice: this is an open drain output, so an external pulled-up resistor is needed)
27	TEST_ON	(PD)	**Test Enable:** Set this pin to high to enable test mode, while for normal operation, this pin does not need to be connected. (An internal weak pulled-down is used to disable test mode as a default)
28	ISET	I	**Transmit Bias Resistor Connection:** This pin should be connected to GND via a 6.2KΩ (1%) resistor to define driving current for transmit DAC.

Pin Descriptions (continued)

Pin no.	Label	Type	Description
Power and Ground			
32	REGOUT	P	**Regulator Power Output:** This is a regulator power output for IP101 LF digital circuitry.
36	AVDD33	P	**3.3V Analog power input:** This is a 3.3V power supply for analog circuitry, and it should be decoupled carefully.
29,35	AGND	P	**Analog Ground:** These 2 pins should connect to motherboard's GND.
8	REGIN	P	**Regulator Power Input:** This is a regulator power input from Pin32. No external regulator needed.
14	DVDD33	P	**3.3V Digital Power input:** This is a 3.3V power supply for digital circuitry.
11,17,45	DGND	P	**Digital Ground:** These 3 pins should connect to motherboard's GND.

2 Register Descriptions

Bit Bit	Name	Description/Usage	Default value (h): 3100
Register 0 : MII Control Register			
15	Reset	When set, this action will bring both status and control registers of the PHY to default state. This bit is self-clearing. 1 = Software reset 0 = Normal operation	0, RW
14	Loop-back	This bit enables loop-back of transmit data to the receive data path, i.e., TXD to RXD. IP101 LF requires at least 512us to link after programming this bit. TX/RX packets should be activated after 512us. 1 = enable loop-back 0 = normal operation	0, RW
13	Speed Selection	This bit sets the speed of transmission. 1 = 100Mbps 0 = 10Mbps	1, RW
12	Auto-Negotiation Enable	This bit determines the auto-negotiation function. 1 = enable auto-negotiation; bits 13 and 8 will be ignored. 0 = disable auto-negotiation; bits 13 and 0:<8> will determine the link speed and the data transfer mode, under this condition. Auto-MDIX function should be disabled (set Reg16.11=1) if this bit has been set to “0”. Please refer to section 7 Auto-MDIX function description for details.	1, RW (TP)
11	Power Down	This bit will turn down the power of the PHY chip and the internal crystal oscillator circuit if this bit is enabled. The MDC and MDIO are still activated for accessing to the MAC. 1 = power down 0 = normal operation	0, RW
10	Isolate	1=electrically Isolate PHY from MII but not isolate MDC and MDIO 0=normal operation	0,RW
9	Restart Auto-Negotiation	This bit allows the Nway auto-negotiation function to be reset. 1 = restart auto-negotiation 0 = normal operation	0, RW
8	Duplex Mode	This bit sets the duplex mode if auto-negotiation is disabled (bit 12=0) 1 = full duplex 0 = half duplex After completing auto-negotiation, this bit will reflect the duplex status.(1: Full duplex, 0: Half duplex)	1, RW
7	Collision Test	1=enable COL signal test 0=disable COL signal test	0,RW
6:0	Reserved		0, RO

Register Descriptions (continued)

Bit	Name	Description/Usage	Default value (h): 7849
Register 1 : MII Status Register			
15	100Base-T4	1 = enable 100Base-T4 support 0 = suppress 100Base-T4 support	0, RO
14	100Base-TX Full Duplex	1 = enable 100Base-TX full duplex support 0 = suppress 100Base-TX full duplex support	1, RO
13	100BASE-TX Half Duplex	1 = enable 100Base-TX half duplex support 0 = suppress 100Base-TX half duplex support	1, RO
12	10Base-T Full Duplex	1 = enable 10Base-T full duplex support 0 = suppress 10Base-T full duplex support	1, RO
11	10_Base-T Half Duplex	1 = enable 10Base-T half duplex support 0 = suppress 10Base-T half duplex support	1, RO
10:7	Reserved		0, RO
6	MF Preamble Suppression	The IP101 LF will accept management frames with preamble suppressed. The IP101 LF accepts management frames without preamble. A Minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE802.3u specifications	1, RO
5	Auto-Negotiation Complete	1 = auto-negotiation process completed 0 = auto-negotiation process not completed	0, RO
4	Remote Fault	1 = remote fault condition detected (cleared on read) 0 = no remote fault condition detected	0, RO/LH
3	Auto-Negotiation	1 = Link had not been experienced fail state 0 = Link had been experienced fail state	1, RO
2	Link Status	1 = valid link established 0 = no valid link established	0, RO/LL
1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	0, RO/LH
0	Extended Capability	1 = extended register capability 0 = basic register capability only	1, RO

Register Descriptions (continued)

Bit	Name	Description/Usage	Default value (h): 0243
Register 2 : PHY Identifier Register 1			
15:0	PHYID1	PHY identifier ID for software recognize IP101 LF	0X0243, RO

Bit	Name	Description/Usage	Default value (h): 0C54
Register 3 : PHY Identifier Register 2			
15:0	PHYID2	PHY identifier ID for software recognize	0X0C54, RO

Note : Register 2 and register 3 identifier registers altogether consist of Vender model, model revision number and Organizationally Unique identifier (OUI) information. Total of 32 bits allocate in these 2 registers and they can return all zeroes in all bits if desired. Register 2 contains OUI's most significant bits and OUI's lest significant bits, Vender model, Model revision number are allocated in register 3.

Register Descriptions (continued)

Register 4 lists the advertised abilities during auto-negotiation for what will be transmitted to IP101 LF's Link Partner.

Bit	Name	Description/Usage	Default value (h): 0001
Register 4 : Auto-Negotiation Advertisement Register			
15	NP	Next Page bit. 0 = transmitting the primary capability data page 1 = transmitting the protocol specific data page	0, RO
14	Reserved		0, RO
13	RF	1 = advertise remote fault detection capability 0 = do not advertise remote fault detection capability Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "1". Hardware reset or power on reset will set it to default value.	0, RW
12	Reserved		0, RW
11	Asymmetric. Pause	1 = asymmetric flow control is supported by local node 0 = asymmetric flow control is NOT supported by local node Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "1". Hardware reset or power on reset will set it to default value.	0, RW
10	Pause	1 = flow control is supported by local node 0 = flow control is NOT supported by local node Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "1". Hardware reset or power on reset will set it to default value.	0, RW
9	T4	1 = 100Base-T4 is supported by local node 0 = 100Base-T4 not supported by local node Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "0". Hardware reset or power on reset will set it to default value.	0, RO
8	TX Full Duplex	1 = 100Base-TX full duplex is supported by local node 0 = 100Base-TX full duplex not supported by local node Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "0". Hardware reset or power on reset will set it to default value.	1, RW
7	TX	1 = 100Base-TX is supported by local node 0 = 100Base-TX not supported by local node Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "0". Hardware reset or power on reset will set it to default value.	1, RW
6	10 Full Duplex	1 = 10Base-T full duplex supported by local node 0 = 10Base-T full duplex not supported by local node Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "0". Hardware reset or power on reset will set it to default value.	1, RW

Register Descriptions (continued)

Bit	Name	Description/Usage	Default value (h): 0001
Register 4 : Auto-Negotiation Advertisement Register (continued)			
5	10	1 = 10Base-T is supported by local node 0 = 10Base-T not supported by local node Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to “0”. Hardware reset or power on reset will set it to default value.	1, RW
4:0	Selector	Binary encoded selector supported by this node. Currently only CSMA/CD <00001> is specified. No other protocols are supported.	<00001>, RO

Register Descriptions (continued)

Register 5 describes the advertised abilities of the Link Partner's PHY when it is receiving data during the process of auto-negotiation. If next-pages are supported, this register may change after the auto-negotiation has established.

Bit	Name	Description/Usage	Default value (h): 0080
Register 5 : Auto-Negotiation Link Partner Ability Register			
15	Next Page	Next Page bit. 0 = transmitting the primary capability data page 1 = transmitting the protocol specific data page	0, RO
14	Acknowledge	1 = link partner acknowledges reception of local node's capability data word 0 = no acknowledgement	0, RO
13	Remote Fault	1 = link partner is indicating a remote fault 0 = link partner does not indicate a remote fault	0, RO
12	Reserved		0, RO
11	Asymmetric. Pause	1 = asymmetric flow control is supported by local node 0 = asymmetric flow control is NOT supported by local node	0, RO
10	Pause	1 = flow control is supported by Link partner 0 = flow control is NOT supported by Link partner	0, RO
9	T4	1 = 100Base-T4 is supported by link partner 0 = 100Base-T4 not supported by link partner	0, RO
8	TXFD	1 = 100Base-TX full duplex is supported by link partner 0 = 100Base-TX full duplex not supported by link partner	0, RO
7	100BASE-TX	1 = 100Base-TX is supported by link partner 0 = 100Base-TX not supported by link partner This bit will also be set after the link in 100Base is established by parallel detection.	0, RO
6	10FD	1 = 10Base-T full duplex is supported by link partner 0 = 10Base-T full duplex not supported by link partner	0, RO
5	10Base-T	1 = 10Base-T is supported by link partner 0 = 10Base-T not supported by link partner This bit will also be set after the link in 10Base is established by parallel detection.	0, RO
4:0	Selector	Link Partner's binary encoded node selector Currently only CSMA/CD <00001> is specified	<00000>, RO

Register Descriptions (continued)

Register 6 defines more auto-negotiation registers to meet the requirement.

Bit	Name	Description/Usage	Default value (h): 0000
Register 6 : Auto-Negotiation Expansion Register			
15:5	Reserved	This bit is always set to 0.	0, RO
4	MLF	This status indicates if a multiple link fault has occurred. 1 = fault occurred 0 = no fault occurred	0, RO
3	LP_NP_ABLE	This status indicates if the link partner supports Next Page negotiation. 1 = supported 0 = not supported	0, RO
2	NP_ABLE	This bit indicates if the device is able to send additional Next Pages.	0, RO
1	PAGE_RX	This bit will be set if a new link code word page has been received. It is cleared automatically after the auto-negotiation link partner's ability register (register 5) is read by the management.	0, RO
0	LP_NW_ABLE	1 = link partner supports Nway auto-negotiation.	0, RO

Register Descriptions (continued)

Register 16 and register 17 are defined by IC Plus Corp. and some of them are for internal testing purpose.

Bit	Name	Description/Usage	Default value (h): 0000
Register 16 : PHY Spec. Control Register			
15	Debug Mode	0 = IP101 LF operates at normal mode 1 = IP101 LF operates at debug mode, for internal use only (Notice the functionalities of bit 16:<14>, 16:<13>, 16:<12>, and 16:<4:0> depend on the setting of this bit 16:<15> Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "1". Hardware reset or power on reset will set it to default value.	0, R/W
14:12	Reserved		0, RO
11	Auto MDIX Off	Set high to disable the automatic switch of MDI and MDI-X modes. If AN is disabled by setting pin37=0 during power up, this bit will be set to 1 (Auto-MDIX off) automatically. Setting Reg0.12=1 will re-activate AN, in this case, if user needs Auto-MDIX function, this bit should be set to 0. For details, please refer to section 7 Auto-MDIX function description.	0, R/W
10	Heart Beat Enable	Heart beat function enable at 10Base-T Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "1". Hardware reset or power on reset will set it to default value.	0, R/W
9	Jabber Enable	Jabber function enable at 10Base-T Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "1". Hardware reset or power on reset will set it to default value.	0, R/W
8	Far-End Fault Enable/Disable	To enable or disable the functionality of Far-End Fault Mode Enable Disable 100Base-TX 1 0 Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "1". Hardware reset or power on reset will set it to default value.	0, R/W
7	Analog Power Saving Disable	Set high to disable the power saving during auto-negotiation Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "1". Hardware reset or power on reset will set it to default value.	0, R/W
6	Reserved		0, RO
5	Bypass DSP reset	Set high to bypass the reset DSP mechanism in PCS sub-layer Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to "1". Hardware reset or power on reset will set it to default value.	0, R/W
4:3	Reserved		0, RO

Register Descriptions (continued)

Bit	Name	Description/Usage	Default value (h): 0000
Register 16 : PHY Spec. Control Register (continued)			
2	Repeater Mode	Set high to put IP101 LF into repeater mode Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to “1”. Hardware reset or power on reset will set it to default value.	0, R/W
1	APS Mode	Set high to enable Auto Power Saving mode Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to “1”. Hardware reset or power on reset will set it to default value.	0, R/W
0	Analog Off	Set high to power down analog transceiver Software reset(reg0.15) will not set this bit to default value if this bit has been programmed to “1”. Hardware reset or power on reset will set it to default value.	0, R/W

Register Descriptions (continued)

Bit	Name	Description/Usage	Default value (h): 0E00
Register 17 : PHY Interrupt Ctrl/Status Register			
15	INTR pin used	Set high to enable pin48 as an interrupt pin. Pin48 will be high impedance if this bit is set low.	0, R/W
14:12	Reserved		0, RO
11	All Mask	When this bit is set high, changes in all events will not cause an interrupt	1, R/W
10	Speed Mask	When this bit is set high, changes in speed mode will not cause an interrupt	1, R/W
9	Duplex Mask	When this bit is set high, changes in duplex mode will not cause an interrupt	1, R/W
8	Link Mask	When this bit is set high, changes in link status will not cause an interrupt	1, R/W
7	Arbiter State Enable	When this bit is set low, changes in N-WAY arbiter state machine will not cause an interrupt	0, R/W
6	Arbiter State Change	Flag to indicate N-WAY arbiter change interrupt	0, RC
5:3	Reserved		0, RO
2	Link Status Change	Flag to indicate link status change interrupt	0, RC
1	Speed Change	Flag to indicate speed change interrupt	0, RC
0	Duplex Change	Flag to indicate duplex change interrupt	0, RC

3 Functional Description

IP101 LF 10/100Mbps Ethernet PHY Transceiver integrates 100 Base-TX and 10 Base-T modules into a single chip. IP101 LF acts as an interface between physical signaling and Media Access Controller (MAC).

IP101 LF has several major functions:
1. **PCS layer (Physical Coding Sub-Layer)**: This function contains transmit, receive and carrier sense functional circuitries.
2. **Management interface**: Media Independent Interface (MII) registers contains information for communication with other MAC.
3. **Auto-Negotiation**: Communication conditions between 2 PHY transceivers. IP101 LF advertise its own ability and also detects corresponding operational mode from the other party, eventually both sides will come to an agreement for their optimized transmission mode.

IP101 LF's major features included:
1. Flow Control ability
2. LED configuration access
3. Operation modes for both full and half duplex
4. APS (Auto Power Saving) mode
5. Base Line Wander (BLW) compensation
6. Auto MDI/MDIX function
7. Interrupt function
8. Repeater Mode

Major Functional Block Description

The functional blocks diagram is referred to Figure 1:

1. **4B/5B encoder:** 100 Base-X transmissions require converting 4-bit nibble data into 5-bit wide data code-word format. Transmitting data is packaged by J/K codes at the start of packet and by T/R codes at the end of packet in the 4B/5B block. When transmit error has occurred during a transmitting process, the H error code will be sent. The idle code is sent between two packets.

2. **4B/5B Decoder:** The decoder performs the 5B/4B decoding from the received code-groups. The 5 bits (5B) data is decoded into four bits nibble data. The decoded 4 bit (4B) data is then forwarded through MII to the repeater, switch or MAC device. The SSD is then converted into 4B 5 nibbles and the ESD and IDLE Codes are replaced by 4B 0 nibbles data. The decoded data is driven onto the corresponding MII port or shared MII port. Receiving an invalid code group will cause PHY to assert the MII RXER signal.

3. **Scrambler/Descrambler:** Repetitive patterns exist in 4B/5B encoded data which result in large RF spectrum peaks and keep the system from being approved by regulatory agencies. The peak in the radiated signal is reduced significantly by scrambling the transmitted signal. Scrambler adds a random generator to the data signal output. The resulting signal is with fewer repetitive data patterns. The scrambled data stream is descrambled at the receiver by adding another random generator to the output. The receiver's random generator has the same function as the transmitter's random generator. Scrambler operation is dictated by the 100Base-X and TP_FDDI standards.

4. **NRZI/MLT-3(Manchester) Encoder and Decoder:** 100 Base-TX Transmission requires to encode the data into NRZ format and again converted into MLT-3 signal, while 10 Base-T will convert into Manchester form after NRZ coding. This helps to remove the high frequency noise generated by the twisted pair cables. At receiving end, the coding is reversed from MLT-3 (Manchester) signal back to NRZ format.

5. **Clock Recovery:** The receiver circuit recovers data from the input stream by regenerating clocking information embedded in the serial stream. The clock recovery block extracts the RXCLK from the transition of received

6. **DSP Engine:** This block includes Adaptive equalizer and Base Line Wander correction function.

Transmission Description

10Mbps Transmit flow path:

TXD ➔ Parallel to Serial ➔ NRZI/Manchester Encoder ➔ D/A & line driver ➔ TXO

After MAC passes data to PHY via 4 bits nibbles, the data are serialized in the parallel to serial converter. The converter outputs NRZI coded data which the data are then mapped to Manchester code within the Manchester Encoder. Before transmitting to the physical medium, the Manchester coded data are shaped by D/A converter to fit the physical medium.

10Mbps Receive:

RXI ➔ Squelch ➔ Clock Recovery ➔ Manchester/NRZ Decoder ➔ Serial to Parallel ➔ RXD

The squelch block determines valid data from both AC timing and DC amplitude measurement. When a valid data is present in the medium, squelch block will generate a signal to indicate the data has received. The data receive are coded in Manchester form, and are decoded in the Manchester to NRZ Decoder. Then the data are mapped to 4 bits nibbles and transmitted onto MAC interface.

100Mbps TX Transmit:

TXD ➔ 4B/5B Encoder ➔ Scrambler ➔ NRZI/MLT-3 Encoder ➔ D/A & line driver ➔ TXO

The major differences between 10Mbps transmission and 100Mbps transmission are that 100Mbps transmission requires to be coded from 4-bit wide nibbles to 5 bits wide data coding, and after that the data are scrambled through scrambler to reduce the radiated energy generated by the 4B/5B conversion. Then the data is converted into NRZI form and again from NRZI coded form into MLT-3 form. The MLT-3 data form is fed into D/A converter and shaped to fit the physical medium transmission.

100Mbps TX Receive:

RXI ➔ DSP ➔ Serial to Parallel ➔ Descrambler ➔ 4B/5B Decoder ➔ RXD

The received data first go through DSP engines which includes adaptive equalizer and base-line wander correction mechanism. The adaptive equalizer will compensate the loss of signals during the transmission, while base-line wander monitors and corrects the equalization process. If a valid data is detected then the data are parallelized in Serial to Parallel block, which it converts NRZI coded data form back to scrambled data. The scrambled data are descrambled and converted back to 4 bits–wide format data and then feed into MAC.

MII and Management Control Interface

Media Independent Interface (MII) is described in clause 22 in the IEEE 802.3u standard. The main function of this interface is to provide a communication path between PHY and MAC/Repeater. It can operate either in 10Mb or 100Mb environment, and operate at 2.5MHz frequency for 10Mb clock data rate or 25MHz frequency for 100Mb data rate transmission. MII consists of 4 bit wide data path for both transmit and receive. The transmission pins consists of TXD[3:0], TX_EN and TXC, and at receiving MII pins have RXD[3:0], RXER, RX_DV and RXC. The Management control pins include MDC and MDIO. MDC, Management Data Clock, provides management data clock at maximum of 10MHz as a reference for MDIO, Management Data Input/Output. CRS, Carrier Sense, is used for signaling data transmission is in process while COL, Collision, is used for signaling the occurrence of collision during transmission.

Transmitting a packet, MAC will first assert TX_EN and convert the information into 4 bit wide data and then pass the data to IP101 LF. IP101 LF will sample the data according to TX_CLK until TX_EN is low. While receiving a packet, IP101 LF asserts RX_DV high when data present in the medium through RXD[3:0] bus lines. IP101 LF samples received data according to RX_CLK until the medium is back to idle state.

Auto-Negotiation and Related Information

IP101 LF supports clause 28 in the IEEE 802.3u standard. IP101 LF can be operated either in 10Mbps/100Mbps or half/full duplex transmission mode. IP101 LF also supports flow control mechanism to prevent any collision in the network. If the other end does not support N-Way function, IP101 LF will link at half duplex mode and enter parallel detection.

At beginning of auto-negotiation, IP101 LF will advertise its own ability by sending FLP waveform out to the other end and also listening signals from the other end. IP101 LF will place itself into correct connection speed depends on the received signals. If NLP signal is replied from the other end, IP101 LF will enter 10Mbps, while active idle pulses (unique 100Mbps pattern) IP101 LF will go to 100Mbps mode instead.

Once the negotiation has completed with the other party, IP101 LF will configure itself to the desired connection mode, i.e., 10/100Mbps or Half/Full duplex modes. If there is no detection of link pulses within 1200ms~1500mS, IP101 LF will enter Link Fail State and restart auto-negotiation procedure.

The auto-negotiation information is stored in the IP101 LF's MII registers. These registers can be modified and monitor the IP101 LF's N-Way status. The reset auto-negotiation in register 0 of MII registers can be set at any time to restart auto-negotiation.

The flow control ability is also included in the IP101 LF chip. If MAC supports flow control condition, then flow control will be enabled by setting bit 10 (Pause) of the Register 4.

Pin 37 (AN_ENA), 38 (DLPX), 39 (SPD) can be configured manually to set IP101 LF's transmission ability.

1. Enabling Pin 37 (set high) will put IP101 LF to N-Way mode, if set low to pin 37, it will put IP101 LF into forced mode.
2. Pin 38 will configure Duplex ability of IP101 LF, at high, IP101 LF is set to Full-Duplex and low will let IP101 LF enter half duplex mode.
3. Pin 39 determines the speed of connection. If the pin is pulled high, IP101 LF is set at 100Mbps, while at low will make IP101 LF to connect at 10Mbps speed.

AN_ENA (Pin 37)	DLPX (Pin38)	SPD (Pin39)	Operation
H	L	L	NWAY enable, the ability field does not support 100Mbps and full duplex mode operation
H	H	L	NWAY enable, the ability field does not support 100Mbps operation
H	L	H	NWAY enable, the ability field does not support full duplex mode operation
H	H	H	Default setup, auto-negotiation enable, the IP101 LF will support 10BT/100BT, half/full duplex mode operation
L	L	L	NWAY disable, force the IP101 LF into 10BT and half duplex mode.
L	H	L	NWAY disable, force the IP101 LF into 10BT and full duplex mode.

L	L	H	NWAY disable, force the IP101 LF into 100BT and half duplex mode.
L	H	H	NWAY disable, force the IP101 LF into 100BT and full duplex mode.

Auto MDIX function

Since Auto MDIX function is part of AN function, IP101 LF supports Auto MDIX function only if AN is enabled. IP101 LF will keep sensing incoming signal in MDI RX pair, if no incoming signal is detected, IP101 LF will switch TX and RX pairs automatically trying to establish connection. If AN is disabled by setting Pin37=0 during reset, Auto-MDIX will be disabled automatically. However, if AN is re-activated by setting reg0.12=1, Auto-MDIX will still be disabled. In this case, if user wants to activate Auto-MDIX function, setting reg16.11=0 will solve. The other condition is, pin37 (AN_ENA)=1 during reset, and reg0.12 has been set to "0" later on, in this case we suggest user to disable Auto-MDIX function by setting reg16.11=1; otherwise, there might be link problems for certain kinds of link partners.

LED Configuration

IP101 LF provides 2 LED operation modes,

Mode 1 (default):

LED	Function
LED0	Link status: Active indicates the link has established
LED1	Duplex operation: Active indicates full duplex
LED2	10BT/ACT: Active indicates 10Mbps connection has established, and blinking while TX/RX events occur.
LED3	100BT/ACT: Active indicates 100Mbps connection has established, and blinking while TX/RX events occur.
LED4	Collision detect: Active indicates Collision has occurred

Mode 2 (could be set by pulling up CRS with a 4.7K resistor):

LED	Function
LED0	Link/ACT: Active indicates the link has established, and blinking while TX/RX events occur.
LED1	Duplex/COL: Active indicates full duplex, and blinking while collision events occur.
LED2	10BT: Active indicates 10Mbps connection has established
LED3	100BT: Active indicates 100Mbps connection has established
LED4	-

LED pins also include the information of PHY address, the default PHY address is set at 00001b (01h). The PHY address can be modified by changing the LED circuitry. The modification can be arranged as follow:

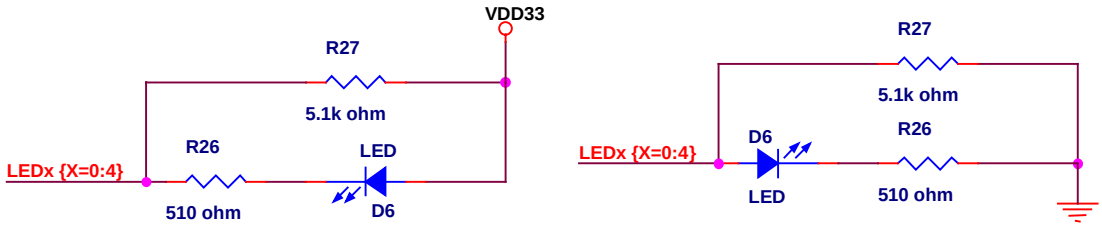


Figure 3: PHY address Configuration

The left diagram will enable the specific PHY address to 1, if it is connected to VDD33. The diagram on the right shows the configuration for setting PHY address to 0, when the circuit is connected to ground. By setting either one of the bits according to the diagram will allow one to modify PHY addresses from PHYAD0 to PHYAD4.

Power-Down Modes

IP101 LF can be power-down by 4 methods. These 4 methods are as follow:
Power Down in bit 11 of Register 0: Enable this bit will disconnect the power to IP101 LF and also internal clock, but MDC and MDIO are still activated.
APS mode in bit 1 of Register 16: Set high to this bit will let PHY into power saving mode, MDC and MDIO are also activated.
Analog off in bit 0 of Register 16: Enable this bit will put IP101 LF in analog off state. This will power down all analog functions but internal 25MHz operating clock is active, and MDC and MDIO are also activated.
ISOL pin (pin 43): Set high will isolate IP101 LF from MAC and disable management interface (MDC and MDIO). The power usage is at minimum when this pin is activated.

Repeater Modes

To enter Repeater mode, one can either set pin 40 (RPTR) to high or set 1 to bit 2 of Register 16 will allow IP101 LF to enter Repeater mode. If IP101 LF is used in repeater, CRS will be high if IC is in process of receiving packets, while IP101 LF is used in a network interface card, CRS will be generated in both transmitting and receiving packets.

Miscellaneous

ISET (pin 28) should be connected to GND via a 6.2k ohm resistor with 1% accuracy to ensure a correct driving current for transmit DAC.

Set low to pin 42, REST_N, for at least 10ms will reset all functions available in IP101 LF. The bit 15 of Register 0 will put PHY into its default status.

Interrupt

IP101 LF provides 4 kinds of interrupt function: speed change, duplex change, link change and arbiter state change. Interrupt masks could be selected by Reg 17, and an active low interrupt will be sent from pin48 when event occurs.

4 Crystal Specifications

Item	Parameter	Range
1	Nominal Frequency	25.000 MHz
2	Oscillation Mode	Fundamental Mode
3	Frequency Tolerance at 25˚C	+/- 50 ppm
4	Temperature Characteristics	+/- 50 ppm
5	Operating Temperature Range	-10˚C ~ +70˚C
6	Equivalent Series Resistance	40 ohm Max.
7	Drive Level	100μW
8	Load Capacitance	20 pF
9	Shunt Capacitance	7 pF Max
10	Insulation Resistance	Mega ohm Min./DC 100V
11	Aging Rate A Year	+/- 5 ppm/year

5 Layout Guideline

General Layout Guideline

Best performance depends on good layout. The following recommendation steps will help customer to gain maximum performance.

Create good power source to minimize noise from switching power source.

- All components are qualified, especially high noise component, such as clock component.
- Use bulk capacitors between power plane and ground plane for 4 layers board, signals trace on component and bottom side, power plane on third layer, and ground layer on second layer.
- Use decoupling capacitors to decouple high frequency noise between chip's power and ground, must be as close as possible to IP101 LF.
- The clock trace length to IP101 LF must be equal the clock trace length to MAC.
- Use guard traces to protect clock traces if possible
- Avoid signals path parallel to clock signals path, because clock signals will interference with other parallel signals, degrading signal quality, such as MDC and X1signals.
- The clock must be low jitter with less than 0.5ns for 25Mhz 100ppm.
- Avoid highly speed signal across ground gap to prevent large EMI effect.
- Keep ground region as one continuous and unbroken plane.
- Place a gap between the system and chassis grounds.
- No any ground loop exists on the chassis ground.

Twisted Pair recommendation

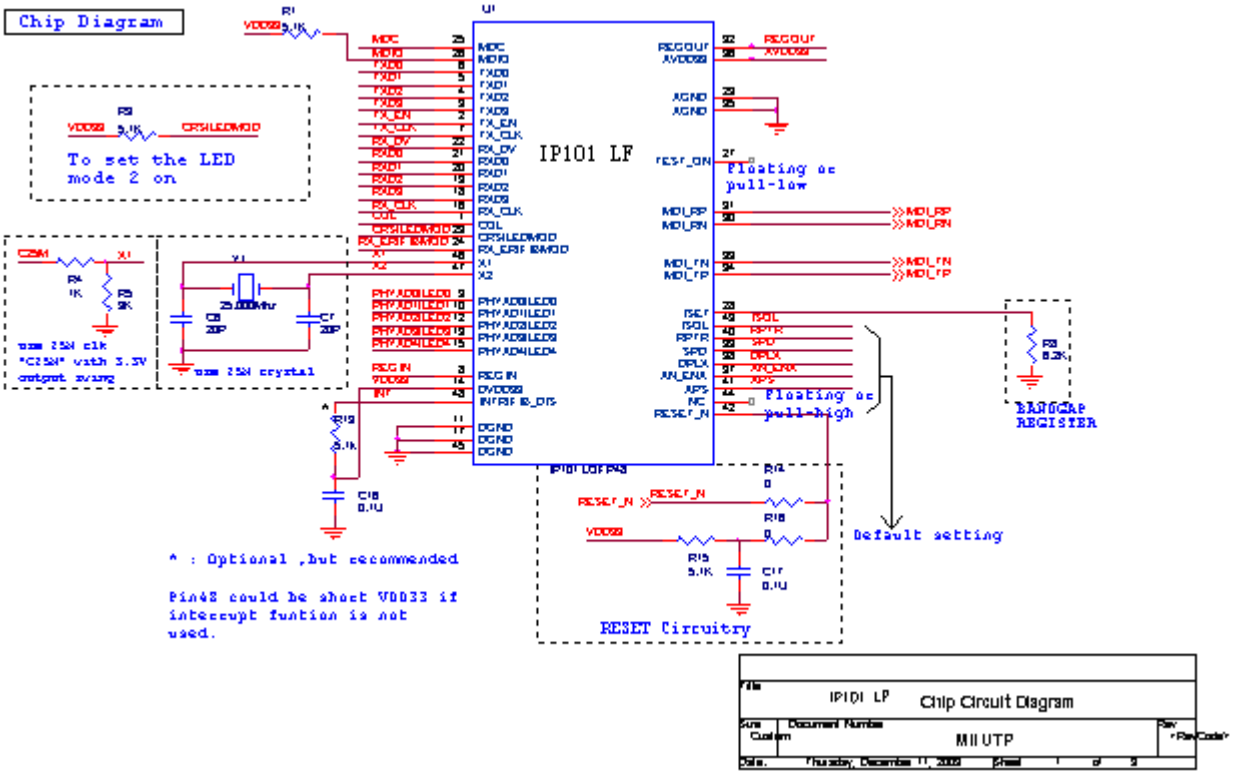
When routing the TD+/- signal traces from IP101 LF to transformer, the traces should be as short as possible, the termination resistors should be as close as possible to the output of the TD+/- pair of IP101 LF. Center tap of primary winding of these transformers must be connected to analog 2.5V respectively. It is recommended that RD+/- trace pair be route such that the space between it and others is three times space, which can separate individual traces from one another.

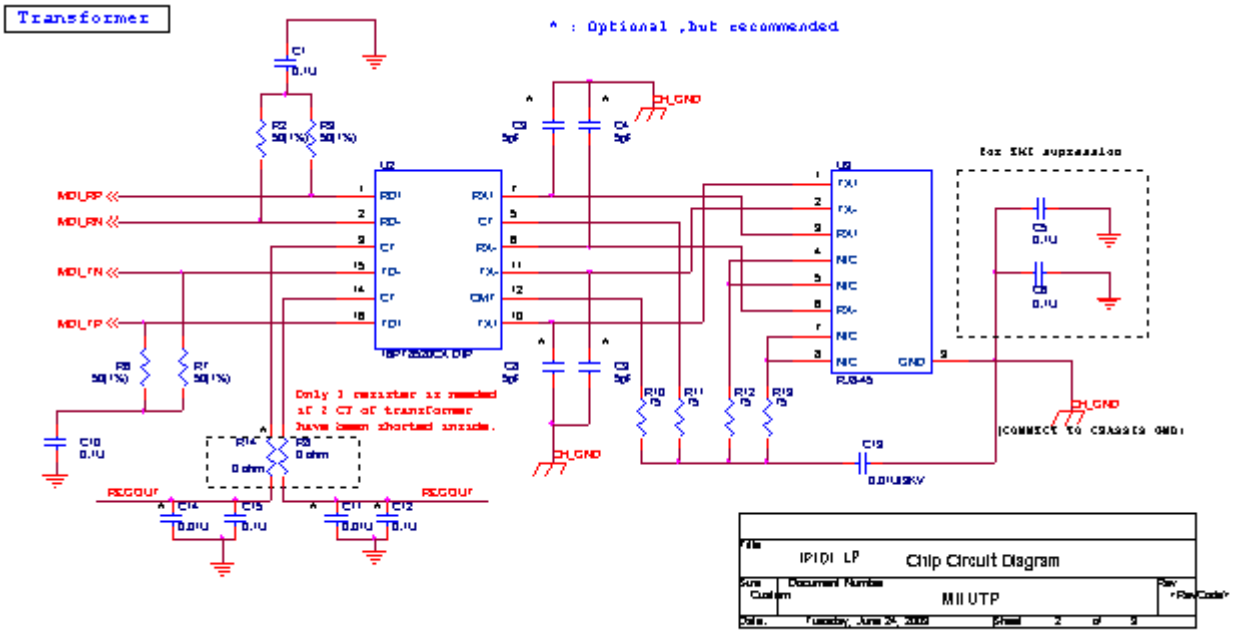
It is recommended that offers chassis ground in the area between transformer and media connector (RJ-45 port), this isolates the analog signals from external noise sources and reduces EMI effect. Note the usage of the vias, it is best not use via to place anywhere other than in close proximity to device, in order to minimize impedance variations in a given signal trace.

6 Circuit Diagram

There are 2 suggested circuit diagrams for IP101 LF.

6.1 MII interface with UTP

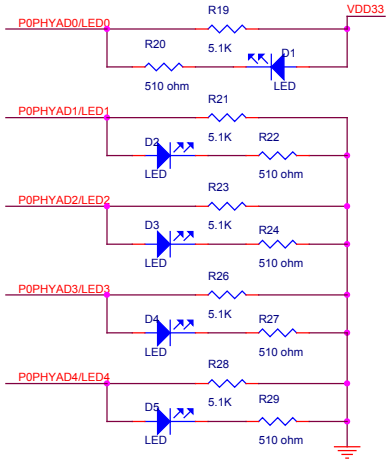




MII interface with UTP (continued)

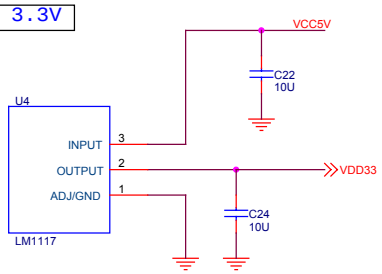
LED and PHY address Configuration

This schematic sets PHY address to 00001b.

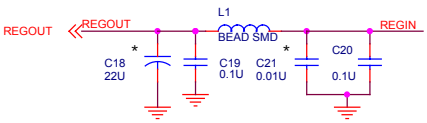


LED0	LED1	LED2	LED3	LED4
Link	Dupx	10Act	100Act	COL

Power: 5V ~ 3.3V



REGOUT and REGIN connection

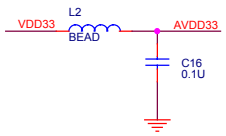


* : Optional ,but recommended

Hardwire Configuration network:

1. This configuration shows
   Enable: Auto negotiation, Full duplex, 100Mbps,
   Link Down Power Saving, MII interface
   Disable: Isolate, Repeater mode
2. These senven configuration pins could be connected to VDD or GND directly.

Analog and Digital 3.3V connection



Title	IP101 Chip Circuit Diagram	
Size A	Document Number MII UTP	Rev <RevCode>
Date: Tuesday, June 24, 2003	Sheet 3 of 3	

7 Electrical Characteristics

7.1 D.C. Characteristic

7.1.1 Absolute Maximum Rating

Symbol	Conditions	Minimum	Typical	Maximum
Supply Voltage		3.0 V	3.3V	3.6V
Storage Temp		-55°C		125°C

7.1.2 Power Dissipation

Symbol	IP101 LF
Auto Power Saving Mode	27mA
Analog off Mode	8mA
Power Down Mode	4mA
Isolate Mode	3mA
100 Full	136mA
100 Half	140mA
10 Full	149mA
10 Half	149mA
10 Transmit	149mA
10 Receive	149mA
10 IDLE	73mA

7.1.3 Operating Condition

Symbol	Conditions	Minimum	Typical	Maximum
Vcc	3.3V Supply voltage	3.0 V	3.3V	3.6V
TA	Operating Temperature	0°C		70°C

7.1.4 Supply Voltage

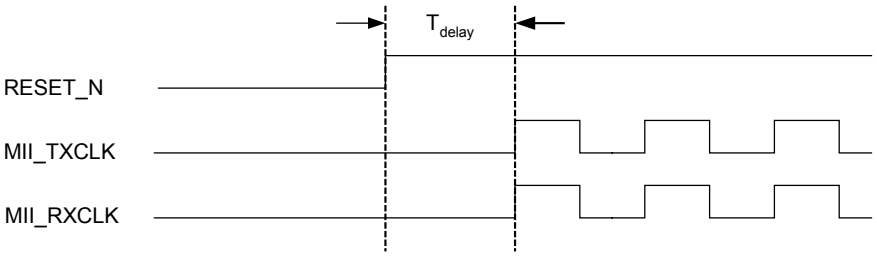
Symbol	Specific Name	Condition	Min	Max
V_{IH}	Input High Vol.		0.5*Vcc	Vcc+0.5V
V_{IL}	Input Low Vol.		-0.5V	0.3*Vcc
V_{OH}	Output High Vol.		0.9*Vcc	Vcc
V_{OL}	Output Low Vol.			0.1*Vcc
I_{OZ}	Tri-state Leakage	Vout=Vcc or GND		
I_{IN}	Input Current	Vin=Vcc or GND		
Icc	Average Operating Supply Current	Iout=0mA		200mA
PECL V_{IH}	PECL Input High Vol		Vdd-1.16V	Vdd-0.88V
PECL V_{IL}	PECL Input Low Vol.		Vdd-1.81V	Vdd-1.47V
PECL V_{OH}	PECL Output High Vol.		Vdd-1.02V	

PECL V_{OL}	PECL Output Low Vol.			Vdd-1.62V

7.2 AC Characteristic

7.2.1 Pin Reset and Clock output timing relationship

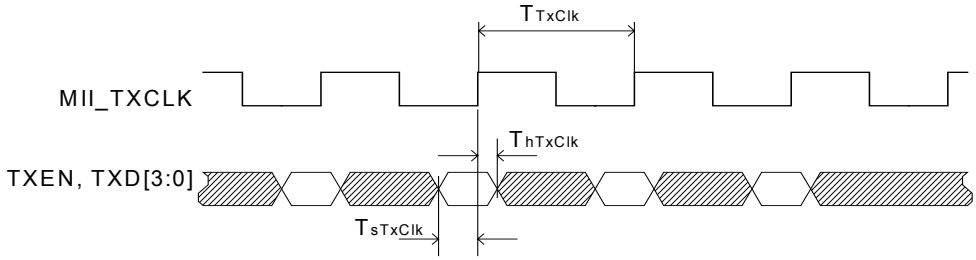
Symbol	Description	Min.	Typ.	Max.	Unit
T_{delay}	Delay time after reset to clock output	-	2.5	-	ms



7.2.2 MII Timing

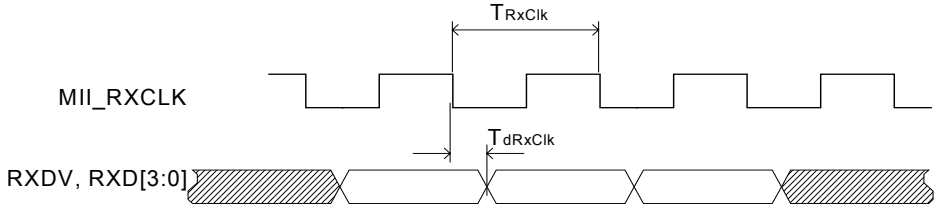
a. Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100M MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10M MII	-	400	-	ns
T_{sTxClk}	TXEN, TXD to MII_TXCLK setup time	2	-	-	ns
T_{hTxClk}	TXEN, TXD to MII_TXCLK hold time	0.5	-	-	ns



b. Receive Timing

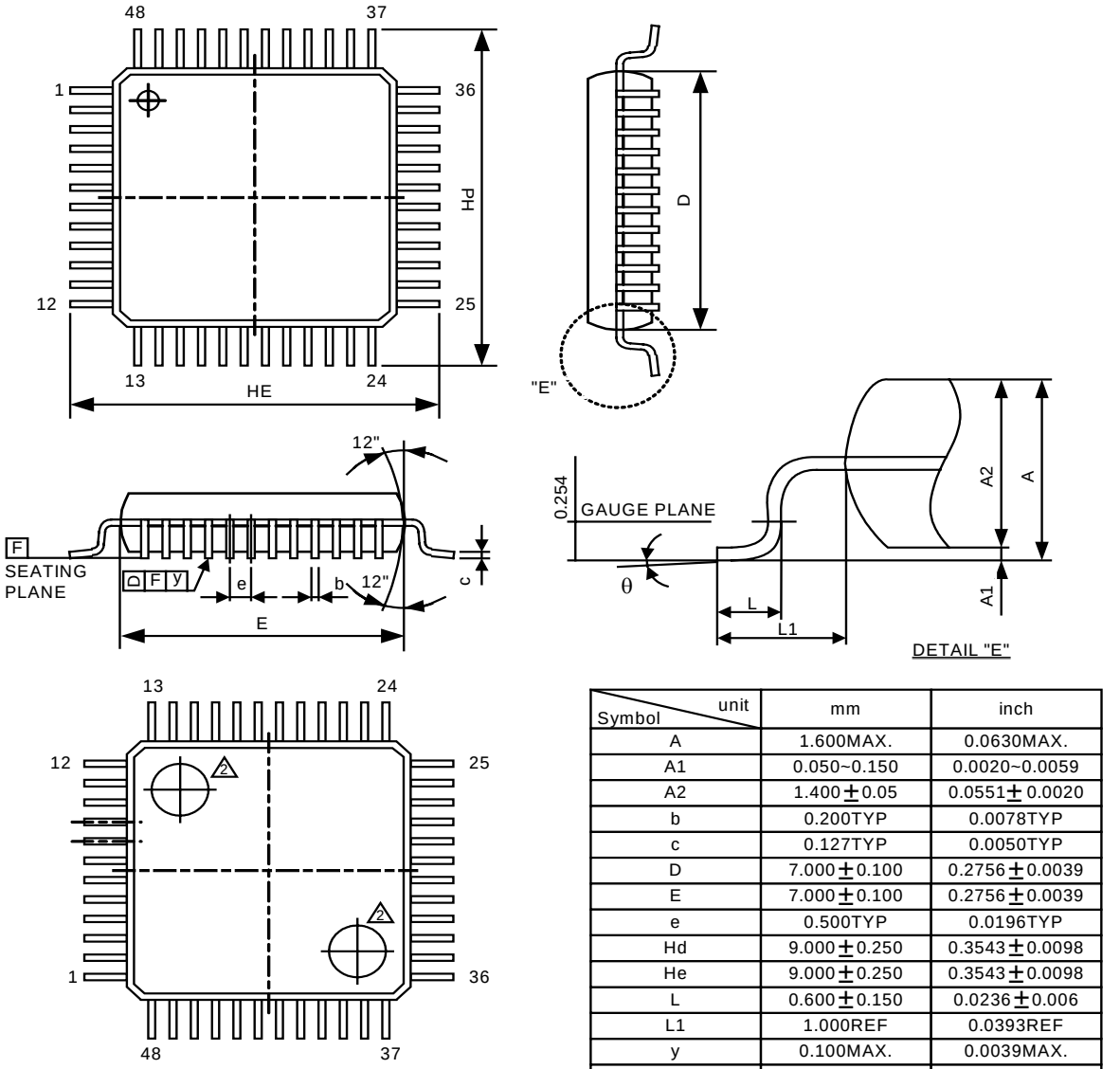
Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100M MII	-	40	-	ns
T_{RxClk}	Receive clock period 10M MII	-	400	-	ns
T_{dRxClk}	MII_RXCLK falling edge to RXDV, RXD	1	-	4	ns



8 Order Information

Part No.	Package	Notice
IP101	48-PIN LQFP	-
IP101 LF	48-PIN LQFP	Lead free

Package and Mechanical Specification



Symbol \ unit	mm	inch
A	1.600MAX.	0.0630MAX.
A1	0.050~0.150	0.0020~0.0059
A2	1.400±0.05	0.0551±0.0020
b	0.200TYP	0.0078TYP
c	0.127TYP	0.0050TYP
D	7.000±0.100	0.2756±0.0039
E	7.000±0.100	0.2756±0.0039
e	0.500TYP	0.0196TYP
Hd	9.000±0.250	0.3543±0.0098
He	9.000±0.250	0.3543±0.0098
L	0.600±0.150	0.0236±0.006
L1	1.000REF	0.0393REF
y	0.100MAX.	0.0039MAX.
θ	0"~7"	0"~7"

Notes:
1. DIMENSION D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION / INTRUSION.
3. MAX. END FLASH IS 0.15MM.
4. MAX. DAMBAR PROTRUSION IS 0.13MM.
GENERAL APPEARANCE SPEC SHOULD BE BASED ON FINAL VISUAL INSPECTION SPEC.

IC Plus Corp.

Headquarters
10F, No.47, Lane 2, Kwang-Fu Road, Sec. 2,
Hsin-Chu City, Taiwan 300, R.O.C.
TEL : 886-3-575-0275 FAX : 886-3-575-0475
Website : www.icplus.com.tw

Sales Office
4F, No. 106, Hsin-Tai-Wu Road, Sec.1,
Hsi-Chih, Taipei Hsien, Taiwan 221, R.O.C.
TEL : 886-2-2696-1669 FAX : 886-2-2696-2220