# 18-port 10/100Mbps Smart Switch Controller

## Features

- Embeds 1.5 Mb packet buffer
- Handles up to 4K MAC address entries
- Supports non-blocking wire speed operation
- Provides 16-port SS-SMII and 2-port MII
- Supports 2 ports selectable normal MII, reverse MII
- All I/O signals can operate at 3.3V or 1.8V.
- Supports up to 18 port based VLAN group
- Supports 256 levels of data rate control
- Captures BPDU, IGMP and OSPF …packet and forward to the CPU port.
- Suppress/enable per port address learning.
- Embeds two levels of priority queues for VLAN tag, physical port and IP Differentiated Service.
- Supports flexible port trunking configuration: up to 3 groups and up to 4 ports for each group
- Embeds an internal regulator controller to simplify the system design.
- Power supply: 1.8V for core logic; optional 3.3V or 1.8V for I/O.
- 128 pin QFP package
- Adjustable I/O driving capability
- Support packet length up to 1536 Bytes
- Spanning Tree state support.
- Supports 3 kinds of port mirrioring methods
- HOL blocking prevention
- Only one 25MHz crystal needed
- Broadcast storm control support
- Programmable MAC address table through 2 serial pins.
- Support Lead Free package (Please refer to the Order Information)

## General Description

Supporting 16-port SS-SMII, 2-port MII and various advanced features, the IP1718 LF fits both the office switch and the ETTH( Ethernet to the Home) application. The IP1718 LF embeds internal SSRAM for the use of the packet buffer and the MAC address table. Besides the traditional switch functions, the IP1718 LF provides the easy-to-design solution, fitting the requirement of most switch application.

The IP1718 LF also supports some features which can simplify the customer's design from the viewpoint of the system. The embedded regulator controller can reduce the component number on the system board. The web management can be easily accomplished by adding an external CPU with protocol stack. All the I/O pins can operate at 3.3V or 1.8V, providing more design flexibility for power supply distribution.

The IP1718 LF embeds 1.5Mb internal packet buffer and stores up to 4K MAC address entries, making it suitable for the generic switch application. In addition, the IP1718 LF supports a wide range of data rate for both egress and ingress, which is useful in the ETTH(Ethernet to the Home) application. The higher layer data packet such as BPDU, IGMP, OSPF can be forwarded to either the 17th or 18th (CPU) port. The flexible trunk configuration allows the user to scale the switch interconnection bandwidth. When the port mirroring function is enabled, the data traffic on the source port will be forwarded to a specified destination port, making the switch administration easier. Supporting up to 18 port based VLAN groups, the IP1718 LF can be configured to fit various traffic partitions. The CoS function is accomplished by configuring the priority of the physical port, the 802.1Q VLAN tag and IP DSCP(Differentiated Service Code Point). In order to fit the application of some special environment, the address learning and the MAC address table aging can be disabled.

## Table Of Contents

**Revision History**

| Revision # | Change Description |
|---|---|
| IP1718 LF-DS-R01 | Initial release. |
| IP1718 LF-DS-R02 | Functions for pin 117 & pin 119 are re-defined. The register 2 description is revised. Revise the timing chart of SCPUIO and the SCPUC. |
| IP1718 LF-DS-R03 | Revised the pin diagram. Revise the pin description of pin 50, pin 53, pin 107 ~ pin 112. Add pin description of the pin 97. |
| IP1718 LF-DS-R04 | Revise the pin diagram. Revise the pin description for pin 89, pin 90, pin 105 and pin 106. |
| IP1718 LF-DS-R05 | Add the order information for lead free package. Update page 25, (6DH) |

# 1 Pin Diagram

IP1718 LF

Top pins (left to right, 102–65):
GND (102), VDD33 (101), M2RXD1 (100), M2RXD0 (99), M2RXDV (98), CLK25M (97), M1COL (96), M1TXEN (95), Port4_Pri_ON/M1TXD3 (94), Port3_Pri_ON/M1TXD2 (93), Port2_Pri_ON/M1TXD1 (92), Port1_Pri_ON/M1TXD0 (91), M1TXC (90), M1RXC (89), M1RXD3 (88), M1RXD2 (87), M1RXD1 (86), M1RXD0 (85), M1RXDV (84), VDD33 (83), GND (82), GND (81), VDD18 (80), CPU_DA (79), CPU_CL (78), INT (77), EEDAT (76), EECLK (75), SCAN_MODE (74), IO_PWR (73), RESET (72), X2 (71), X1 (70), GND (69), VDDPLL (68), REG18 (67), VDD33 (66), GND (65)

Left pins (top to bottom, 103–128):
- 103 M2RXD2
- 104 M2RXD3
- 105 M3RXC
- 106 M2TXC
- 107 M2TXD0/Port5_Pri_ON
- 108 M2TXD1/Port6_Pri_ON
- 109 M2TXD2/WRR_Ration_Set0
- 110 M2TXD3/WRR_Ration_Set1
- 111 M2TXEN
- 112 M2COL
- 113 GND
- 114 VDD18
- 115 VDD33
- 116 GND
- 117 P1TXD/1st MII_Force_Link
- 118 P1RXD
- 119 P2TXD/2nd MII_Force_Link
- 120 P2RXD
- 121 P3TXD/IO_Slew_F
- 122 P3RXD
- 123 P4TXD/IO_Drive0
- 124 P4RXD
- 125 RXSYNC1
- 126 TXSYNC1
- 127 TXCLK1
- 128 P5TXD/IO_Drive1

Right pins (top to bottom, 64–39):
- 64 GND
- 63 Fast_Test_ON
- 62 GND
- 61 IP_Pri_ON
- 60 GND
- 59 TAG_Pri_ON
- 58 GND
- 57 VDD18
- 56 GND
- 55 GND
- 54 PBDU_Bcast_OFF
- 53 N.C
- 52 VDD33
- 51 GND
- 50 N.C
- 49 GND
- 48 GND
- 47 Trunk0_ON1
- 46 GND
- 45 Trunk0_ON0
- 44 GND
- 43 Home_VLAN_ON
- 42 GND
- 41 Aging_OFF
- 40 GND
- 39 VDD33

Bottom pins (left to right, 1–38):
GND (1), VDD33 (2), GND (3), VDD18 (4), RXCLK1 (5), P5RXD (6), P6TXD/MII 1_Link_CPU (7), P6RXD (8), P7TXD/MII 2 Link CPU (9), P7RXD (10), P8TXD/MII 1_Rev_MII (11), P8RXD (12), MDC (13), MDIO (14), P9TXD/MII 2_Rev_MII (15), P9RXD (16), P10TXD/Test_Mode0 (17), P10RXD (18), P11TXD/Test_Mode1 (19), P11RXD (20), P12TXD (21), P12RXD (22), VDD33 (23), GND (24), RXSYNC2 (25), TXSYNC2 (26), TXCLK2 (27), P13TXD/F_Ctrl_OFF (28), RXCLK2 (29), P13RXD (30), P14TXD/BKP_OFF (31), P14RXD (32), P15TXD/BCST_Ctrl_ON (33), P15RXD (34), P16TXD/A (35), P16RXD (36), VDD18 (37), GND (38)

## 2 Block Diagram

## 3    Pin description

| Type | Description |
|------|-------------|
| P | Positive power or ground |
| I; O | I: Input pin; O:Output pin |
| IL | Input latched upon reset |

| Type | Description |
|------|-------------|
| PD, | PD:Pulled down with internal resistor |
| PU | PU:Pulled up with internal resistor |
| I/O | Bi-direction Input/Output |

| Pin No. | Label | Type | Description |
|---------|-------|------|-------------|
| **SS-SMII** | | | |
| 117, 119 121, 123, 128, 7, 9, 11, 15, 17, 19, 21, 28, 31, 33, 35, | P1TXD, P2TXD, P3TXD, P4TXD, P5TXD, P6TXD, P7TXD, P8TXD, P9TXD, P10TXD, P11TXD, P12TXD, P13TXD, P14TXD, P15TXD, P16TXD, | O | SS-SMII transmit data output for port 1 to port 16. |
| 126, 26, | TXSYNC1, TXSYNC2, | O | SS-SMII synchronization output for transmit data |
| 127, 27, | TXCLK1, TXCLK2, | O | SS-SMII transmit clock output |
| 118, 120, 122, 124, 6, 8, 10, 12, 16, 18, 20, 22, 30, 32, 34, 36, | P1RXD, P2RXD, P3RXD, P4RXD, P5RXD, P6RXD, P7RXD, P8RXD, P9RXD, P10RXD, P11RXD, P12RXD, P13RXD, P14RXD, P15RXD, P16RXD, | I | SS-SMII receive data input |
| 42, 44, 46, 48, 56, 60, 62, 64 49, 55 | GND | I | Should be tied to GND. |
| 125, 25, | RXSYNC1, RXSYNC2, | I | SS-SMII receive synchronization input |
| 5, 29, | RXCLK1, RXCLK2, | I | SS-SMII receive clock input |

**Pin description** (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **MII/Reverse MII** | | | |
| 95 | M1TXEN | O | 1st MII (port 17) transmit enable |
| 94, 93, 92, 91 | M1TXD[3:0] | O | 1st MII (port 17) transmit data output |
| 84 | M1RXDV | I | 1st MII (port 17) receive valid |
| 88, 87, 86, 85 | M1RXD[3:0] | I | 1st MII (port 17) receive data input |
| 90 | M1TXC | I/O | 1st MII (port 17) transmit clock. Input for normal (MAC mode) MII. Output for reverse (PHY mode) MII |
| 89 | M1RXC | I/O | 1st MII (port 17) receive clock. Input for normal (MAC mode) MII. Output for reverse (PHY mode) MII. |
| 111 | M2TXEN | O | 2nd MII (port 18) transmit enable |
| 110,109,108,107 | M2TXD[3:0] | O | 2nd MII (port 18) transmit data output |
| 98 | M2RXDV | I | 2nd MII (port 18) receive valid |
| 104,103,100,99 | M2RXD[3:0] | I | 2nd MII (port 18) receive data input |
| 106 | M2TXC | I/O | 2nd MII (port 18) transmit clock. Input for normal (MAC mode) MII. Output for reverse (PHY mode) MII |
| 105 | M2RXC | I/O | 2nd MII (port 18) receive clock. Input for normal (MAC mode) MII.   Output for reverse (PHY mode) MII. |
| 112 | M2COL | I/O | 2nd MII (port 18) collision input. Input for normal MII Output for reverse MII |
| 13 | MDC | O | Clock for serial management bus. It's recommended to add a 30pf capacitor to ground for noise filetrring. |
| 14 | MDIO | I/O | I/O data for serial manment bus. It's recommended to add a 4.7K pull up resistor connecting to VDD and a 30pf capacitor connecting to ground. |
| **Miscellaneous** | | | |
| 70 | X1/OSCI | I | Crystal/ Oscillator 25MHz input |
| 71 | X2 | O | Crystal output |
| 72 | RESETB | I | System reset (low active). Should be kept at "low" for at least 10 microseconds. |
| 97 | CLK25M | O | This output pin is 25MHz clock signal which is the counterpart of the clock generated by the X'tal placed on X1 & X2. |
| 75 | SCL | O, PU | Serial EEPROM clock output |
| 76 | SDA | I/O,PU | Serial EEPROM data |
| 78 | SCPUC | I, PU | Serial CPU access clock input. Please see the section of "Programming the Internal Register" for the usage of SCPUC and SCPUIO. |
| 79 | SCPUIO | I/O, PU | Serial CPU data |
| 77 | INTB | O, PU | Interrupt output. Active low. |
| 74 | TEST | O, PD | Test mode control. |

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| 73 | IO_PWR | I | Power selection for I/O pad. 0:1.8V; 1:3.3V. |
|---|---|---|---|
| 67 | REG18 | O | 1.8V regulator control. This pin can be connected to the base of the PNP transistor to generate the 1.8V power. |
| 50, 53 | N.C | | Reserved for IC test. Leave it unconnected in application. |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **Power & Ground** | | | |
| 68 | VDDPLL | P | 1.8V Power for PLL |
| 69 | GNDPLL | P | Ground for PLL |
| 4,37,57,80,114 | VDD18 | P | 1.8V Power for Core circuit |
| 3,38,58,81,113 | GND18 | P | Ground for core circuit |
| 2,23,39,52,66,83,101,115 | VDD33 | P | 3.3/1.8V Power for I/O PAD |
| 1,24,40,51,65,82,102,116 | GND33 | P | Ground for I/O PAD |
| **Power On setting. These pins' state will be latched upon reset** | | | |
| 117 | 1st MII_Force_Link | IL, PU | This pin is pulled up internally. Connecting a pull down resistor to this pin will force the 1st MII linking to the external device regardless of the PHY polling status, |
| 119 | 2nd MII_Force_Link | IL, PU | This pin is pulled up internally. Connecting a pull down resistor to this pin will force the 2nd MII linking to the external device regardless of the PHY polling status, |
| 121 | IO_SLEW | IL, PD | Output PAD slew rate setting. 1: fast, 0: normal (Default) |
| 128, 123 | IO_DRIVE[1:0] | IL, PD | Output PAD driving current capability<br>00 : 4mA (Default)<br>01 : 8mA<br>10 : 12mA<br>11 : 16mA |
| 7 | MII 1_LINK_CPU | IL, PD | 1st MII (port 17) linked to CPU.<br>1: 1st MII is connected to CPU.<br>0: 1st MII is the normal port (Default) |
| 9 | MII 2_LINK_CPU | IL, PD | 2nd MII (port 18) linked to CPU.<br>1: 2nd MII is connected to CPU.<br>0: 2nd MII is the normal port (Default) |
| 11 | MII 1_REV_MII | IL, PD | 1st MII (port 17) is reverse MII interface<br>1: Reverse MII; 0:Normal MII (Default). |
| 15 | MII 2_REV_MII | IL, PD | 2nd MII (port 18) is reverse MII interface.<br>1: Reverse MII; 0:Normal MII (Default). |
| 19,17 | TEST_MODE[1:0] | IL, PD | Reserved for IC test. |
| 21 | IPG_COMP_EN | IL, PD | Transmit IPG compensation (+80ppm)<br>1: Enable; 0: Disable (Default) |
| 28 | FCTRL_OFF | IL, PD | Disable the full duplex flow control of all ports<br>1: Disable; 0: Enable (Default) |
| 31 | BKP_OFF | IL, PD | Disable the half duplex backpressure control of all ports.<br>1: Disable; 0: Enable (Default). |
| 33 | BCST_CTRL_EN | IL, PD | Enable the broadcast storm control<br>1: Enable; 0: Disable (Default) |
| 35 | AUTO_OFF_FC | IL, PD | 1: Auto turn off the flow control, when the flow control and the priority is enabled.<br>0: Flow control works normally (Default) |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---------|-------|------|-------------|
| **Power On setting. These pins will be latched upon reset** (continued) | | | |
| 41 | AGING_OFF | IL, PD | Disable the MAC address table aging function<br>1: Disable; 0: Enable (Default) |
| 43 | HOME_VLAN_EN | IL, PD | 1: Enable the home VLAN setting :<br>Port 1 ~ Port16 are all individual VLAN shared with 2 MII ports. For example, Port 1, port 17 and port 18 form a VLAN group, etc.<br>1: Enable; 0: Disable (Default) |
| 47, 45 | TRUNK_0_ON[1:0] | IL, PD | The trunk group 0 setting:<br>00 : no trunk (Default)<br>01 : port 1, 2 trunk-grouped<br>10 : port 1, 2, 3 trunk-grouped<br>11 : port 1, 2, 3, 4 trunk-grouped |
| 54 | BPDU_BCST_OFF | IL, PD | Filter the packet with MAC destination address 01-80-c2-00-00-03~01-80-c2-00-00-0F<br>0 : Broadcast (Default)<br>1 : Filter |
| 59 | TAG_PRI_ON | IL, PD | Enable 802.1Q TAG priority function of all ports<br>1:Enable; 0: Disable (Default) |
| 61 | IP_PRI_ON | IL, PD | Enable IP TOS/DS priority function of all ports<br>1: Enable; 0: Disable (Default) |
| 63 | FAST_TEST_MODE | IL, PD | Reserved for IC test. |
| 108,107,94,93, 92,91 | PORT_PRI_ON[5:0] | IL, PD | Enable port base high priority function of port 1~ port 6<br>1: Enable; 0: Disable (Default) |
| 109,110 | WRR_RATIO_SET[1:0] | IL, PD | The ratio of the packet number for the weighted round robin. The switch engine handles both priority queues based on the ratio of the packet number defined below.<br>00 : First in first out (Default)<br>01 : 2/1<br>10 : 4/1<br>11 : 8/1<br>When these bits are set to "00", the CoS priority will be void. |
| 50, 26, 126 | DELAY_SSSMII[2:0] | IL, PD | The delay time of SS-SMII transmit data<br>delay_sssmii[0] : port 1~ port 8<br>delay_sssmii[1] : port 9~ port 16<br>delay_sssmii[2] : reserved<br>1: 4ns delay; 0: no delay(Default) |

**Note:**
1. All the trapped pins are latched upon reset and are pulled down or pulled up by a 50K resistor inside the chip.
2. The designer can connect a 4.7K ohms resistor to set these pins to "1" or "0" to change the default state.
3. The content of an EEPROM will override the pin setting.

## 4    Functional Description

### 4.1    Medium Access Control(MAC)

#### 4.1.1  Data Rate Control

The IP1718 LF implements a sophisticated data rate control mechanism, which is very useful for the bandwidth-limited network. By controlling both the ingress data rate and the egress data rate, the IP1718 LF provides a variety of the bandwidth configuration.

By means of calculating the maximum TX/RX byte number in a time unit of the corresponding port, the IP1718 LF provides a precise bandwidth control mechanism. The formula for calculating the maximum byte during a time unit is:

$$M.B.N= S.D.R* 512$$

Where M.B.N stands for the maximum byte number;    S.D.R the specified data rate.
The time unit is 10ms at 100 Mbps speed and 100ms at 10Mbps speed.
The data rate for each port is specified in registers ranging from 03H to 12H and 1BH ~ 1CH.

If the transmit/receive byte number reaches the specified M.B.N after the transmit/receive timer expires, the MAC will continue the operation until the whole data packet is transmitted/received and then wait until the next time unit starts.

For example, if the value set to register 06H is 12H(18 in decimal) and the port 1 runs at 100Mbps speed, the maximum byte number allowed to transmit through port 1 is 9216 bytes(the result of 512*18) within 10ms( 1,000,000 bit time). 9216 bytes stands for 73,728 bit time. The flow control mechanism will be activated for the spare time. Thus the data rate can be limited to a specified value.

#### 4.1.2  Flow Control

The IP1718 LF embeds the flow control mechanism for both full duplex mode and half duplex mode. When the buffer reach a pre-defined level, the transmit MAC will generate the flow control pattern to prevent the buffer overflow. These flow control patterns are dependent on the duplex mode. The IP1718 LF transmit MAC generates the backpressure pattern in half duplex mode and the 802.3x pause packet in full duplex mode.

When operating in half duplex mode, the IP1718 LF should comply with CSMA/CD standard. The transmit MAC will generate the jam pattern to inform the link partner that the receive buffer is not available when the buffer reaches a pre-defined level. The IP1718 LF supports the collision_based backpressure. When the collision_based backpressure is enabled, the transmit MAC of the IP1718 LF will generate the jam pattern only when the link partner is transmitting data and the buffer is not available. When detecting the collision on line, the link partner will back off the transmission and then wait until the back off time expires.

The IP1718 LF uses 802.3x pause packet to accomplish the flow control for full duplex mode. When the buffer reach a pre-defined level, the transmit MAC generates a Xoff pause packet immediately or right after the current packet has been transmitted. When receiving a pause packet, the link partner will stop the transmission for a time period according to the pause value carried by the pause packet, preventing the internal buffer from overrun.

## 4.2 Switch Engine and Queue Management

### 4.2.1 Store & Forward Mechanism

The IP1718 LF utilizes the "store & forward" method to handle the switch engine. Each data packet will not be forwarded to the destination port until the entire packet is received. The internal mechanism will check whether the packet is correct. The data packet will be forwarded to the destination port if the packet is correct; otherwise it will be discarded.

Besides the erroneous packet and the 802.3x pause packet are not forwarded. The 802.1D Reserved Group packet with 01-80-c2-00-00-03 ~ 01-80-c2-00-00-0F MAC address can be optionally dropped by setting pin 54 or register 01H.

### 4.2.2 Address Learning and aging time

The address learning function for each port can be either disabled or enabled by setting the corresponding bit in registers 31H and 32H. The overall MAC address capacity is 4096. The aging time can be programmed according to the system requirement, ranging from 30sec to 8400sec +-6.7%.

The IP1718 LF provides two kinks of hash method to store the MAC address table. One is the direct mapping and the other is the CRC-12 algorithm. When the direct mapping method is selected, the IP1718 LF recognizes the least significant 12 bits of the source MAC address. When the CRC-12 algorithm is used, the IP1718 LF executes the following equation to decide the address of the MAC address table.

CRC-12 equation: $X^{12}+X^{11}+X^3+X^2+X+1$

Some source MAC address will be excluded in MAC address table. These data packets are:
- Erroneous packet
- 802.3x pause packet
- 802.1D Reserved Group packet
- Multicast source MAC address

### 4.2.3 Class of Service

The IP1718 LF implements two levels of priority queues, high priority and low priority. The priority for each data packet is based on one of the following schemes: 802.1Q VLAN tag, IP TOS/DS or physical port. Each incoming data packet can be mapped to either one priority. When no CoS function is enabled, the first-in first-out forwarding method is used.

When the CoS for 802.1Q VLAN tag is enabled, the IP1718 LF will recognize 3 bits of precedence carried by the VLAN tag and map it to the specified priority. The data precedence 0 to 3 will be treated as low priority packet, and the packet with other values will be stored in high priority queue. Setting register 25H and 26H to "1" will enable the CoS function for the corresponding port. The LSB of both registers controls the lowest port ID for that group. For example, the bit 0 of register 25H corresponds to port 1.

The IP1718 LF provides the IP layer CoS function by recognizing the DSCP(Differentiated Service Code Point) Octet and mapping it to the specified priority. For IPv4 packet, DSCP is embedded in the TOS(type of Service) Octet. For a IPv6 data packet, the Traffic Class Octet can be used to differentiate the Class of Service. When this function is enabled, the IP1718 LF will automatically recognize the IP version and capture the either the TOS field(IPv4) or Traffic Class(IPv6). The following tables show the location of DSCP in a packet.

| Destination MAC Address(6 bytes) | Source MAC Address(6 bytes) | 0800H | IP version = 0100b(4 bits) | IHL(4 bits) | TOS(8 bits). IP1718 LF maps TOS[5:0] to 2 levels of |
|---|---|---|---|---|---|

| | | | | | priority. |
|---|---|---|---|---|---|

**Table 4.1 IPv4 Data Format**

| Destination MAC Address(6 bytes) | Source MAC Address(6 bytes) | 0800H | IP version = 0110b(4 bits) | Traffic Class(8 bits). IP1718 LF maps TC[5:0] to 2 levels of priority. |
|---|---|---|---|---|

**Table 4.2 IPv6 Data Format**

| | **High Priority** | **Low Priority** |
|---|---|---|
| 802.1Q VLAN tag Precedence | 3'b100 ~ 3'b111 | 3'b000 ~ 3'b011 |
| IPv6 Traffic Class Field & IPv4 TOS | 6'b101110; 6'b001010; 6'b010010; 6'b011010; 6'b100010; 6'b11x000 | Other values |

**Table 4.3   Forwarding Priority for IP DS and 802.1Q VLAN tag**

The IP TOS/DS priority configuration can be set through enabling the corresponding register, ranging from 27H to 28H.

The port based priority only concerns the physical port location in a switch. By enabling the CoS function of the corresponding bit in registers 23H and 24H, the IP1718 LF can set each physical port to a "high" priority.

Please note that for those three CoS functions, the LSB (Least Significant Bit) of the registers corresponds to the low physical port number for that group.

A data packet dropping mechanism is implemented to prevent the buffer from overrun. Once the packet buffer reach a specified level, the data packet assigned to the low priority will be dropped to reserve the buffer space for the high priority data packet.

When multiple CoS schemes are enabled, the data packet is treated as the high priority as long as any one of three CoS schemes is mapped to "high".

Take the following example for detailed explanation.

If port 3 is set as a low priority port and it receives a data packet which embeds VLAN tag with high priority and IP DS field with low priority, this data packet will be forwarded in a high priority. In the other word, the priority of a data packet would be set to high if any of three CoS schemes is interpreted as the high priority.

### 4.2.4  Port_based VLAN

The IP1718 LF provides various port_based VLAN configurations. The overall number of VALN groups that the IP1718 LF can support is 18. The IP1718 LF implements two registers to describe the routing table for each port. Thus the total number of registers which defines the port_based VLAN is 52.

Take the following example for the detailed description. The data incoming from port 1 will be forwarded to the corresponding port defined in register 34H and 35H. Similarly, the forwarding rule for the data incoming from port 2 will refer to the register 36H and 37H.

**Note:** The port ID is counted from 1 to 18.

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### 4.2.5 Trunk Channel

Supporting up to 3 trunk channels, the IP1718 LF provides a versatile configurations that fit many applications. Each trunk channel may comprise 2 to 4 ports. The traffic of the destination port passing through the trunk channel is defined by the registers 68H to 6AH. The hash algorithm from which the IP1718 LF derives the trunk ID is specified by registers 2FH. The result calculated by the hash algorithm is mapped to the trunk ID. A physical port can forward the trunk traffic only when the trunk ID decided by hash algorithm matches the setting of the Trunk Configuration register. The following table describes the traffic distribution rule.

**The Behavior for Each Port in a Trunk**

| Result of the Hash Algorithm | Trunk Channel Configuration | Behavior of the Member of Trunk |
|---|---|---|
| 2'b00 | 4'bXXX1 | Forward the data through the first port of this group |
| | 4'bXXX0 | Do not forward the data through the first port of this group |
| 2'b01 | 4'bXX1X | Forward the data through the second port of this group |
| | 4'bXX0X | Do not forward the data through the second port of this group |
| 2'b10 | 4'bX1XX | Forward the data through the third port of this group |
| | 4'bX0XX | Do not forward the data through the third 7 port of this group |
| 2'b11 | 4'b1XXXX | Forward the data through the fourth port of this group |
| | 4'b0XXXX | Do not forward the data through the fourth port of this group |

There are four ports for each trunk and each port can be configured to fit the trunk traffic as depicted above.

### 4.2.6 Port Mirroring

There are some circumstances that the network administrator requires to monitor the network status. The port mirroring function can help the network administrator diagnose the network.

A port mirroring function can be accomplished by assigning a monitored port(source port) and a snooping port (destination port). The IP1718 LF supports three kinks of mirroring methods: the ingress, the egress and ingress plus egress. This function can be enabled by programming the corresponding bit in registers 6BH to 6DH.

Registers 6BH and 6CH defined the port which will be monitored(mirroring source). The register 6DH specifies the port which will snoop( mirroring destination) and the mirroring method.

### 4.2.7 Queue Management

The IP1718 LF supports three kinds of priority management: The first in first out, the strict priority and the weighted-round-robin.

The first in first out method will override the CoS setting and is not recommended when the CoS function is enabled. When the strict priority is enabled, the data packets stored in low priority queue will not be sent out until all data packets in high priority queue are sent out. When the weighted round robin function is enabled, the IP1718 LF will send the data packet in an order switching between high priority queue and low priority queue with ratio defined by pin 109,110 setting (without EEPROM) or Register 2CH(with EEPROM/CPU)

### 4.2.8  Broadcast Storm Control

To prevent the broadcast storm, the IP1718 LF implement a broadcast storm control mechanism. When this function is enabled, the IP1718 LF will monitor the number of the broadcast packet and take the proper action to prevent the broadcast packet from reaching the pre-defined buffer level. The behavior of the broadcast packet is dependent on the operating mode of the IP1718 LF.

- Drop the data when the flow control is disabled

### 4.2.9  Handling the Higher Layer Protocol

The IP1718 LF can handle two categories of data packet, the configuration related and the TCP/IP related. The configuration-related protocol concerns the network configuration such as, the VLAN group, the link aggregation and the spanning tree. Unlike the configuration-related protocol, the TCP/IP related data has nothing to do with the network.

Four forwarding schemes can be selected to handle the protocol mentioned above, dropping the packet, sending to a specified port(commonly connected to a CPU), sending to a group of ports and broadcasting to all ports. The protocol handling scheme is programmed by writing the corresponding bit in register 02H.

### 4.2.10  Port Security

In some cases, it is required to disable the address learning mechanism and specify the MAC address. This function is useful for the application which will prevent the unauthorized user from intruding the network. The typical application is the Ethernet to the Home(ETTH).

Programming the registers 31H and 32H will enable/disable the address learning function. The LSB of the register 31H corresponds port 1.

The register 33H handles the forwarding rule. A data packet will be either forwarded or dropped depending on the setting of this register.

## 5    System Operation

### 5.1    Reset and EEPROM Download Procedure

The reset input should be kept at "0" for more than 1.6 microsecond after power up. After detecting the rising edge of reset input, the IP1718 LF will start downloading the content of EEPROM(acting like an EEPROM master).

The internal register address of the IP1718 LF should comply with the address of EEPROM. Being an EEPROM master, the IP1718 LF will download the content of EEPROM with EEPROM ID "1726H".

The mapping relationship between the IP1718 LF registers and the EEPROM address are depicted as the following table.

| EEPROM address | EEPROM content | IP1718 LF Register |
|---|---|---|
| 00H | 17H | XX |
| 01H | 26H | XX |
| 02H | Expected value | 01H[15:8] |
| 03H | Expected value | 01H[7:0] |
| 04H | Expected value | 02H[15:8] |
| 05H | Expected value | 02H[7:0] |
| •••••• | •••••• | •••••• |
| •••••• | •••••• | •••••• |
| FCH | Expected value | 7EH[15:8] |
| FDH | Expected value | 7EH[8:0] |

**Note:**
1.    The EEPROM ID should be set to "3'b000"; i.e. A2=0; A1=0; A0=0
2.    The IP1718 LF download the content of the EEPROM ranging from address 00H to FDH; i.e. the register beyond this range is not recognized by the IP1718 LF.
3.    The ID for IP1718 LF recognition should be set at address 00H and address 01H as stated in the table.

### 5.2    Polling/Writing the PHY

The IP1718 LF periodically, around 2.8ms for each access cycle, read the status of the PHY through MDC, MDIO management signals. The PHY registers that will be read/write are 0, 1, 4 and 5. After reading the PHY status, the IP1718 LF will reconfigure the internal MAC to meet the operating mode of the PHY.

The relationship between the port ID and the PHY ID is shown below.

| IP1718 LF Port ID | Port 1 to Port 24 | Port 17 | Port 18 |
|---|---|---|---|
| **PHY ID** | address 8 to address 31 | address 4 | address 5 |
| **Comment** | The smallest ID of the IP1718 LF corresponds to the smallest PHY ID. | | |

**Table 5.1 The Relationship between PHY ID and the IP1718 LF Port ID**

The IP1718 LF can be enforced to run at a specified mode without referring to the PHY status. When enforced, the IP1718 LF will write the forced mode to the corresponding PHY through MDC/MDIO and poll the link status of PHY. Care should be taken that the operating mode in both MAC side and PHY side should be consistent.

By programming the register 80H and 81H, the user can easily set the PHY register to a specified value. Since the MDC runs at 2.5 Mhz clock speed, the CPU should check whether the current command has been completed or not before issuing the next command. Bit 13 in the register 80H indicates the progress of the read/write operation.

## 5.3    Programming the Internal Registers

There is no need to program the register of the IP1718 LF for the generic application. However it's probably necessary to program the internal register to fit some special applications. The interface between the IP1718 LF and the CPU is a serial bus which comprises a clock and a I/O signal. Like the access cycle of the serial management interface, the serial interface comprises the device ID, the read/write command, the address and the data. The access cycle is depicted as below.
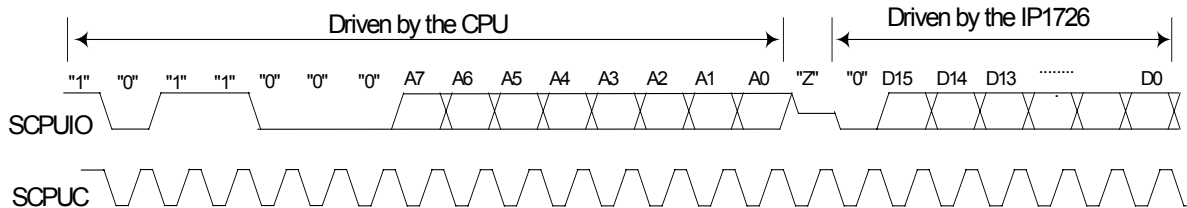

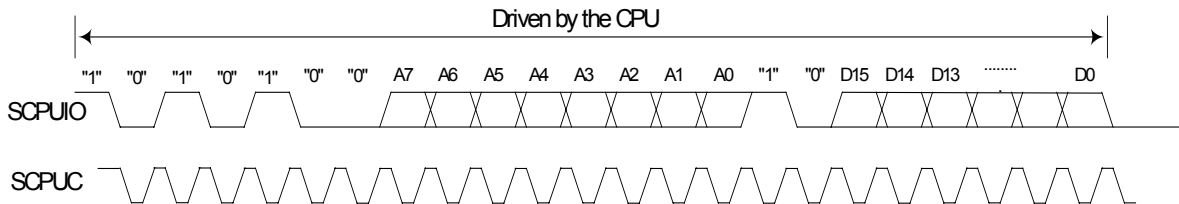
**Fig. 5.1 The CPU read data from the IP1718 LF**



**Fig. 5.2 The CPU write data to the IP1718 LF**

The access cycle is much like the access cycle of MDC, MDIO. Care should be taken that the switch ID is 2-bit wide rather than 5-bit wide.

## 5.4    SS-SMII

The transmitter of the MAC transfers the transmit data to the PHY at the rising edge of TXCLK and the TXSYNC indicates the start of the 10-bit frame. By recognizing the high pulse of the TXSYNC, the PHY can capture the correct transmit data stream. The PHY transfers the receive data to the IP1718 LF in a similar way. The difference is that the signal direction is reverse.

Accompanied by the high pulse of TXSYNC, the TXEN status is present on the TXDATA pin and then the TX-ER status and finally 8-bit data. For the RX part of SS-SMII, the CRS(Carrier Sense) status is present

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on the RXDATA during the high pulse of RXSYNC. The RX_DV(receive data valid) status follows CRS and finally the 8-bit data.

For a given PHY port, the SS-SMII consists of six signals.
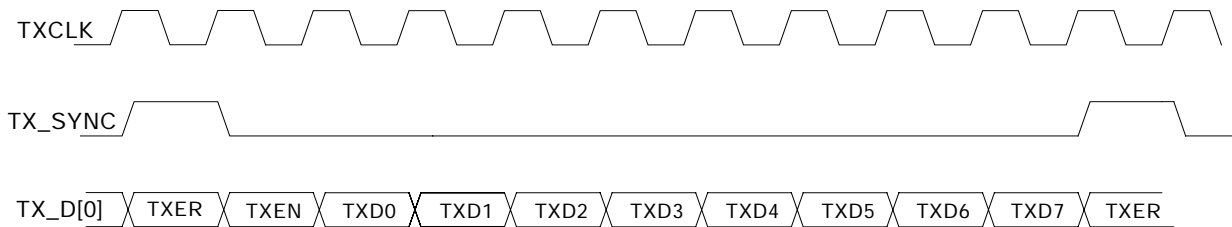RXDATA-one bit data for receiver
TXDATA- one bit data for transmitter
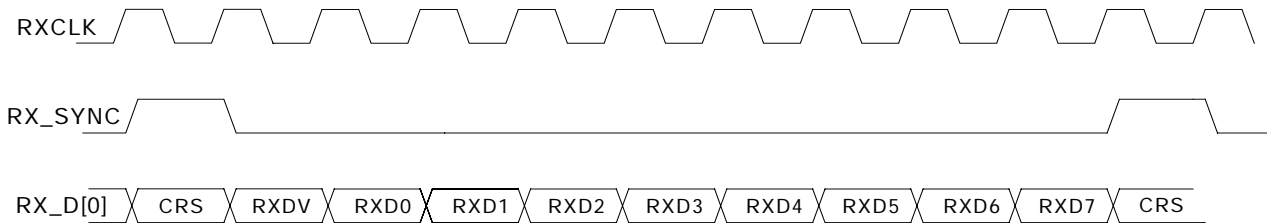TXSYNC- This signal is driven by MAC.
RXSYNC- This signal is driven by PHY.
TXCLK- This signal is driven by MAC
RXCLK- This signal is driven by PHY.

Transmit SS-SMII

Receive SS-SMII

## 6    Register Map

R = Read ; W = Write ; R/W = Read/Write

| Register Address | Register Description | Attribute | Default value |
|---|---|---|---|
| 01H | Half duplex control<br>Bit [0]: Drops the packet that encounters 16 successive collisions.<br>　　　1: Drop; 0: Forward<br>Bit [1]: Collision back off.<br>　　　1: Disable; 0: Enable<br>Bit [2]: Reserved and should be set to "0".<br>Bit [3]: Broadcast BPDU packet.<br>　　　1: Broadcast; 0: Drop<br>Bit [4]: Reserved and should be set to "0".<br>Bit [15]~ Bit 5: Not used. | R/W | 5'h0A |
| 02H | Network configuration packet capture:<br>Bit [0]: Spanning tree.<br>　　　1: Capture & forward to the CPU port.<br>　　　0: Drop.<br>Bit[1]:  In-band  management  packet(Destinatopn  MAC  Address =This Switch MAC Address)<br>　　　1: Capture & forward to the CPU port.<br>　　　0:   Drop<br>**Note:** If this bit is set to "1", the ARP will be sent to CPU port too.<br>Bit[2]: LACP<br>　　　1:<br>　　　　Only forward to the CPU port when register1 bit[3]= 0.<br>　　　　Braodcast to other ports when register1 bit[3]=1<br>　　　0: Drop<br>Bit[3]: GVRP<br>　　　1: Capture & forward to the CPU port only .<br>　　　0: Broadcast<br>IP packet capture<br>Bit[5:4] : ICMP<br>Bit[7:6] : IGMP<br>Bit[9:8] : TCP<br>Bit[11:10] : UDP<br>Bit[13:12] : OSPF<br>Bit[15:14] : Others<br>　　　00 : Send to port 1 ~ port 16 only<br>　　　01 : Send to port 18(CPU) and port 1 ~ port 16<br>　　　10 : Send to port 18(CPU) only<br>**Note:**<br>1.　When the packet capture function is enabled, port 18 should be set to as CPU port.<br>2.　If only one CPU port is required, it's recommedded to set port 18 as the CPU port. | R/W | 16'h0000 |

| Register Address | Register Description | Attribute | Default value |
|---|---|---|---|
| 03H | Egress/Ingress data rate control.<br>Bit[7:0]: Egress data rate control.<br>Bit[15:8]: Ingress data rate control.<br>The maximum ingress/egress byte number in one time unit is.<br>Bit[15:8] * 512 for Ingress<br>Bit[7:0] * 512 for Egress.<br>The one time unit is 10ms for 100Mbps seed and 100ms for 10Mbps speed. | R/W | 16'hffff |
| 04H ~ 12H<br><br>1BH~ 1CH | 04H ~ 12H: Egress/Ingress data rate control for port 2 to port 16.<br>04H register corresponds to port 2.<br>1BH ~ 1CH: Egress/Ingress data rate control for port 17 and port 18.<br>1BH register corresponds to port 17.<br>The definition is the same as that of the register 03H. | R/W | 16'hffff |
| 1DH | Port receive function.<br>1: Enable;<br>0: Disable.<br>Bit 0 corresponds to port 1.<br>Bit 15 corresponds to port 16. | R/W | 16'Hffff |
| 1E | Port receive function.<br>Bit[9:8] 1: Enable; 0: Disable.<br>Bit 8 and bit 9 correspond to port 17 and port 18 respectively. Other bits are reserved. | R/W | 10'h3ff |
| 1FH | MAC reset for port 1 to port 16.<br>0: Activate reset; 1: normal operation.<br>Bit 0 corresponds to port 1.<br>Bit 15 corresponds to port 16. | R/W | 16'hffff |
| 20H | MAC reset for port 17 and port 18.<br>Bit[9:8] 0: Activate reset; 1: normal operation.<br>Bit 8 and bit 9 correspond to port 17 and port 18 respectively. Other bits are reserved. | R/W | 10'h3ff |
| 21H | MAC filters the data frames for port16~pot1, 1 bit per port<br>       0: only control frames are forwarded<br>       1: all good frames are forwarded | R/W | 16'hffff |
| 22H | MAC filters the data frames for port 17 and port 18, 1 bit per port<br>bit[9:8] : 0: only control frames are forwarded<br>       1: all good frames are forwarded<br>Other bits are reserved | R/W | 10'h3ff |
| 23H | Port base priority enable for port16~pot1, 1 bit per port<br>bit[15:0] : 0: This port is set to normal priority<br>       1: This port is set to high priority | R/W | 16'h0 |
| 24H | Port base priority enable for port 17 and port 18, 1 bit per port<br>bit[9:8] : 0: This port is set to normal priority<br>       1: This port is set to high priority<br>Other bits are reserved | R/W | 10'h0 |
| 25H | VLAN Tag based priority enable for port16~pot1, 1 bit per port<br>bit[15:0] : 0: disable<br>       1: enable | R/W | 16'h0 |

| Register Address | Register Description | Attribute | Default value |
|---|---|---|---|
| 26H | VLAN Tag based priority enable for pot17 and port 18, 1 bit per port<br>bit[9:8] :　0: disable<br>　　　　　 1: enable<br>Other bits are reserved. | R/W | 10'h0 |
| 27H | IP DS based priority enable for port16~pot1, 1 bit per port<br>bit[15:0] :　0: disable<br>　　　　　　1: enable | R/W | 16'h0 |
| 28H | IP DS based priority enable for port 17 and pott 18, 1 bit per port<br>bit[9:8] :　0: disable<br>　　　　　 1: enable<br>Other bits are reserved. | R/W | 10'h0 |
| 29H | Switch MAC address[15:0] | R/W | 16'h0 |
| 2AH | Switch MAC address[31:16] | R/W | 16'h0 |
| 2BH | Switch MAC address[47:32] | R/W | 16'h0 |
| 2CH | Out queue schedule mode / weight selection<br>Bit[1:0] :　Schedule mode<br>　　　　　2'b00: First in First out<br>　　　　　2'b01: Strict Priority.<br>　　　　　　The IP1718 LF will always forward all packets with high priority until the packet in the high priority queue is empty.<br>　　　　　2'b10 : WRR. Weighted-and-round-robin scheme.The packet number in both priority queues is based on the defined ratio.<br>　　　　　2'b11 : undefined<br>Bit[4:2] : Low priority queue weight number when the WRR mode is selected<br>Bit[7:5] : High priority queue weight number when the WRR mode is selected.<br><br>**Note:** When Bit[4:2] and Bit[7:5] are set to "000", the weight number will be interpreted as "8". | R/W | 8'd0 |
| 2DH | Reserved for test. Do not access to this register. | R/W | 9'd475 |
| 2EH | Reserved for test. Do not access to this register. | R/W | 9'd500 |

| Register Address | Register Description | Attribute | Default value |
|---|---|---|---|
| 2FH | bit[0] : Hash algorithm selection<br>    0 : CRC mapping<br>    1 : Direct mapping<br>bit[1] : Address table aging function disable<br>    0 : aging function enabled<br>    1 : aging function disabled<br>bit[3:2] : Trunk ID hash algorithm selection<br>    2'b00 : Port ID(the least significant 2 bits of the result of port ID +1);<br>    **Note:** The port ID is counted from 1 to 18.<br>    2'b01 : SA(the least significant 2 bits of the source MAC address)<br>    2'b10 : DA(address bit 16 is mapped to trunk ID[1] and address bit 0 is mapped to trunk ID[0] );<br>    2'b11 : SA XOR DA(the result of the XOR operation described above)<br>bit[4] : Broadcast Strom Control enable<br>    0 : broadcast storm control disabled<br>    1 : broadcast storm control enabled<br>bit[5] : Auto turn on/off flow control when priority queue enable<br>    0 : normal flow control<br>    1 : auto turn on/off flow control<br>bit[6] : Broadcast frames egress is blocked for port 17<br>    0 : Broadcast frames send to port 17<br>    1 : Broadcast frames do not send to port 17<br>bit[7] : Broadcast frames egress is blocked for port 18 | R/W | 8'h0 |
| 30H | bit[7:0] : Aging timer<br>The aging time is about : (aging_timer + 1) x 30.7 +-6.7% sec.<br>bit[14:8] : Broadcast storm control threshold<br>The broadcast frame number allow in one time unit<br>The time period is 1ms for 100M speed<br>The time period is 10ms for 10M speed | R/W | 8'd9<br><br>8h'7f |
| 31H | Enable Source MAC address learning function for port16~1<br>bit[15:0] :  0: disable learning<br>          1: enable learning | R/W | 16'hffff |
| 32H | Enable Source MAC address learning function for port 18~ port 17<br>bit[9:8] : 0: disable learning<br>        1: enable learning | R/W | 10'h3ff |
| 33H | Security configuration<br>bit[0] : Drop the unknown SA frame going to port 18<br>    0 : forward<br>    1 : Drop<br>bit[1] : forward unknown Source MAC address frame when the address learning function is disabled<br>    0 : drop the frame with unknown source MAC addreess<br>    1 : forward the frame with unknown source MAC addreess | R/W | 2'b10 |

| Register Address | Register Description | Attribute | Default value |
|---|---|---|---|
| 34H | VLAN group setting for port 1 (p16~p01)<br>The bit 15 corresponds to port 16 and the LSB corresponds to port 1.<br>0: The data incoming from port 1 is NOT allowed to be forwarded to the corresponding port.<br>1: The data incoming from port 1 is allowed to be forwarded to the corresponding port. | R/W | 16'hffff |
| 35H | VLAN group setting for port 1 (p18~p17)<br>The bit 9 corresponds to port 18 and bit 8 corresponds to port 17. Other bits are reserved.<br>0: The data incoming from port 1 is NOT allowed to be forwarded to the corresponding port.<br>1: The data incoming from port 1 is allowed to be forwarded to the corresponding port. | R/W | 10'h3ff |
| 36H~ 53H | The registers within this range are used to define the VLAN group setting for port 2 to port 16. Like the statement of registers 34H and 35H, two registers comprise the definition of the forwarding rule for a port. | R/W | 16'hffff &10'h3ff |
| 54H~63H | Reserved | | |
| 64H~67H | The registers within this range are used to define the VLAN group setting for port 17 and port 18. | R/W | 16'hffff &10'h3ff |

| Register Address | Register Description | Attribute | Default value |
|---|---|---|---|
| 68H | Trunk group 0 (p4, p3, p2, p1) setting<br>port 1 ~ port 4 are the same trunk group and can be any combination to form a trunk. The trunk ID described below is derived by the algorithm defined in register 2FH.<br>bit[3:0] : trunk configuration for port 01<br>    4'b0000 : the trunk is disabled.<br>    4'bxxx1 : pass the frame with trunk ID = 0<br>    4'bxx1x : pass the frame with trunk ID = 1<br>    4'bx1xx : pass the frame with trunk ID = 2<br>    4'b1xxx : pass the frame with trunk ID = 3<br>bit[7:4] : trunk configuration for port 02<br>bit[11:8] : trunk configuration for port 03<br>bit[15:12] : trunk configuration for port 04<br><br>**Note :** In a trunk group, the configuration should be ORed to 4'b1111 and no more than one port has the same configuration bit.<br><br>**Example 1:**<br>bit[3:0] = 4'b1100,<br>bit[7:4] = 4'b0010,<br>bit[11:8]=4'b0001,<br>bit[15:12]=4'b0000.<br>This configuration stands for the following forwarding rule.<br>Forwarding to port 1 of this group when the hash result defined in register 21H is 3 or 2.<br>Forwarding to port 2 of this group when the hash result defined in register 21H is 1.<br>Forwarding to port 3 of this group when the hash result defined in register 21H is 0.<br>Port 4 is not allowed to forward the data since bit[15:12] is set to 4'b0000.<br><br>**Example 2:**<br>Bit[3:0]=4'b1100, bit[15:12]=4'b1000 is not allowed.<br>When the hash result is 3, the switch can not decide to forward the packet through either port 1 or port 4. | R/W | 16'h0000 |
| 69H | Trunk group 1 (p8, p7, p6, p5) setting<br>port 5 ~ port 8 are the same trunk group and can be any combination to form a trunk<br>bit[3:0] :    trunk configuration for port 05<br>bit[7:4] :    trunk configuration for port 06<br>bit[11:8] :    trunk configuration for port 07<br>bit[15:12] :    trunk configuration for port 08 | R/W | 16'd0 |
| 6AH | Trunk group 2 (port 17, port 18) setting<br>port 17 ~port 18 are the same trunk group<br>bit[3:0] :    trunk configuration for port 17<br>bit[7:4] :    trunk configuration for port 18 | R/W | 8'h00 |

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| Register Address | Register Description | Attribute | Default value |
|---|---|---|---|
| 6BH | Port Mirroring Configuration 0<br>bit[15:0] : p16~p01 monitored port (source port)<br>      0 : this port is not monitored<br>      1 : this port is monitored<br>      The LSB corresponds to port 1. | R/W | 16'h0000 |
| 6CH | Port Mirroring Configuration 1<br>bit[9:8] : p18~p17 monitored port (source port)<br>      0 : this port is not monitored<br>      1 : this port is monitored<br>      The bit 8 corresponds to port 17. | R/W | 10'h000 |
| 6DH | Port Mirroring Configuration 2<br>bit[4:0]   : the snooping port(destination)<br>      5'h0: port 1<br>      ….<br>      ….<br>      5'h15: port 16<br>      5'h19: port 17<br>      5'h1A: port 18<br>bit[6:5] : the port snooping scheme<br>      00 : disabled<br>      01 : egress<br>      10 : ingress<br>      11 : egress/ingress | R/W | 7'd0 |
| 6EH | (Reserved) | | |
| 6FH | CPU read/write MAC address table Configuration<br>bit[11:0] : the 4K SRAM address for MAC address table<br>bit[12] : read/write configuration<br>      0 : read<br>      1 : write<br>bit[13] : 70H data indicator<br>      0 : 70H is the data read from the table<br>      1 : 70H is the data to be written to table<br>bit[14] : read/write enable<br>      0 : No action<br>      1 : read/write table<br>bit[15] : command complete | R/W | 16'h0000 |
| 70H | CPU read/write table Data [15:0]<br>Store the data read from table for read command<br>Store the data to be written to table for write command | R/W | 16'd0 |
| 71H | CPU read/write table Data [31:16]<br>Store the data read from table for read command<br>Store the data to be written to table for write command | R/W | 16'd0 |
| 72H | CPU read/write table Data [45:32]<br>Store the data read from table for read command<br>Store the data to be written to table for write command | R/W | 14'd0 |
| 73H | Auto negotiation for port16~pot1, 1 bit per port<br>bit[15:0] :  0: auto negotiation disabled<br>            1: auto negotiation enabled | R/W | 16'hffff |

| Register Address | Register Description | Attribute | Default value |
|---|---|---|---|
| 74H | Auto negotiation for port18~pot17, 1 bit per port<br>bit[9:8] :   0: auto negotiation disable;     1: auto negotiation enable<br>Other bits are reserved. | R/W | 10'h3ff |
| 75H | Speed setting for port16~pot1, 1 bit per port<br>bit[15:0] :   0: 10Mb<br>            1: 100Mb<br>            The LSB corresponds to port 1. | R/W | 16'hffff |
| 76H | Speed setting for port18~pot17, 1 bit per port<br>bit[9:8] :   0: 10Mb;         1: 100Mb<br>            The bit 8 corresponds to port 17.<br>Other bits are reserved. | R/W | 10'h3ff |
| 77H | Duplex setting for port16~pot1, 1 bit per port<br>bit[15:0] :   0: Half duplex;<br>            1: Full duplex<br>            The LSB corresponds to port 1. | R/W | 16'hffff |
| 78H | Duplex setting for port18~pot17, 1 bit per port<br>bit[9:8] :     0: Half duplex; 1: Full duplex<br>            The bit 8 corresponds to port 17.<br>Other bits are reserved. | R/W | 10'h3ff |
| 79H | Pause setting for port16~pot1, 1 bit per port<br>bit[15:0] :   0: disabled<br>            1: enabled<br>            The LSB corresponds to port 1. | R/W | 16'hffff |
| 7AH | Pause setting for port18~pot17, 1 bit per port<br>bit[9:8] :     0: disabled; 1: enabled<br>            The bit8 corresponds to port 17.<br>Other bits are reserved. | R/W | 10'h3ff |
| 7BH | Backpressure setting for port16~pot1, 1 bit per port<br>bit[15:0] :   0: disabled;<br>            1: enabled<br>            The LSB corresponds to port 1. | R/W | 16'hffff |
| 7CH | Backpressure setting for port18~pot17, 1 bit per port<br>bit[9:8] :     0: disable; 1: enable<br>            The bit8 corresponds to port 17.<br>Other bits are reserved. | R/W | 10'h3ff |
| 7DH | Transmit enable for port16~pot1, 1 bit per port<br>bit[15:0] :   0: Tx. disabled<br>            1: Tx. Enabled<br>            The LSB corresponds to port 1. | R/W | 16'hffff |
| 7EH | Transmit enable for port18~pot17, 1 bit per port<br>bit[9:8] :     0: Tx. Disabled; 1: Tx. Enabled<br>            The bit8 corresponds to port 17.<br>Other bits are reserved. | R/W | 10'h3ff |

| Register Address | Register Description | Attribute | Default value |
|---|---|---|---|
| 80H | CPU read/write PHY register command<br>bit[4:0] : the PHY address<br>bit[9:5] : the MII register address<br>bit[12:10] : (Reserved)<br>bit[13] : 1: the read/write command has been completed<br>     0: not yet<br>bit[14] : 0: read operation,<br>     1: write operation<br>bit[15] : the read/write command trigger<br>     0: IDLE or command complete<br>     1: Start command | R/W | 16'd0 |
| 81H | CPU read/ write PHY register data<br>bit[15:0] : the data to be written into PHY register for write command.<br>The last data read from PHY register read command. | R/W | 16'd0 |
| 82H | Port status of port4~pot1, 4 bit per port<br>bit[3:0] : {flow_ctrl, duplex, speed, link}. Bit[15:4] indicates the operating mode for port4 to port2. | R | 16'd0 |
| 83H~85H | Port status for port5 to port16. | R | 16'd0 |
| 88H | Link status port18~pot17, 4 bit per port<br>bit[7:0] : {flow_ctrl, duplex, speed, link}<br>Bit0~bit4 stands fot the operating mode for port 17. | R | 16'd0 |
| 90H | bit[15] : share memory over-flow indication<br>bit[14] : share memory under-flow indiaction<br><br>bit[10:0] : share memory current page count | R | 16'hxx |
| 91H | Reserved for test | Reserved | 16'hxx |
| 92H | Reserved for test | Reserved | 16'hxx |
| A0H | bit[0] : Interrupt enable for completing CPU r/w SMI command<br>     1: Enable interrupt indication;<br>     0: No interrupt<br><br>bit[4] : Status of the CPU r/w SMI command<br>     1: Command completed;<br>     0: Command processing | R/W | 5'h00 |
| A1 | Do not access to this register. | Reserved | 16'h000f |
| A2H | bit[0] : Software reset. Writing a "1" to this bit will reset the IP1718 LF. This bit is self-cleared to "0". | W | 1'b0 |

## 7    Electrical Characteristics

### 7.1    Absolute Maximum Rating

Permanent device damage may occur if Absolute Maximum Ratings are applied. Functional operation should be restricted to the conditions as specified in the following section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

| PARAMETER | | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | I/O | $V_{DDI/O}$ | – 0.5 | +3.6V | V |
| | Core | $V_{DDCore}$ | – 0.5 | +1.9V | V |
| Input Voltage | | $V_I$ | – 0.5 | $V_{DDI/O}$ | V |
| Output Voltage | | $V_O$ | – 0.5 | $V_{DDI/O}$ | V |
| Storage Temperature | | $T_{STG}$ | -65 | +150 | °C |
| Operation Temperature | | $T_{OPT}$ | 0 | +70 | °C |

**Note:** The maximum ratings are the limit value that must never be exceeded even for short time.

### 7.2    AC Characteristics

#### SS-SMII Transmit Timing

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{Tx\_Clk}$ | Transmit clock cycle time | - | 8 | - | ns |
| $T_{TSync\_D}$ | Tx_Clk rising edge to TX_Sync output delay | 1.0 | | 5.0 | ns |
| $T_{TData\_D}$ | Tx_Clk rising edge to TXD output delay | 1.0 | - | 5.0 | ns |
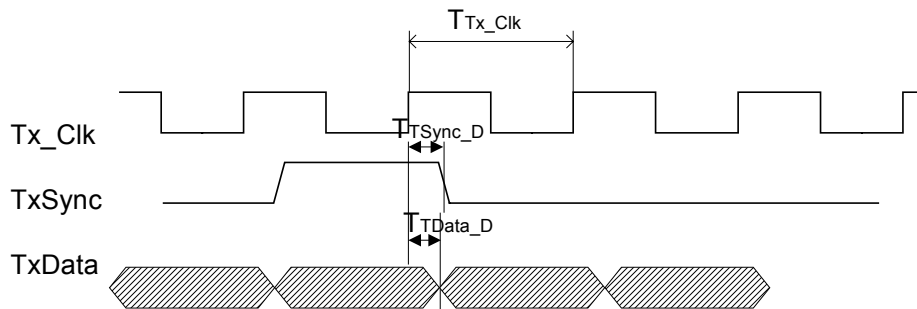


**SS-SMII Transmit**

#### SS-SMII Receive Timing

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{Rx\_Clk}$ | Receive clock cycle time | - | 8 | - | ns |
| $T_{RSync\_SU}$ | Rx_Sync Set up time | 2.0 | | | ns |
| $T_{Rdata\_H}$ | Rx_Sync Hold time | 1.0 | - | | ns |
| $T_{Rdata\_SU}$ | RxData Set up time | 2.0 | | | ns |
| $T_{RData\_H}$ | RxData Hold time | 1.0 | - | | ns |
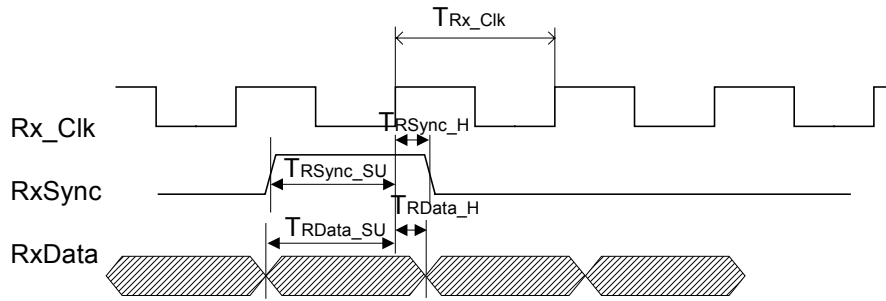
**SS-SMII Receive**

**PHY Management (MDIO) Timing**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{ch}$ | MDCK High Time | - | 200 | - | ns |
| $T_{cl}$ | MDCK Low Time | - | 200 | - | ns |
| $T_{cm}$ | MDCK cycle time | - | 400 | - | ns |
| $T_{MD\_SU}$ | MDIO set up time | 10 | - | | ns |
| $T_{MD\_H}$ | MDIO hold time | 10 | - | - | ns |
| $T_{MD\_D}$ | MDIO output delay time | 200 | - | 210 | ns |
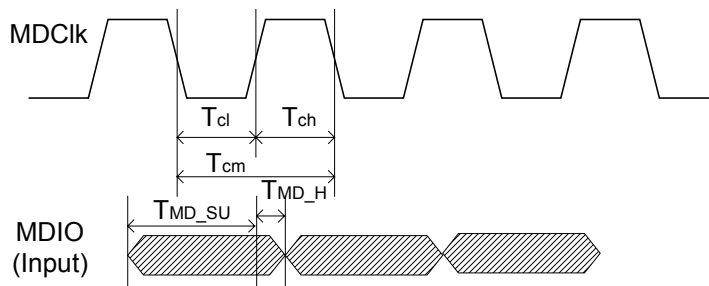


**MDIO Input Cycle**
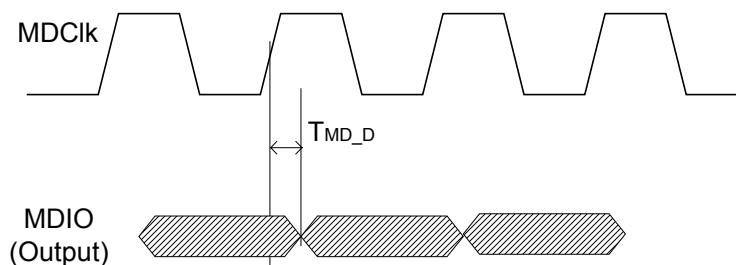


**MDIO Output Cicle**

**CPU Serial Bus Timing**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------|-------------|------|------|------|------|
| $T_{S\_C}$ | SCPUC cycle time | 400 | | - | ns |
| $T_{SIO\_SU}$ | Serial I/O set up time | 10 | - | | ns |
| $T_{SIO\_H}$ | Serial I/O hold time | 10 | - | - | ns |
| $T_{SIO\_D}$ | Serial I/O output delay time | | - | 20 | ns |
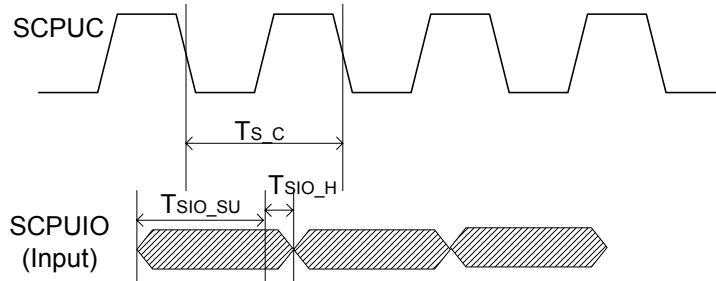
**Serial I/O Input Cycle**
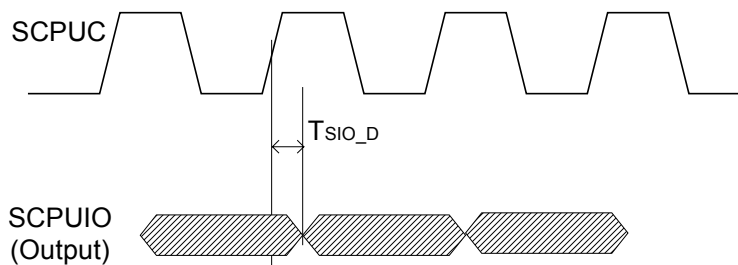
**Serial I/O Output Cycle**

**MII Transmit Timing**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------|-------------|------|------|------|------|
| $T_{TxClk}$ | Transmit clock period 100Mbps MII | - | 40 | - | ns |
| $T_{TxClk}$ | Transmit clock period 10Mbps MII | - | 400 | - | ns |
| $T_{TxClk\_SU}$ | TXEN, TXD to MII_TXCLK setup time | 2 | - | - | ns |
| $T_{TxClk\_H}$ | TXEN, TXD to MII_TXCLK hold time | 0.5 | - | - | ns |

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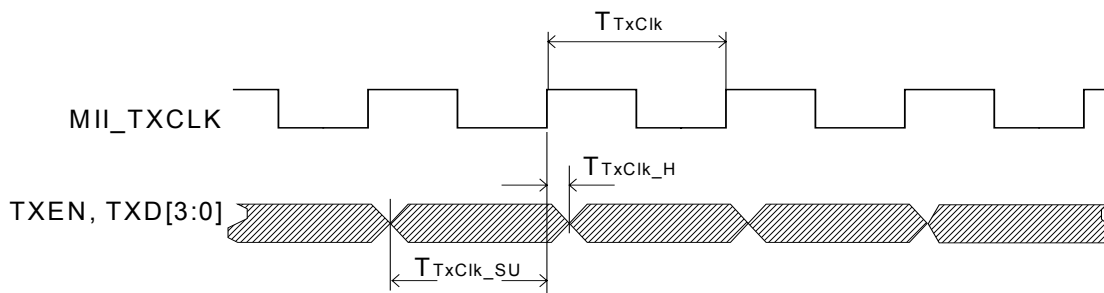
**MII Receive Timing**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{RxClk}$ | Receive clock period 100Mbps MII | - | 40 | - | ns |
| $T_{RxClk}$ | Receive clock period 10Mbps MII | - | 400 | - | ns |
| $T_{RxClk\_D}$ | MII_RXCLK falling edge to RXDV, RXD | 1 | - | 4 | ns |
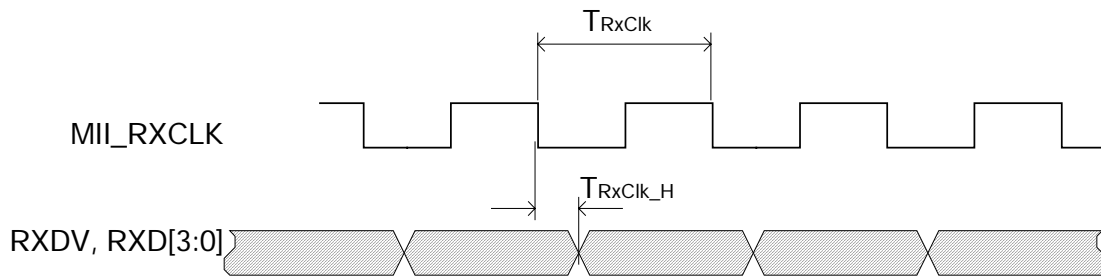
### 7.3 DC Characteristics

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Output low voltage | $V_{OL}$ | | | 0.4 | V |
| Output high voltage | $V_{OH}$ | 1.7V for 1.8V I/O supply voltage; 3V for 3.3V I/O supply voltage; | | | V |
| Low level output current | $I_{OL}$ | | | | mA |
| High level output current | $I_{OH}$ | | | | |
| VDD33 supply current | | | | | |
| VDD18 supply current | | | | | |
| VDDPLL supply current | | | | | |
| VDD33 supply voltage | | | 1.8 or 3.3 | | V |
| VDD18 supply voltage | | | 1.8 | | V |
| VDDPLL supply voltage | | | 1.8 | | V |
| SS-SMII Input Low to High treshold point(3.3V operation) | $V_{T+}$ | 1.66 | 1.75 | 1.79 | V |
| SS-SMII Input High to Low treshold point(3.3V operation) | $V_{T-}$ | 0.93 | 1.01 | 1.06 | V |
| Pull-down resistor | $R_{PD}$ | 51 | | 127 | KΩ |
| $\Theta_{Jc}$ | | | | | |
| $\Theta_{Ja}$ | | | | | |

## 8    Order Information

| Part No. | Package | Notice |
|----------|---------|--------|
| IP1718 | 128-PIN PQFP | - |
| IP1718 LF | 128-PIN PQFP | Lead free |

## 9    Package Detail

**128 PQFP Outline Dimensions**
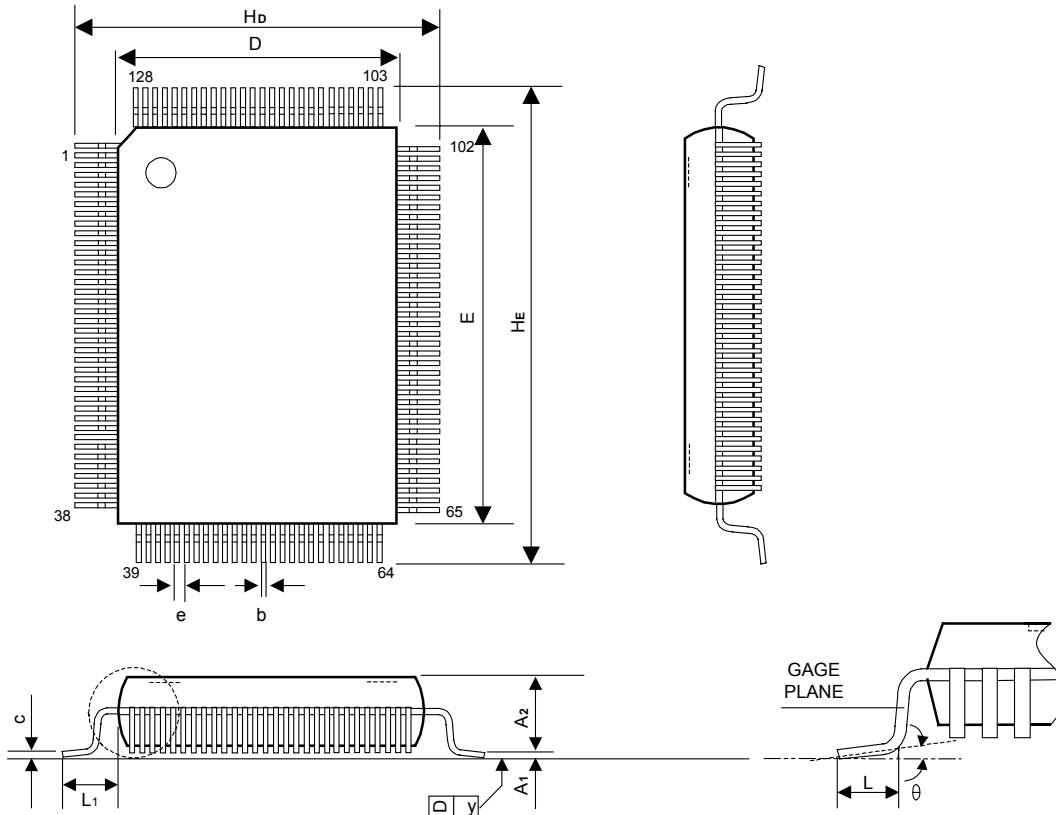


| Symbol | Dimensions In Inches | | | Dimensions In mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A1 | 0.010 | 0.014 | 0.018 | 0.25 | 0.35 | 0.45 |
| A2 | 0.107 | 0.112 | 0.117 | 2.73 | 2.85 | 2.97 |
| b | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| c | 0.004 | 0.006 | 0.008 | 0.09 | 0.15 | 0.20 |
| HD | 0.669 | 0.677 | 0.685 | 17.00 | 17.20 | 17.40 |
| D | 0.547 | 0.551 | 0.555 | 13.90 | 14.00 | 14.10 |
| HE | 0.906 | 0.913 | 0.921 | 23.00 | 23.20 | 23.40 |
| E | 0.783 | 0.787 | 0.791 | 19.90 | 20.00 | 20.10 |
| e | - | 0.020 | - | - | 0.50 | - |
| L | 0.025 | 0.035 | 0.041 | 0.65 | 0.88 | 1.03 |
| L1 | - | 0.063 | - | - | 1.60 | - |
| y | - | - | 0.004 | - | - | 0.10 |
| θ | 0° | - | 12° | 0° | - | 12° |

Note:
1. Dimension D & E do not include mold protrusion.
2. Dimension B does not include dambar protrusion.
   Total in excess of the B dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.

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