5 Port 10/100 Ethernet Integrated Switch

Features

- 5 port 10/100 Ethernet switch with built in transceivers and memory
- Build in SSRAM for frame buffer
- Built in storage of 1K MAC address
- Support flow control
  - Support IEEE802.3x for flow control for full duplex mode operation
  - Support backpressure for flow control for half duplex mode operation
- 5 port switching fabric
  - Support two-level hashing algorithm to solve MAC address collision
  - Support MAC address aging
  - Store and forward mode
  - Broadcast storm protection
  - Full line speed capability of 148800 (14880) packets/sec for 100M (10M)
  - Support 1536 byte data transfer for VLAN packet traffic
  - Port base VLAN
  - Port base CoS configuration
- Integrate 5 ports transceiver
  - Each port can be auto negotiable or forced 10M/100M, full/half duplex
  - Each port can be configured as 100BaseFX
  - Automatic MDI/MDI-X configuration
- Support two MII, one SMI and extended MII registers for router application
- Built in regulator for 3.3v to 2.15v
- LED status of Link, activity, Full/half duplex, speed, and power on diagnostic function
- Initial parameter setting by pin or EEPROM (24LC01) configuration
- Utilize single clock source (25Mhz)
- 0.25u technology
- Support Lead Free package (Please refer to the Order Information)

General Description

IP175A LF is a low cost 10/100 Ethernet single chip switch. It integrates a 5-port switch controller, SSRAM, and 5 10/100 Ethernet transceivers. Each of the transceivers complies with the IEEE802.3, IEEE802.3u, and IEEE802.3x specifications. The transceivers are designed in DSP approach with 0.25um technology; they have high noise immunity and robust performance.

IP175A LF operates in store and forward mode. It supports flow control, auto MDI/MDI-X, CoS, port base VLAN, and LED functions, etc. Each port can be configured to auto-negotiation or forced 10M/100M, full/half duplex, and it is also able to configure to 100BaseFX transmission mode. Using an EEPROM or pull up/down resistors on specified pins can configure the desired options. IP175A LF does not support “forced 10M half mode”.

IP175A LF supports two MII ports for router application, which supports 4 LAN ports and one WAN port. MII0 is for LAN traffic and MII1 is for WAN traffic and no external PHY is needed. Both MII can work in PHY mode and interface to the external MAC in this application. The external MAC can monitor or configure IP175A LF by accessing MII registers through SMI.

MII0 also can be configured to be MAC mode. It is used to interface an external PHY to work as a 4+1 switch.

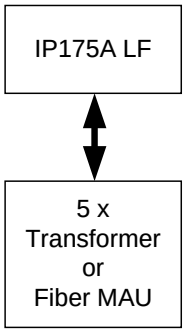
Table Of Contents

Revision History

Revision #	Change Description
IP175A LF-DS-R01	Initial release.
IP175A LF-DS-R02	1. Update pin description of REG_OUT on page 14. 2. Add VCC_IO limitation to the operation condition on page 61. 3. Add VCC_IO_1, VCC_IO_2, VCC pin description on page 18
IP175A LF-DS-R03	Update pin description of Reg_out page 14.
IP175A LF-DS-R04	Remove MII register 16H.
IP175A LF-DS-R05	Remove VLAN from MII Register.
IP175A LF-DS-R06	1. ADD AC Timing 2. Change minimum VCC from 2.1v to 2.0v on page 14 & 50
IP175A LF-DS-R07	Add the order information for lead free package.
IP175A LF-DS-R08	ADD LED Blink Timing Table on page 52.

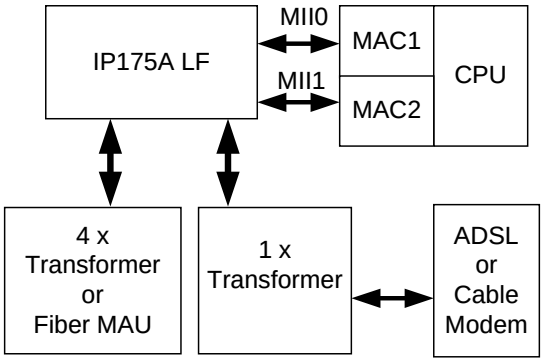
1 Applications

Application 1:



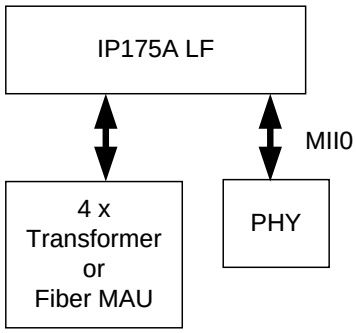
5 port Ethernet switch

Application 2:



4 LAN port + one WAN port (Router)

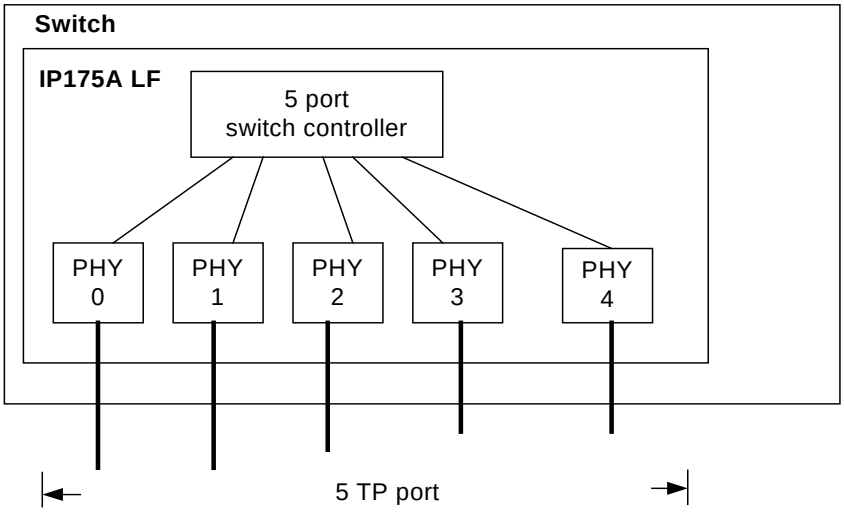
Application 3:



4 TP ports + one external PHY

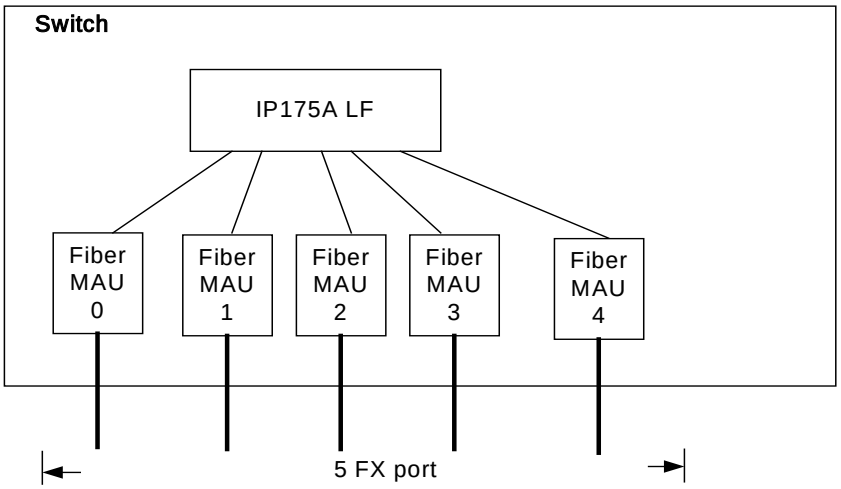
Applications (continued)

Application 1: 5 TP port switch



Use 5 builtin PHY.
MII0 and MII1 ports are not used.

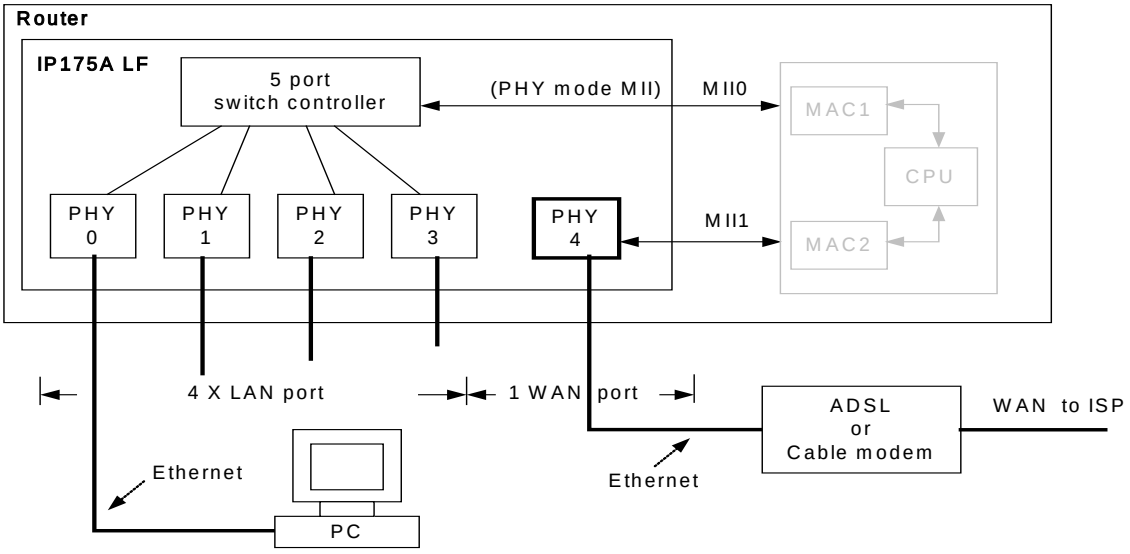
Application 1: 5 FX port switch



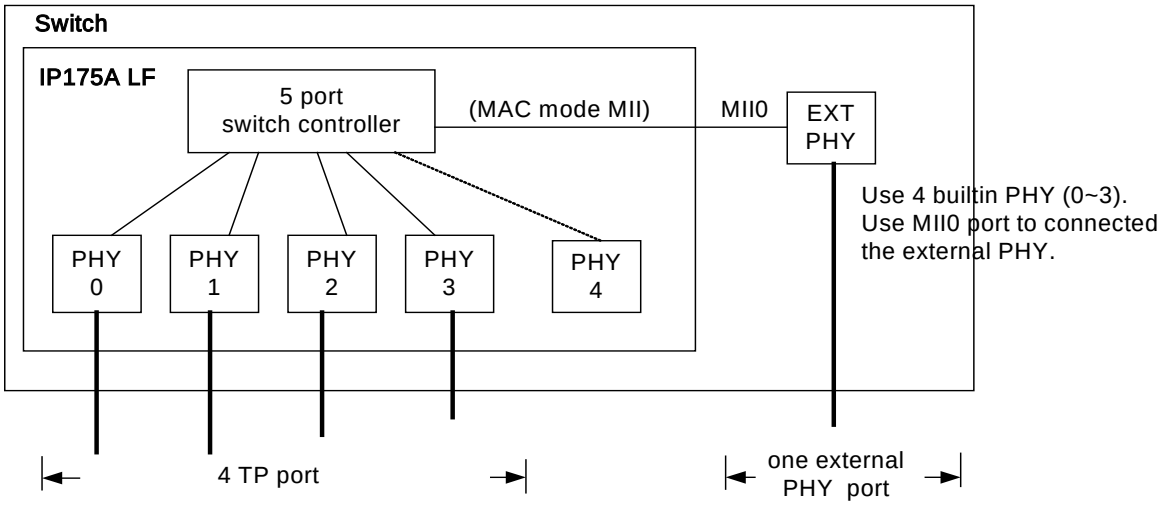
Use 5 external fiber MAU.
MII0 and MII1 ports are not used.

Applications (continued)

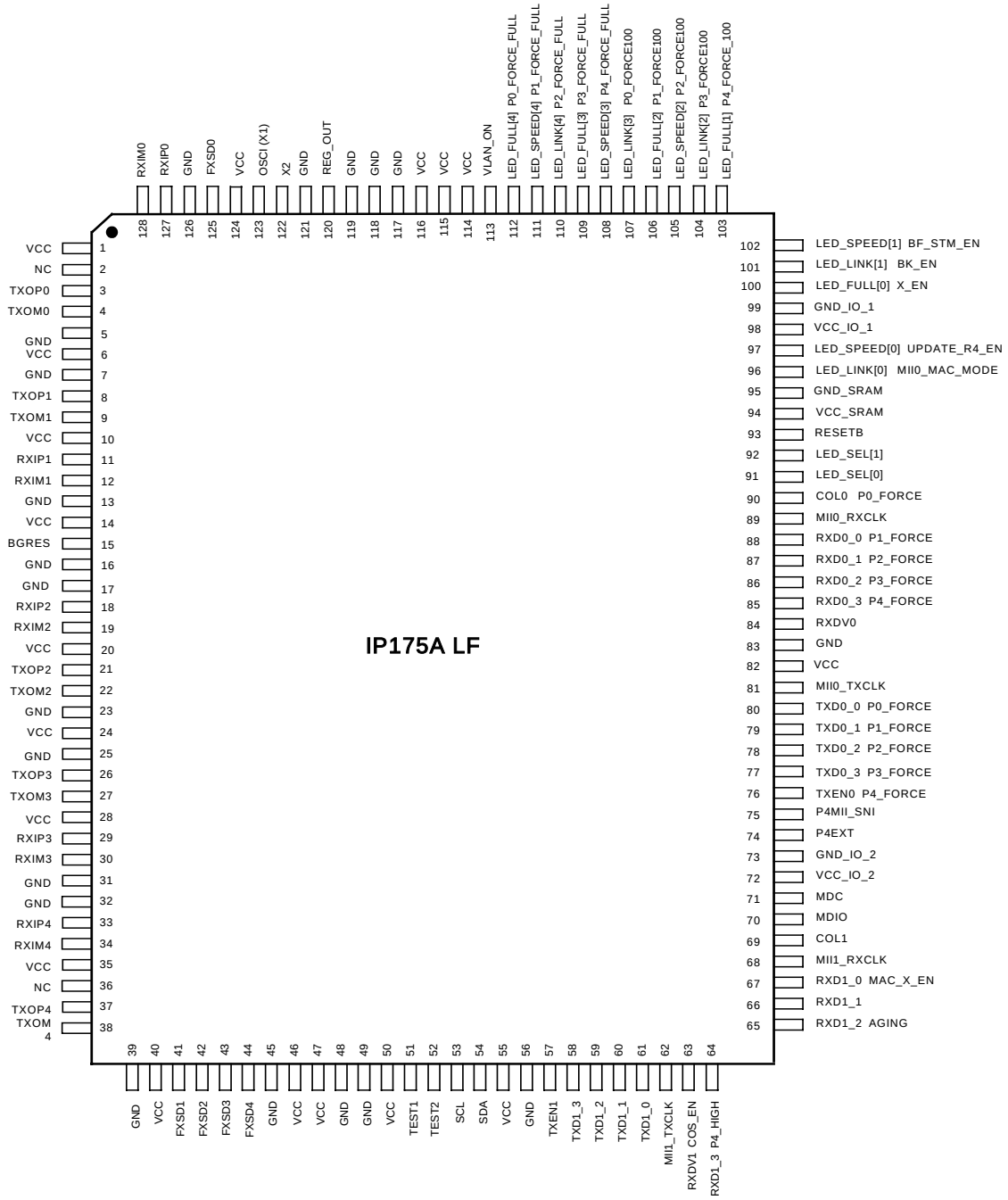
Application 2: 4 LAN port + one WAN port (Router)



Application 3: 4 TP port + one external PHY



2 Pin Diagram



3 Pin Descriptions

Type	Description
I	Input pin
O	Output pin
IPL	Input pin with internal pull low
IPH	Input pin with internal pull high

Type	Description
IPL1	Input pin with internal pull low 22.8k ohm
IPH1	Input pin with internal pull high 22.8k ohm
IPL2	Input pin with internal pull low 92.6k ohm
IPH2	Input pin with internal pull high 113.8k ohm

Pin no.	Label	Type	Description
LED pins used as initial setting mode during reset			
102	BF_STM_EN	IPL1	Broadcast storm protection enable 1: enable, 0: disable (default)
101	BK_EN	IPH1	Backpressure enable 1: enable (default), 0: disable This pin doesn't set the flow control of MII0 port. MAC_X_EN sets the flow control of MII0 port.
100	X_EN	IPH1	IEEE802.3X enable 1: enable (default), 0: disable This pin doesn't set the flow control of MII0 port. MAC_X_EN sets the flow control of MII0 port.
97	UPDATE_R4_EN	IPL1	Change capability enable A full duplex port will change its capability to half duplex, if the remote full duplex port does not support IEEE802.3x then this function is enabled. It should be pulled low for normal operation. 1: enable, 0: disable (default)

Pin Descriptions (continued)

Pin no.	Label	Type	Description
MII pins used as initial setting mode during reset			
113	VLAN_ON	IPL	VLAN enable 1: enable, 0: disable (default) IP175A LF is separated into 4 VLAN groups if this function is enabled. VLAN 1: port0, port 4; VLAN 2: port 1, port 4; VLAN 3: port 2, port 4; VLAN 4: port 3, port 4; Programming EEPROM registers 0Eh~12h or MII register 13h~15h will overwrite the VLAN configuration.
64	P4_HIGH	IPL2	Port4 is set to be high priority port 1: enable, 0: disabled (default) Packets received from port4 are handled as high priority packets if the feature is enabled. Please refer to EEPROM registers 0Eh~12h or MII register 13h~15h for detail information.
63	COS_EN	IPL2	Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag are handled as high priority packets for all ports if the feature is enabled. Please refer to EEPROM registers 0Eh~12h or MII register 13h~15h for detail information.
65	AGING	IPH2	Address aging enable 1: enable, aging time 300s (default), 0: disable

Pin Descriptions (continued)

Pin no.	Label	Type	Description
External MII port setting			
74	P4EXT	IPL	External MII port enable 1: Both MII interface are enabled for router application. MII1 supports PHY mode only. MII1 interfaces to internal PHY4 of IP175A LF. It is connected to an external MAC device. MII0 supports both PHY mode and MAC mode depending on the setting of MII0_MAC_MOD (pin 96). 0: External MII interface is disabled and IP175A LF works as a 5-port switch (default).
75	P4MII_SNI	IPL	External MII interface selection 1: SNI interface IP175A LF supports PHY mode SNI (MII0_MAC_MOD=0), i.e., it can be connected to an external MAC. IP175A LF doesn't support MAC mode SNI (MII0_MAC_MOD=1), i.e., it should not be connected to an external PHY. 0: MII interface (default).

Pin no.	Label	Type	Description
External MII0 interface (P4EXT=1)			
67	MAC_X_EN	IPH2	Flow control enable for external MII0 port 1: enable (default), 0: disable
96	MII0_MAC_MOD	IPL1	External MII0 port MAC mode 1: MII0 works as a MAC and should be connected to an external PHY. 0: MII0 works as a PHY and should be connected to an external MAC device (default). This pin does not affect MII1 port.
71, 70	MDC, MDIO	IPL	SMI The external MAC device uses the interface to program basic and extended MII register to configure PHY 4 and switch controller,

Pin Descriptions (continued)

Pin no.	Label	Type	Description
External MII0 interface (PHY mode, MII0_MAC_MOD=0, P4MII_SNI=0)			
81	MII0_TXCLK	O	MII transmit clock
80, 79, 78, 77	TXD0_0, TXD0_1, TXD0_2, TXD0_3	IPL2	MII transmit data It is sampled at the rising edge of MII0_TXCLK.
76	TXEN0	IPL2	MII transmit enable It is used to frame TXD0[3:0]. It is sampled at the rising edge of MII0_TXCLK.
90	COL0	O	MII collision It is active when port 4 of switch controller is set to be half duplex and a collision event happens.
84	RXDV0	O	MII receive data valid It is used to frame RXD0[3:0]. It is sent out at the falling edge of MII0_TXCLK.
88, 87, 86, 85	RXD0_0, RXD0_1, RXD0_2, RXD0_3	O	MII receive data It is sent out at the falling edge of MII0_TXCLK.
89	MII0_RXCLK	O	MII receive clock There is no clock output in this mode.

Pin no.	Label	Type	Description
External MII0 interface (MAC mode, MII0_MAC_MOD=1, P4MII_SNI=0)			
81	MII0_TXCLK	I	MII transmit clock It is an input clock and it is connected to MII_TXCLK of external PHY.
80, 79, 78, 77	TXD0_0, TXD0_1, TXD0_2, TXD0_3	O	MII transmit data It is connected to MII_TXD of external PHY. It is sent out at the rising edge of MII0_TXCLK.
76	TXEN0	O	MII transmit enable It is an output signal and is connected to MII_TXEN of external PHY. It is sent out at the rising edge of MII0_TXCLK.
90	COL0	IPL2	MII collision It is an input signal and is connected to the MII_COL of external PHY.
84	RXDV0	I	MII receive data valid It is an input signal and is connected to the MII_RXDV of external PHY. RXDV0 is used to frame RXD0[3:0].
88, 87, 86, 85	RXD0_0, RXD0_1, RXD0_2, RXD0_3	I	Receive data It is NRZ data and is connected MII_RXD[3:0] of external PHY. It is received at the rising edge of MII0_RXCLK.
89	MII0_RXCLK	I	MII receive clock

Pin Descriptions (continued)

Pin no.	Label	Type	Description
External MII1 interface (PHY mode only, P4EXT=1)			
62	MII1_TXCLK	O	MII Transmit clock
61, 60, 59, 58	TXD1_0, TXD1_1, TXD1_2, TXD1_3	IPL2	MII transmit data It is sampled at the rising edge of MII1_TXCLK.
57	TXEN1	IPL2	MII transmit enable It is used to frame TXD1[3:0]. It is sampled at the rising edge of MII1_TXCLK.
69	COL1	O	MII collision It is active when PHY4 is set to be half duplex and a collision event happens.
63	RXDV1	O	MII receive data valid It is used to frame RXD1[3:0]. It is sent out at the falling edge of MII1_RXCLK.
67, 66, 65, 64	RXD1_0, RXD1_1, RXD1_2, RXD1_3	O	MII receive data It is sent out at the falling edge of MII1_RXCLK.
68	MII1_RXCLK	O	MII receive clock

Pin Descriptions (continued)

Pin no.	Label	Type	Description
Force mode			
85	P4_FORCE	IPL2	Port4 works at force mode. 1: force mode, disable port4 NWAY capability 0: auto-negotiation with all capability enabled (default) It is used to force MII0 port PHY mode if P4EXT is pulled high. It's set by pin 85 if MII0 is in PHY mode and it's set by pin 76 if MII0 is in MAC mode.
76			
86	P3_FORCE	IPL2	Port3 works at force mode. 1: force mode, disable port3 NWAY capability 0: auto-negotiation with all capability enabled (default) It's set by pin 86 if MII0 is in PHY mode and it's set by pin 77 if MII0 is in MAC mode.
77			
87	P2_FORCE	IPL2	Port2 works at force mode. 1: force mode, disable port2 NWAY capability 0: auto-negotiation with all capability enabled (default) It's set by pin 87 if MII0 is in PHY mode and it's set by pin 78 if MII0 is in MAC mode.
78			
88	P1_FORCE	IPL2	Port1 works at force mode. 1: force mode, disable port1 NWAY capability 0: auto-negotiation with all capability enabled (default) It's set by pin 88 if MII0 is in PHY mode and it's set by pin 79 if MII0 is in MAC mode.
79			
90	P0_FORCE	IPL2	Port0 works at force mode. 1: force mode, disable port0 NWAY capability 0: auto-negotiation with all capability enabled (default) It's set by pin 90 if MII0 is in PHY mode and it's set by pin 80 if MII0 is in MAC mode.
80			

Pin Descriptions (continued)

Pin no.	Label	Type	Description
Force mode			
103	P4_FORCE100	IPL1	Force port4 work at 100M or 10M. 1: force 100M 0: force 10M (default) It is used to force MII0 port PHY mode if P4EXT =1.
104	P3_FORCE100	IPL1	Force port3 work at 100M or 10M. 1: force 100M 0: force 10M (default)
105	P2_FORCE100	IPL1	Force port2 work at 100M or 10M. 1: force 100M 0: force 10M (default)
106	P1_FORCE100	IPL1	Force port1 work at 100M or 10M. 1: force 100M 0: force 10M (default)
107	P0_FORCE100	IPL1	Force port0 work at 100M or 10M. 1: force 100M 0: force 10M (default)

Pin no.	Label	Type	Description
Force mode			
108	P4_FORCE_FULL	IPL1	Force port4 work at full duplex or half duplex 1: force full duplex 0: force half duplex (default) It is used to force MII0 port PHY mode if P4EXT=1. IP175A LF does not support “force 10M half mode”.
109	P3_FORCE_FULL	IPL1	Force port3 work at full duplex or half duplex 1: force full duplex 0: force half duplex (default) IP175A LF does not support “force 10M half mode”.
110	P2_FORCE_FULL	IPL1	Force port2 work at full duplex or half duplex 1: force full duplex 0: force half duplex (default) IP175A LF does not support “force 10M half mode”.
111	P1_FORCE_FULL	IPL1	Force port1 work at full duplex or half duplex 1: force full duplex 0: force half duplex (default) IP175A LF does not support “force 10M half mode”.
112	P0_FORCE_FULL	IPL1	Force port0 work at full duplex or half duplex 1: force full duplex 0: force half duplex (default) IP175A LF does not support “force 10M half mode”.

Pin Descriptions (continued)

Pin no.	Label	Type	Description
Transceiver			
127, 128, 11, 12, 18,19, 29, 30, 33, 34	RXIP0, RXIM0, RXIP1, RXIM1, RXIP2, RXIM2, RXIP3, RXIM3, RXIP4, RXIM4	I	TP receive
3, 4, 8, 9, 21, 22, 26, 27, 37, 38	TXOP0, TXOM0, TXOP1, TXOM1, TXOP2, TXOM2, TXOP3, TXOM3, TXOP4, TXOM4	O	TP transmit
14	BGRES	O	Band gap resister. It is connected to GND through a 6.2 k ohms resistor. Please refer to application circuit for more information.
125, 41, 42, 43, 44	FXSD0~4	I	100Base-FX Signal detect IP175A LF will latch the value on FXSDx pins at the end of reset to decide if the port works at 100BaseFX mode. A port works in 100BaseFX mode, if its corresponding signal FXSDx > 0.6v at the end of reset. FXSDx should be connected to GND if the port works in TP mode. That is, a port is a fiber port if its FXSDx is connected to the SD of fiber MAU and a port is a TP port if its FXSDx is connected to GND. The SD of fiber port is active if the voltage of FXSDx is higher than 1.2v. It is used to inform IP175A LF if the fiber is plugged or not.

Pin no.	Label	Type	Description
Misc.			
123	X1	I	25M system clock input
122	X2	O	Crystal pin
93	RESETB	I	Reset, low active

Pin no.	Label	Type	Description
Misc.			
120	REG_OUT	O	Regulator output It is used to control external transistor to generate a 2.15v ±5% voltage source when VCC_IO_1 and VCC_IO_2 are exactly 3.3v and all ports are link on. To meet the specification of minimum VCC (2.0v), VCC_IO_1 and VCC_IO_2 should be at least 3.3v. The supply current of external transistor used should be at least 1A.

Pin Descriptions (continued)

Pin no.	Label	Type	Description
EEPROM			
53	SCL	I/O	After reset, it is used as clock pin SCL of EEPROM. Its period is longer than 10us. IP175A LF stops reading EEPROM if it finds there is no 55AA pattern in register 0. After reading EEPROM, this pin becomes an input pin.
54	SDA	IO	After reset, it is used as data pin SDA of EEPROM. After reading EEPROM, this pin becomes an input pin.

Pin no.	Label	Type	Description
LED			
92, 91	LED_SEL[1:0]	IPH	LED output mode selection. LED_SEL[1:0]=00: LED mode 0, LED_SEL[1:0]=01: LED mode 1, LED_SEL[1:0]=10: LED mode 2, LED_SEL[1:0]=11: LED mode 3 (default)
110, 107, 104, 101, 96	LED_LINK[4:0]	O	Link, Activity (output after reset) LED mode0: 100M Link + Activity (same as mode 2) LED mode1: Receive activity (1: not receiving, flash: receiving) LED mode2, 100M Link + Activity (1: 100M Link fail, 0: 100M Link ok and no activity, flash: 100M Link ok and TX/RX activity) LED mode3: Link + Activity (1: link fail, 0: link ok, flash: Link ok and TX/ RX activity)
111, 108, 105, 102, 97	LED_SPEED[4:0]	O	Speed (output after reset) LED mode0: (1: no collision, flash: collision) (note*) LED mode1: (1: speed=10M, 0: speed=100M) LED mode2: Full/half: (1: half, 0: full, flash: collision) LED mode3: (1: speed=10M, 0: speed=100M)
112, 109, 106, 103, 100	LED_FULL[4:0]	O	Full/half, Link (output after reset) LED mode0, 10M Link + Activity (same as mode 2) LED mode1, Link: (1: Link fail, 0: Link ok) LED mode2, 10M Link + Activity (1: 10M Link fail, 0: 10M Link ok and no activity, flash: 10M Link ok and TX/RX activity) LED mode3: Full/half: (1: half, 0: full, flash: collision)

Note: LED_SPEED[0] shows collision information for all ports. LED_SPEED[4:1] is undefined.

Pin Descriptions (continued)

Pin no.	Label	Type	Description
Power			
98, 72	VCC_IO_1, VCC_IO_2	I	Power for output pins They should be connected 3.3v if MII, EEPROM, or built in regulator (REG_OUT) is used. They can be connected to the same power source as VCC if IP175A LF works as a 5-port switch without using bulilt in regulator.
	VCC	I	Power for core 2.15v~2.625v

Pin no.	Label	Type	Description
Test mode			
51, 52	TEST1, TEST2	IPL	Test mode selection They should be connected to GND for normal operation.

4 Functional Description

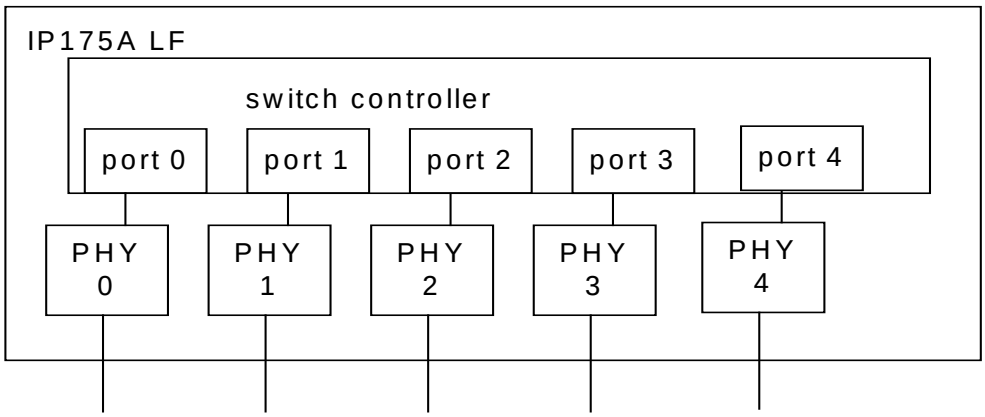
4.1 5-port switch application

IP175A LF works as a 5 TP port auto MDI-MDIX switch when all fibers and MII function are disabled. In this case, both FXSDx and P4EXT should be pulled low. Each port can be with auto-negotiation or force mode in this application.

An example to illustrate the configuration setting of port4 when P4EXT is pulled low and MII is disabled

Port	TP	FX	Nway	Capability	FXSD4	P4_FORCE	P4_FORCE100	P4_FORCE_FULL
4	V	--	V	All capability	0	0	0	0
4	V	--	V	10M/ full	0	1	0	1
4	V	--	--	100M/ half	0	1	1	0
4	V	--	V	100M/ full	0	1	1	1
4	--	V	--	100M half	> 0.6v	1	1	0
4	--	V	--	100M full	> 0.6v	1	1	1

Note:
1. The configuration not in the table is inhibited.
2. "--": Not applicable



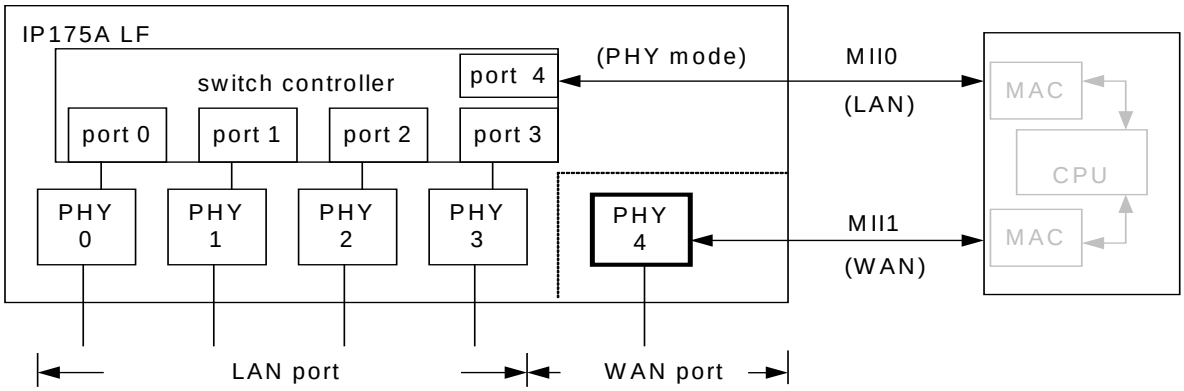
4.2 Router application

IP175A LF supports two MII ports, MII0 and MII1, for router application when P4EXT is pulled high. Pin P4_FORCE, P4_FORCE100 and P4_FORCE_FULL decide the speed and duplex of MII0. The speed and duplex of MII1 depend on the result of auto-negotiation of PHY4. But, programming basic MII registers through SMI can modify them. MAC_X_EN pin decides the flow control option of MII0. It is illustrated in the following table.

MII0							
P4EXT	**MAC_X_EN**	**P4_FORCE**	**P4_FORCE100**	**P4_FORCE_FULL**	**Speed**	**Duplex**	**Flow control**
0	X	X	X	X	MII0 disabled.		
1	0	1	1	1	100M	Full	Off
1	0	1	1	0	100M	Half	Off
1	0	1	0	1	10M	Full	Off
1	0	1	0	0	10M	Half	Off
1	1	1	1	1	100M	Full	On
1	1	1	1	0	100M	Half	On
1	1	1	0	1	10M	Full	On

X: “don’t care”

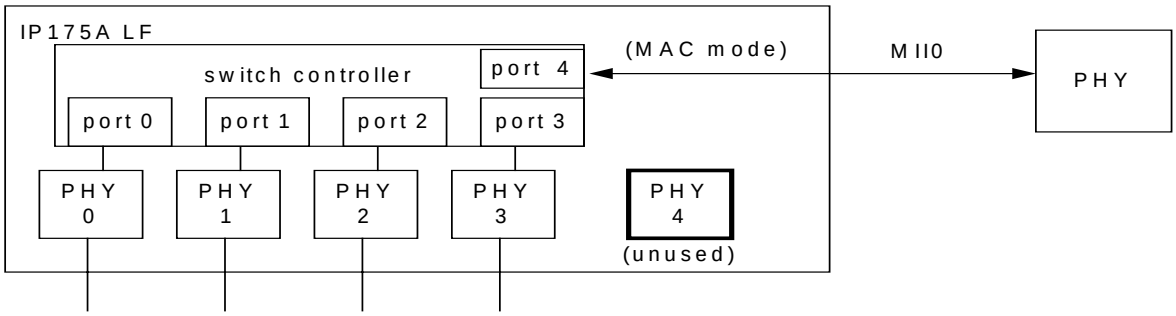
IP175A LF can work as a router with 4 LAN ports and one WAN port, which use internal PHY (PHY4). MII0 is the interface between port4 of internal switch controller and external MAC. MII1 is the interface between internal transceiver PHY4 and external MAC. The switch controller forwards frames from port0~3 to MII0 and vice versa. PHY4 works as an independent single PHY for external MAC. MII0 works at PHY mode in this application (MII_MAC_MOD=0).



4.3 MII0 MAC mode

MII0 works at MAC mode if MII_MAC_MOD is pulled high. MII0 is an interface between port4 of internal switch controller and external PHY. It replaces an Ethernet PHY with a user specified PHY in this application.

The speed and duplex of MII0 are configured by P4_FORCE, P4_FORCE100 and P4_FORCE_FULL. IP175A LF doesn't read the status of external PHY via SMI at this mode.

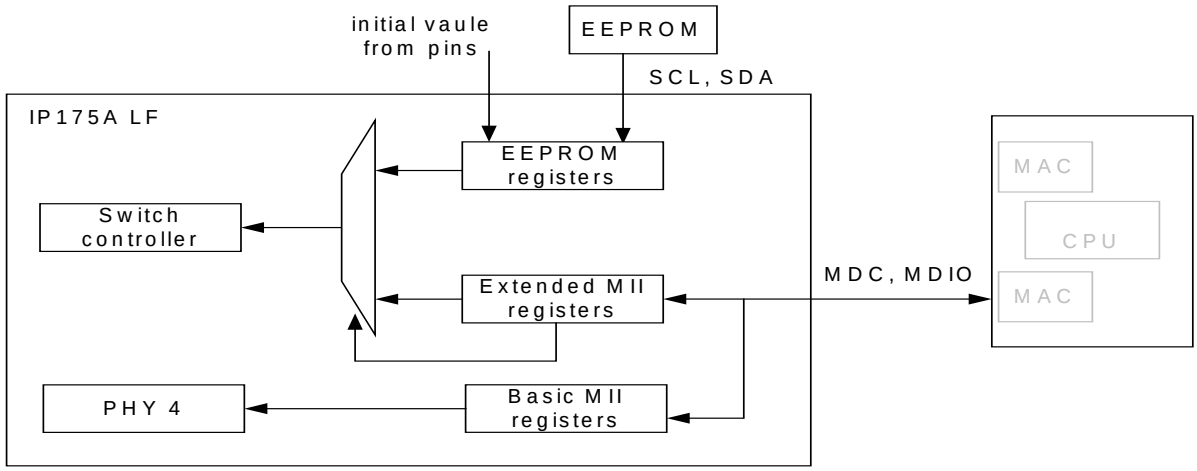


4.4 MII, SMI and MII register

IP175A LF supports two MII and one SMI (MDC and MDIO). Two MII interface to the external MAC for data transfer and the SMI is used to program switch controller and PHY4.

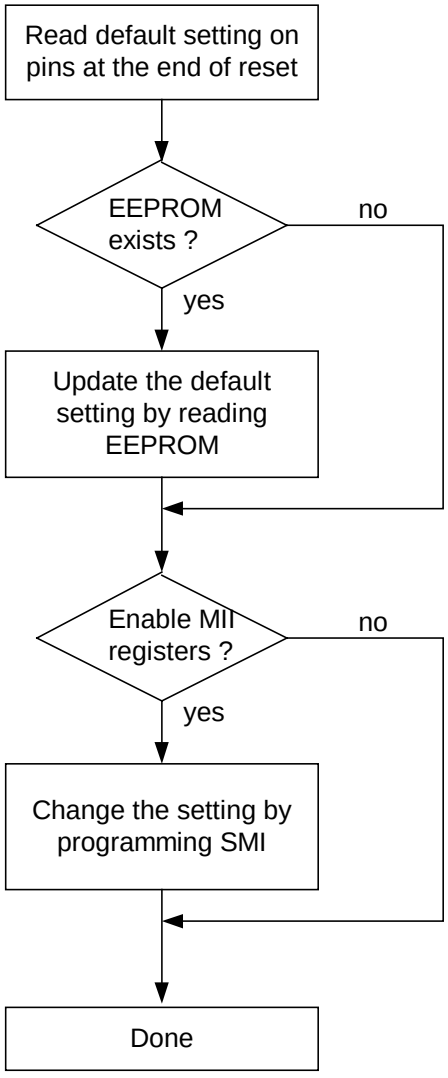
IP175A LF provides basic MII registers for PHY4 and extended MII registers for switch controller. The external MAC monitors or configures PHY4 by reading or writing the basic MII registers through SMI. The external MAC monitors or configures switch controller by reading or writing the extended MII registers through SMI.

The switch controller can be configured by pin and EEPROM, too. The operation is illustrated in the following diagrams.



Three ways to configure IP175A, by pins, EEPROM, or programming MII registers

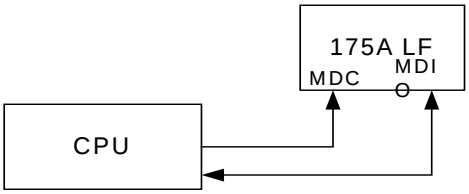
Parameter setting with pins, EEPROM and MII registers in IP175A LF



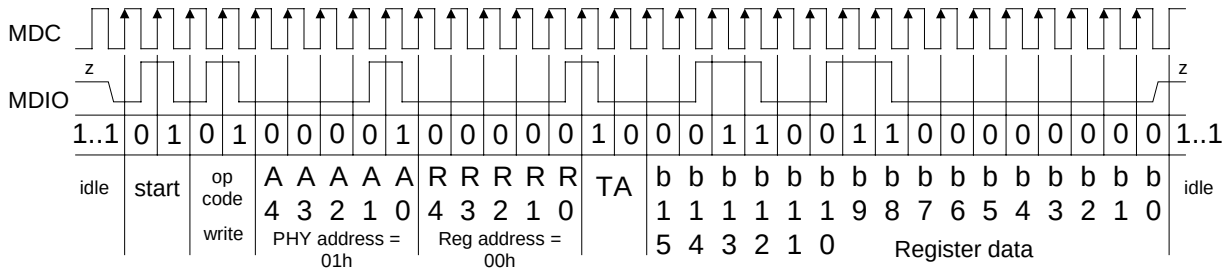
Serial management interface (SMI)

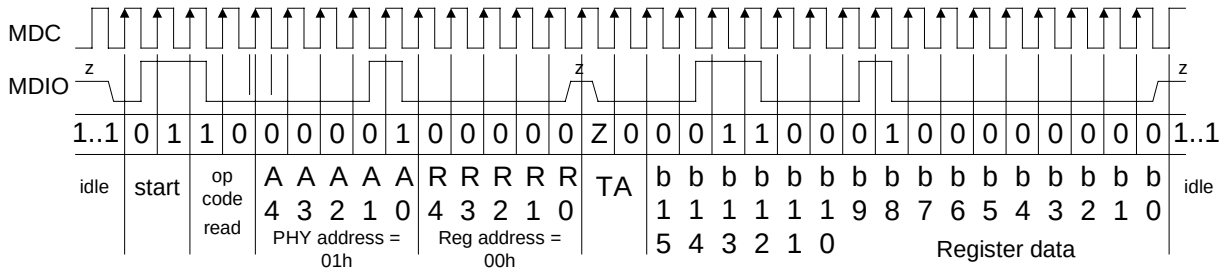
User can access IP175A LF's MII registers through serial management interface with pin MDC and MDIO. A specific pattern on MDIO is used to access a MII register. Its format is shown in the following table. When the SMI is idle, MDIO is in high impedance. To initialize the MDIO interface, the management entity sends a sequence of 32 contiguous "1" and "start" on MDIO.

Syatem diagram



Frame format	<Idle><start><op code><PHY address><Registers address><turnaround> <data><idle>
Read Operation	<Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0> <b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>
Write Operation	<Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10> <b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>



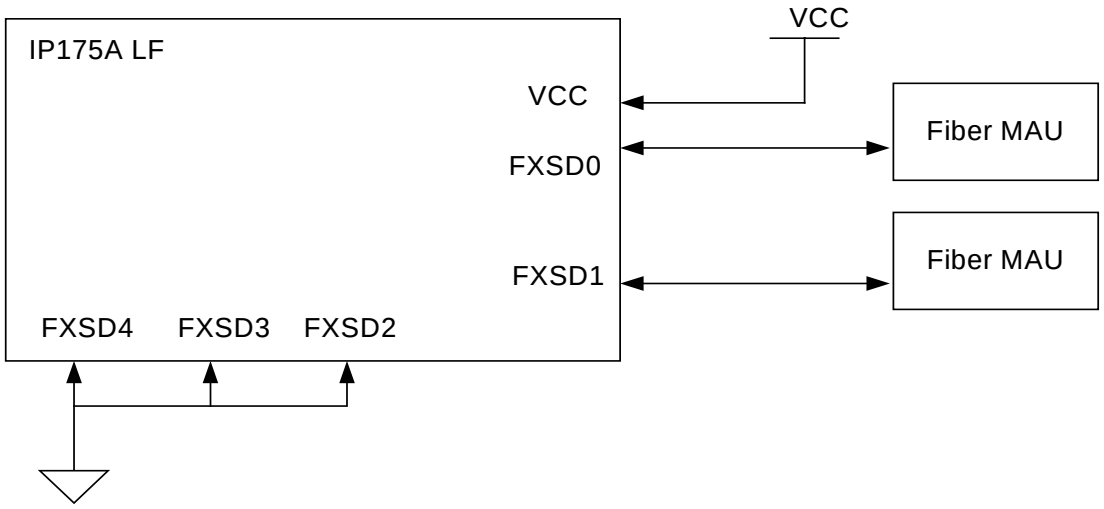


4.5 Fiber port configuration

Each port of IP175A LF can be configured to be a fiber port or a TP port. A port becomes a fiber port if its FXSDx is connected to a fiber MAU or it is pulled high. A port becomes a TP port if its FXSDx is pulled low. It is illustrated in the following table.

	Port configuration			
Voltage on FXSDx	**TP port**	**Fiber port**	**Fiber signal detect**	**Condition**
< 0.6v	V	--	--	--
> 0.6v, < 1.2v	--	V	Off	Fiber unplugged
> 1.2v	--	V	On	Fiber plugged

The following is an example that IP175A LF is configured to be 3 TP ports and 2 fiber ports. In this case, the speed and duplex of fiber ports are defined by pin P0_FORCE100, P0_FORCE_FULL, P1_FORCE100, and P1_FORCE_FULL.



4.6 CoS

IP175A LF supports two type of Cos. One is port base priority function and the other is frame base priority function. IP175A LF supports two levels of priority queues. A high priority packet will be queued in the memory as a high priority queue, this action will ensure more bandwidth for the high priority packets in the transmission.

The packets received from high priority port will be handled as high priority frames if the port base priority is enabled. It is enabled by programming the corresponding bit in EEPROM register 0Eh~12h of or MII register 13h~15h. Each port of IP175A LF can be configured as a high priority port individually.

IP175A LF examines the specific bits of VLAN tag and TCP/IP TOS for priority frames if the frame base priority is enabled. The packets will be handled as high priority frames if the value of VLAN tag or TCP/IP TOS field meets the high priority requirement. It is enabled by programming the corresponding bit in EEPROM register 16H~21H or MII register 17h~1Ch. The frame base priority function of each port can be enabled individually.

The Cos function can be active even if there is no EEPROM. IP175A LF supports an easy way to enable a sub set CoS function without EEPROM. Port 4 can be set as a high priority port if pin 64 (p4_high) is pulled high. Frame base priority function of all ports is enabled if pin 63 (Cos_en) is pulled high. The setting in register takes precedence of the setting on pins.

4.7 VLAN

4.7.1 Port base VLAN

IP175A LF supports port base VLAN functions. It separates IP175A LF into some groups (VLAN). A port is limited to communicate with other ports within the same group when the function is enabled. Frames are limited in a VLAN group and will not transmit out of this VLAN group. A port can be assigned to one or more VLAN groups. The members (ports) of a VLAN group are assigned by programming EEPROM register 0Eh~12h of or MII register 13h~15h.

The VLAN function can be active even if there is no EEPROM. IP175A LF supports an easy way to enable a sub set VLAN function without EEPROM. A default configuration of VLAN is adopted if pin 113 (VLAN_on) is pulled high. The VLAN group in this mode is illustrated in the pin description of VLAN_on. It is benefit in a router application that an individual LAN port can shares a WAN port. The setting in register takes precedence of the setting on pins.

4.7.2 Tag / un-tag

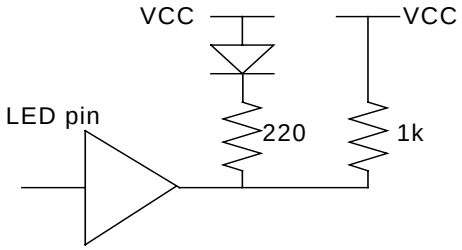
IP175A LF supports tag / un-tag functions. When the function is enabled, IP175A LF inserts the pre-defined tag into a forwarded frame if the frame is forwarded to a tagged field. IP175A LF strips the tag of a frame if the frame is forwarded to an untagged field. The operation is illustrated as follows. IP175A LF doesn't support tag VLAN function.

Frame type of the received packet	The operation of a output port	
	Forward to a untagged filed	Forward to a tagged field
Untagged	Transmit as received	1. Insert VLAN tag to the packet. 2. The inserted VLAN tag is defined in the EEPROM register of source port.
Priority-tagged (VLAN ID=0)	Strip tag	1. Keep priority field. 2. Modify the VLAN ID. 3. The modified VLAN tag is defined in the EEPROM register of source port.
VLAN-tagged	Strip tag	Transmit as received

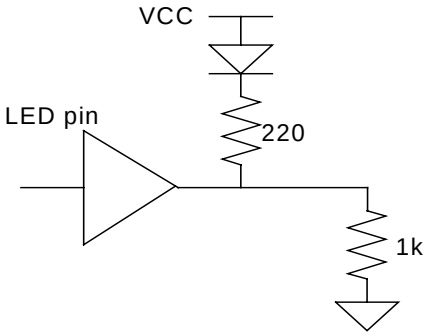
4.8 Initial value set by LED pins

Most configuration pins are shared with LED pin in IP175A LF. These multi-function pins are input during reset period and are LED output after reset. IP175A LF reads initial value via pins during the reset period. An initial value is set to 1 (0) by connecting a pin to vcc (gnd) through a 10kΩ (1kΩ) resistor as shown on the following figure.

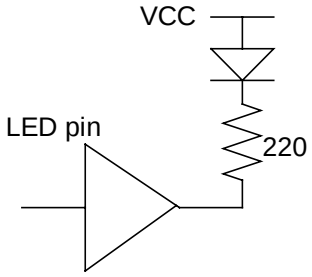
The application circuit is shown below.



to set initial value = 1
with pull up 1k ohm resister to VCC



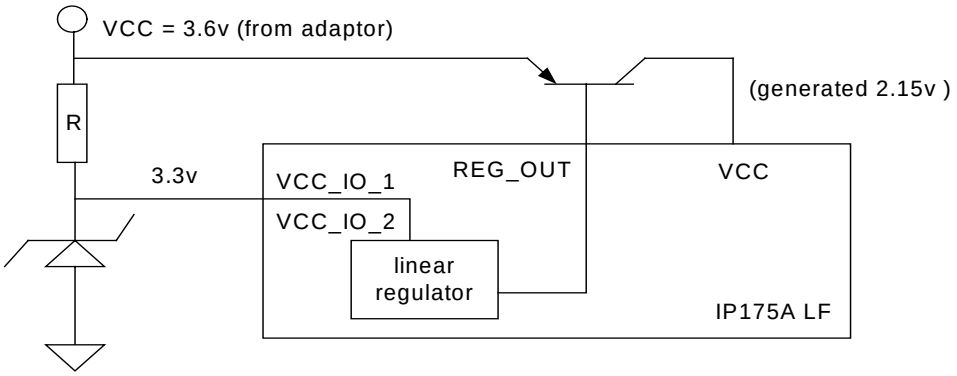
to set initial value = 0
with pull down 1k ohm resister to GND



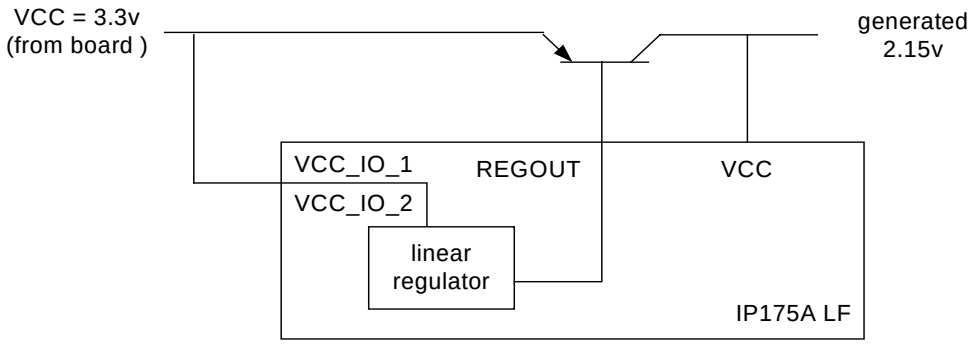
to use default value
(use no resistor to leave it open)

4.9 Built in regulator

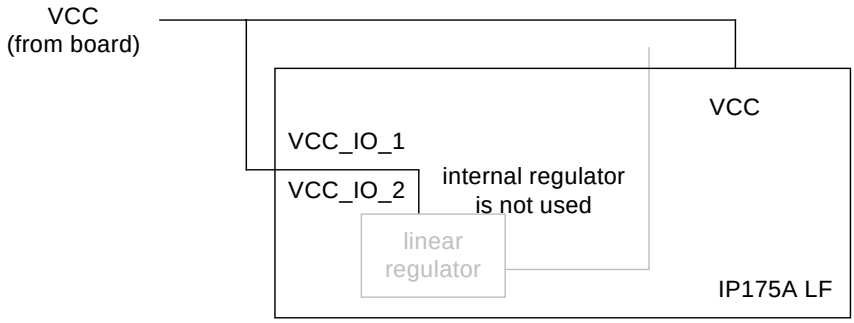
IP175A LF built in a linear regulator to generate 2.15v power. The applications are shown below.



Pure switch with a 3.6v power adaptor.



Router with an on board 3.3v power source



Pure switch uses on board single power source

4.10 Extended MII registers

MII	ROM	Function	R/W	Description	Default
MII register 12H (18D)					
12.15 12.14	2.1 2.0	LED_SEL [1:0]	R/W	Led_sel, LED mode selection. LED_SEL[1:0]=2'b00: LED mode 0, LED_SEL[1:0]=2'b01: LED mode 1, LED_SEL[1:0]=2'b10: LED mode 2, LED_SEL[1:0]=2'b11: LED mode 3 (default)	2'b11
12.13	4.7	X_EN	R/W	X_en, IEEE 802.3x flow control enable This signal is used as pause_en for digital parts. 1: enable, 0:disable	1
12.12	4.4	BK_EN	R/W	Bk_en, Backpressure enable 1: enable, 0: disable	1
12.11	4.2	BF_STM_EN	R/W	Broadcast storm enable 1: enable Drop the incoming packet if the number of queued broadcast packet is over the threshold. The threshold is defined in register 0AH[14:13]. 0: disable	0
12.10	4.3	MAC_X_EN	R/W	MII0 flow control enable 1: enable, 0: disable	1
12.7	--	MII_REGISTER_EN	R/W	1: select MII register 0: select EEPROM register This bit should not be enabled until the contents of MII registers are all filled with correct value.	0
12.6	B.4	UPDATE_R4_EN	R/W	Update_r4_en, Change capability enable A full duplex port will change its capability to half duplex, if the remote full duplex port does not support 802.3x and this function is enable. 1: enable, 0: disable	0
12.4	6.5	Reserved	R/W		0
12.3	6.4	AGING	R/W	Aging time, Aging time of address table selection An address tag in hashing table will be dropped if this function is turned on and its aging timer expires. Aging =bit[4] 0: no aging 1: aging time 300sec (default)	1
12.2	--	MII0_SPEED	RO	Speed of MII0 1: 100M 0: 10M It is speed of MII0 if P4_EXT is enabled. It is speed of port4 if P4EXT is disabled	0

MII	ROM	Function	R/W	Description	Default
MII register 12H (18D)					
12.1	--	MII0_FDX	RO	Speed of MII0 1: full duplex 0: half duplex It is duplex of MII0 if P4_EXT is enabled. It is duplex of port4 if P4EXT is disabled	0
12.0	6.6	Reserved	R/W		0

MII	ROM	Function	R/W	Description	Default
MII register 13H (19D)					
13.15	--		R/W	Don't care	0
13.14	E.6	P0_COS	R/W	Port0 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port0 are handled as high priority packets.	0
13.13	E.5	P0_HIGH	R/W	Port0 set to be high priority port 1: enable, 0: disabled (default) Packets received from port0 are handled as high priority packets.	0
13.12 ~ 13.7	--	Reserved		Don't care	
13.6	F.6	P1_COS	R/W	Port1 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port1 are handled as high priority packets.	0
13.5	F.5	P1_ HIGH	R/W	Port1 set to be high priority port 1: enable, 0: disabled (default) Packets received from port1 are handled as high priority packets.	0
13.4 ~ 13.0	--	Reserved		Don't care	

MII	ROM	Function	R/W	Description	Default
MII register 14H (20D)					
14.15	--		R/W	Don't care	0
14.14	10.6	P2_COS	R/W	Port2 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port2 are handled as high priority packets.	0
14.13	10.5	P2_ HIGH	R/W	Port2 set to be high priority port 1: enable, 0: disabled (default) Packets received from port2 are handled as high priority packets.	0

MII	ROM	Function	R/W	Description	Default
MII register 14H (20D)					
14.12 ~ 14.7	--	Reserved		Don't care	
14.6	11.6	P3_COS	R/W	Port3 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port3 are handled as high priority packets.	0
14.5	11.5	P3_ HIGH	R/W	Port3 set to be high priority port 1: enable, 0: disabled (default) Packets received from port3 are handled as high priority packets.	0
14.4 ~ 14.0	--	Reserved		Don't care	

MII	ROM	Function	R/W	Description	Default
MII register 15H (21D)					
15.15	--		R/W	Don't care	0
15.14	12.6	P4_COS	R/W	Port4 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port4 are handled as high priority packets.	0
15.13	12.5	P4_ HIGH	R/W	Port4 set to be high priority port 1: enable, 0: disabled (default) Packets received from port4 are handled as high priority packets.	0
15.12 ~ 15.0	--	Reserved		Don't care	

MII	ROM	Function	R/W	Description	Default
MII register 16H (22D) is reserved					
--	13.4	P4_FORCE	R/W	Port4 force mode enable 1: enable force mode 0: disable force mode, port4 NWAY with all capability	0
--	13.3	P3_FORCE	R/W	Port3 force mode enable 1: enable force mode 0: disable force mode, port3 NWAY with all capability	0
--	13.2	P2_FORCE	R/W	Port2 force mode enable 1: enable force mode 0: disable force mode, port2 NWAY with all capability	0
--	13.1	P1_FORCE	R/W	Port1 force mode enable 1: enable force mode 0: disable force mode, port1 NWAY with all capability	0

MII	ROM	Function	R/W	Description	Default
MII register 16H (22D) is reserved					
--	13.0	P0_FORCE	R/W	Port0 force mode enable 1: enable force mode 0: disable force mode, port0 NWAY with all capability	0
--	14.4	P4_FORCE100	R/W	Force port4 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p4_force (15h[15]) is set to 1'b1.	0
--	14.3	P3_FORCE100	R/W	Force port3 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p3_force (15h[14]) is set to 1'b1.	0
--	14.2	P2_FORCE100	R/W	Force port2 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p2_force (15h[13]) is set to 1'b1.	0
--	14.1	P1_FORCE100	R/W	Force port1 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p1_force (15h[12]) is set to 1'b1.	0
--	14.0	P0_FORCE100	R/W	Force port0 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p0_force (15h[11]) is set to 1'b1.	0
--	15.4	P4_FORCE_FULL	R/W	Force port4 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (15.15) is set to 1'b1.	0
--	15.3	P3_FORCE_FULL	R/W	Force port3 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (15.14) is set to 1'b1.	0
--	15.2	P2_FORCE_FULL	R/W	Force port2 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (15.13) is set to 1'b1.	0
--	15.1	P1_FORCE_FULL	R/W	Force port1 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (15.12) is set to 1'b1.	0
--	15.0	P0_FORCE_FULL	R/W	Force port0 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (15.11) is set to 1'b1.	0
16.0	--			Reserved	

MII	ROM	Function	R/W	Description	Default
MII register 17H (23D)					
17[15:11]	16[4:0]	Add VLAN tag	R/W	Add VLAN tag 17H[11] 1: port0 adds a VLAN tag to each outgoing packet. 0: port0 doesn't add a VLAN tag. 17H[12] 1: port1 adds a VLAN tag to each outgoing packet. 0: port1 doesn't add a VLAN tag. 17H[13] 1: port2 adds a VLAN tag to each outgoing packet. 0: port2 doesn't add a VLAN tag. 17H[14] 1: port3 adds a VLAN tag to each outgoing packet. 0: port3 doesn't add a VLAN tag. 17H[15] 1: port4 adds a VLAN tag to each outgoing packet. 0: port4 doesn't add a VLAN tag.	5'b0
17[10:6]	17[4:0]	Remove VLAN tag	R/W	Remove VLAN tag 17H[6] 1: port0 removes the VLAN tag from each outgoing packet. 0: port0 doesn't remove the VLAN tag. 17H[7] 1: port1 removes the VLAN tag from each outgoing packet. 0: port1 doesn't remove the VLAN tag. 17H[8] 1: port2 removes the VLAN tag from each outgoing packet. 0: port2 doesn't remove the VLAN tag. 17H[9] 1: port3 removes the VLAN tag from each outgoing packet. 0: port3 doesn't remove the VLAN tag. 17H[10] 1: port4 removes the VLAN tag from each outgoing packet. 0: port4 doesn't remove the VLAN tag.	5'b0

MII	ROM	Function	R/W	Description	Default
MII register 18H (24D)					
18[15:8]	19[7:0]	Port 0 vlan_tag[15:8]	R/W	Vlan_tag_0_high This register defines the high byte of VLAN tag for port 0.	8'b0
18[7:0]	18[7:0]	Port 0 vlan_tag[7:0]	R/W	Vlan_tag_0_low This register defines the low byte of VLAN tag for port 0.	8'b0

MII	ROM	Function	R/W	Description	Default
MII register 19H (25D)					
19[15:8]	1B[7:0]	Port 1 vlan_tag[15:8]	R/W	Vlan_tag_1_high This register defines the high byte of VLAN tag for port 1.	8'b0
19[7:0]	1A[7:0]	Port 1 vlan_tag[7:0]	R/W	Vlan_tag_1_low This register defines the low byte of VLAN tag for port 1.	8'b0

MII	ROM	Function	R/W	Description	Default
MII register 1AH (26D)					
1A[15:8]	1D[7:0]	Port 2 vlan_tag[15:8]	R/W	Vlan_tag_2_high This register defines the high byte of VLAN tag for port 2.	8'b0
1A[7:0]	1C[7:0]	Port 2 vlan_tag[7:0]	R/W	Vlan_tag_2_low This register defines the low byte of VLAN tag for port 2.	8'b0

MII	ROM	Function	R/W	Description	Default
MII register 1BH (27D)					
1B[15:8]	1F[7:0]	Port 3 vlan_tag[15:8]	R/W	Vlan_tag_3_high This register defines the high byte of VLAN tag for port 3.	8'b0
1B[7:0]	1E[7:0]	Port 3 vlan_tag[7:0]	R/W	Vlan_tag_3_low This register defines the low byte of VLAN tag for port 3.	8'b0

MII	ROM	Function	R/W	Description	Default
MII register 1CH (28D)					
1C[15:8]	21[7:0]	Port 4 vlan_tag[15:8]	R/W	Vlan_tag_4_high This register defines the high byte of VLAN tag for port 4.	8'b0
1C[7:0]	20[7:0]	Port 4 vlan_tag[7:0]	R/W	Vlan_tag_4_low This register defines the low byte of VLAN tag for port 4.	8'b0

MII	ROM	Function	R/W	Description	Default
MII register 1DH (29D)					
1D[15:12]	--		RO	Reserved	0
1D.11	--	Reserved	RO		1
1D.10	--	jab_on	R/W	Jabber enabled. 1: jabber function enabled 0: jabber function disabled	0
1D.9	--	heartbt_en,	R/W	Heartbeat enabled. 1: heartbeat function enabled 0: heartbeat function disabled	0
1D.8	--	reptr_en	R/W	Select NIC or repeater mode. 1: repeater mode 0: NIC mode	1
1D.7	--	lp_nway_able	RO	Link partner is auto-negotiation able. 1: link partner supports auto-negotiation 0: link partner doesn't support auto-negotiation	0
1D.6	--	polrev	RO	Analog transmit/receive signal polarity 1: RX+- polarity reversed 0: RX+- polarity not reversed	0
1D.5	--	phyaddr_fix	R/W	PHY address fix or not. 1: MII registers can be accessed only if the PHY address filed in management frame matches the content of MII register 29[4:0]. 0: MII registers can be accessed in spite of the PHY address.	0
1D[4:0]	--	phyaddr	R/W	Define PHY address	5'b0

4.11 EEPROM register

ROM	MII	Pin name	Description	Default
EEPROM registers 00~01H				
0[7:0] 1[7:0]	--	--	EEPROM enable register This register should be filled with 55AA. IP175A LF will check the specified pattern to confirm a valid EEPROM exists. The initial setting is updated after power on reset only if the specified pattern 55AA is found.	AA 55

ROM	MII	Pin name	Description (LED output selection register)	Default
EEPROM registers 02H				
2[7:2]	--	--	Reserved	6'b0
2[1:0]	12[15:14]	LED_SEL[1:0]	Led_sel, LED mode selection. LED_SEL[1:0]=00: LED mode 0, LED_SEL[1:0]=01: LED mode 1, LED_SEL[1:0]=10: LED mode 2, LED_SEL[1:0]=11: LED mode 3 (default) Please refer to pin description for detail LED definition.	11

ROM	MII	Pin name	Description	Default
EEPROM registers 03H				
3[7:0]	--	--	Reserved	8'b0

ROM	MII	Pin name	Description (Switch control register 1)	Default
EEPROM registers 04H				
4.7	12.13	X_en (LED_FULL[0])	X_en, IEEE 802.3x flow control enable This signal is used as pause_en for digital parts. 1: enable, 0:disable	1
4[6:5]	--	--	Reserved	2'b0
4.4	12.12	Bk_en (LED_LINK[1])	Bk_en, Backpressure enable 1: enable, 0: disable	1
4.3	12.10	Mac_x_en (RXD1_0)	Mac_x_en, External Mac port flow control enable 1: enable, 0:disable	1
4.2	12.11	Bf_stm_en (LED_SPEED[1])	Broadcast storm enable 1: enable Drop the incoming packet if the number of queued broadcast packet is over the threshold. The threshold is defined in register 0AH[14:13]. 0: disable	0

ROM	MII	Pin name	Description (Switch control register 1)	Default
EEPROM registers 04H				
4.1		Reserved		0
4.0		Reserved		1

ROM	MII	Pin name	Description (Switch control register 2)	Default
EEPROM registers 05H				
5[7:6]	--	--	Reserved	2'b0
5.5	--	--	Reserved	1'b0
5[4:3]	--	--	Bp_kind, Backpressure type selection It is valid only if Bk_en (02H[4]) is set to 1'b1. 00: carrier base backpressure 01: collision base backpressure with hashing 10: collision base backpressure without hashing	00
5[2:0]	--	--	Reserved	3'b0

ROM	MII	Pin name	Description (Switch control register 3)	Default
EEPROM registers 06H				
6.7	--	--	No drop16, A port will drop the transmitting packet after 16 consecutive collisions if this function is turned on. 1: do not drop, 0: drop	1
6.6	12.0	--		0
6.5	12.4	--		0
6.4	12.3	Aging (RXD1_2)	Agetime, Aging time of address table selection An address tag in hashing table will be dropped if this function is turned on and its aging timer expires. Aging =bit[4] 0: no aging 1: aging time 300sec (default)	1
6.2	--	--	Twopart, Turn on twopartD IP175A LF examine the carrier idle for 64 bits only when it is back off if this function is turned. 1: turn on, 0: turn off	1
6.1	--	--	Modbck, Turn on modified back off algorithm The maximum back off period is limited to 16-slot time if this function is turned on. 1: turn on (default), 0: turn off	1
6.0	--	--	Reserved	0

ROM	MII	Pin name	Description	Default
EEPROM registers 07H				
7[7:0]	--	--	Reserved	8'b0

ROM	MII	Pin name	Description (Transceiver control register 1)	Default
EEPROM registers 08H				
8[7:0]	--	--	Reserved	8'b0

ROM	MII	Pin name	Description (Transceiver control register 2)	Default
EEPROM registers 09H				
9[7:2]	--	--	Reserved	6'b0
9.1	--	--	Savepw_a_en, Save power mode Digital sends wake up signal to analog before sending FLP if this function is active. 0: disable, 1: enable The default value must be adopted for normal operation.	1
9.0	--	--	MDI/MDI-X enable 1: enable (default), 0:disable This function should be tuned on for normal operation. Disable MDIX is inhibited.	1

ROM	MII	Pin name	Description (Transceiver verification register 1)	Default
EEPROM registers 0AH				
A[7:6]	--	--	Reserved	00
A.5	--	--	Reserved	0
A.4	--	--	Reserved	0
A.3	--	--	Reserved	0
A.1	--	--	Reserved	0
A.0	--	--	Reserved	0

ROM	MII	Pin name	Description (Transceiver verification register 2)	Default
EEPROM registers 0BH				
B.7	--	--	Reserved	1'b0
B.6	--	--	Reserved	1'b0
B.5	--	--	Reserved	0

ROM	MII	Pin name	Description (Transceiver verification register 2)	Default
EEPROM registers 0BH				
B.4	12.6	Update_r4_en (LED_SPEED[0])	Update_r4_en, Change capability enable A full duplex port will change its capability to half duplex, if the remote full duplex port does not support 802.3x and this function is enable. 1: enable, 0: disable	0
B.3	--	--	Reserved	0
B.2	--	--	Reserved	0
B.1	--	--	Reserved	0
B.0	--	--	Reserved	0

ROM	MII	Pin name	Description (Testing & verify mode register 1)	Default
EEPROM registers 0CH				
C.7	--	--	Reserved	0
C.6	--	--	Reserved	0
C[5:0]	--	--	Reserved	6'b0

ROM	MII	Pin name	Description (Testing & verify mode register 2)	Default
EEPROM registers 0DH				
D[7:3]	--	--	Reserved	0
D.2	--	--	Reserved	1
D.1	--	--	Reserved	0
D.0	--	--	Reserved	0
D.0	--	--	Reserved	1

ROM	MII	Pin name	Description (VLAN register 0)	Default
EEPROM registers 0EH				
E.7	--	--	Don't care	
E.6	13.14	--	Port0 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port0 are handled as high priority packets.	1'b0
E.5	13.13	--	Port0 set to be high priority port 1: enable, 0: disabled (default) Packets received from port0 are handled as high priority packets.	1'b0

ROM	MII	Pin name	Description (VLAN register 0)	Default
EEPROM registers 0EH				
E.4	--	--	Port0 VLAN look up table The register defines the ports in the same VLAN with port0. The bit 0~4 are corresponding to port 0~4. 1: port 4 and port0 are in the same VLAN 0: port 4 and port0 are not in the same VLAN	1'b1
E.3	--	--	Port0 VLAN look up table 1: port 3 and port0 are in the same VLAN 0: port 3 and port0 are not in the same VLAN	1'b1
E.2	--	--	Port0 VLAN look up table 1: port 2 and port0 are in the same VLAN 0: port 2 and port0 are not in the same VLAN	1'b1
E.1	--	--	Port0 VLAN look up table 1: port 1 and port0 are in the same VLAN 0: port 1 and port0 are not in the same VLAN	1'b1
E.0	--	--	Don't care	1'b1

ROM	MII	Pin name	Description (VLAN register 1)	Default
EEPROM registers 0FH				
F.7	--	--	Don't care	
F.6	13.6	--	Port1 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port1 are handled as high priority packets.	1'b0
F.5	13.5	--	Port1 set to be high priority port 1: enable, 0: disabled (default) Packets received from port1 are handled as high priority packets.	1'b0
F.4	--	--	Port1 VLAN look up table The register defines the ports in the same VLAN with port1. The bit 8~12 are corresponding to port 0~4. 1: port 4 and port1 are in the same VLAN 0: port 4 and port1 are not in the same VLAN	1'b1
F.3	--	--	Port1 VLAN look up table 1: port 3 and port1 are in the same VLAN 0: port 3 and port1 are not in the same VLAN	1'b1
F.2	--	--	Port1 VLAN look up table 1: port 2 and port1 are in the same VLAN 0: port 2 and port1 are not in the same VLAN	1'b1
F.1	--	--	Don't care	
F.0	--	--	Port1 VLAN look up table 1: port 0 and port1 are in the same VLAN 0: port 0 and port1 are not in the same VLAN	1'b1

ROM	MII	Pin name	Description (VLAN register 2)	Default
EEPROM registers 10H				
10.7	--	--	Don't care	
10.6	14.14	--	Port2 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port2 are handled as high priority packets.	1'b0
10.5	14.13	--	Port2 set to be high priority port 1: enable, 0: disabled (default) Packets received from port2 are handled as high priority packets.	1'b0
10.4	--	--	Port2 VLAN look up table The register defines the ports in the same VLAN with port2. The bit 0~4 are corresponding to port 0~4. 1: port 4 and port2 are in the same VLAN 0: port 4 and port2 are not in the same VLAN	1'b1
10.3	--	--	Port2 VLAN look up table 1: port 3 and port2 are in the same VLAN 0: port 3 and port2 are not in the same VLAN	1'b1
10.2	--	--	Don't care	
10.1	--	--	Port2 VLAN look up table 1: port 1 and port2 are in the same VLAN 0: port 1 and port2 are not in the same VLAN	1'b1
10.0	--	--	Port2 VLAN look up table 1: port 0 and port2 are in the same VLAN 0: port 0 and port2 are not in the same VLAN	1'b1

ROM	MII	Pin name	Description (VLAN register 3)	Default
EEPROM registers 11H				
11.7	--	--	Don't care	
11.6	14.6	--	Port3 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port3 are handled as high priority packets.	1'b0
11.5	14.5	--	Port3 set to be high priority port 1: enable, 0: disabled (default) Packets received from port3 are handled as high priority packets.	1'b0
11.4	--	--	Port3 VLAN look up table The register defines the ports in the same VLAN with port3. The bit 8~12 are corresponding to port 0~4. 1: port 4 and port3 are in the same VLAN 0: port 4 and port3 are not in the same VLAN	1'b1
11.3	--	--	Don't care	
11.2	--	--	Port3 VLAN look up table 1: port 2 and port3 are in the same VLAN 0: port 2 and port3 are not in the same VLAN	1'b1

ROM	MII	Pin name	Description (VLAN register 3)	Default
EEPROM registers 11H				
11.1	--	--	Port3 VLAN look up table 1: port 1 and port3 are in the same VLAN 0: port 1 and port3 are not in the same VLAN	1'b1
11.0	--	--	Port3 VLAN look up table 1: port 0 and port3 are in the same VLAN 0: port 0 and port3 are not in the same VLAN	1'b1

ROM	MII	Pin name	Description (VLAN register 4)	Default
EEPROM registers 12H				
12.7	--	--	Don't care	
12.6	15.14	--	Port4 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port4 are handled as high priority packets.	1'b0
12.5	15.13	P4_high	Port4 set to be high priority port 1: enable, 0: disabled (default) Packets received from port4 are handled as high priority packets.	1'b0
12.4	--	--	Don't care	
12.3	--	--	Port4 VLAN look up table The register defines the ports in the same VLAN with port4. The bit 0~4 are corresponding to port 0~4. 1: port 3 and port4 are in the same VLAN 0: port 3 and port4 are not in the same VLAN	1'b1
12.2	--	--	Port4 VLAN look up table 1: port 2 and port4 are in the same VLAN 0: port 2 and port4 are not in the same VLAN	1'b1
12.1	--	--	Port4 VLAN look up table 1: port 1 and port4 are in the same VLAN 0: port 1 and port4 are not in the same VLAN	1'b1
12.0	--	--	Port4 VLAN look up table 1: port 0 and port4 are in the same VLAN 0: port 0 and port4 are not in the same VLAN	1'b1

ROM	MII	Pin name	Description	Default
EEPROM registers 13H				
13[7:5]	--	--	Don't care	
13.4	--	P4_FORCE	Port4 force mode enable 1: enable force mode 0: disable force mode, port4 NWAY with all capability	0

ROM	MII	Pin name	Description	Default
EEPROM registers 13H				
13.3	--	P3_FORCE	Port3 force mode enable 1: enable force mode 0: disable force mode, port3 NWAY with all capability	0
13.2	--	P2_FORCE	Port2 force mode enable 1: enable force mode 0: disable force mode, port2 NWAY with all capability	0
13.1	--	P1_FORCE	Port1 force mode enable 1: enable force mode 0: disable force mode, port1 NWAY with all capability	0
13.0	--	P0_FORCE	Port0 force mode enable 1: enable force mode 0: disable force mode, port0 NWAY with all capability	0

ROM	MII	Pin name	Description	Default
EEPROM registers 14H				
14[7:5]	--	--	Don't care	
14.4	--	P4_FORCE100	Force port4 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p4_force (13H[4]) is set to 1'b1.	0
14.3	--	P3_FORCE100	Force port3 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p3_force (13H[3]) is set to 1'b1.	0
14.2	--	P2_FORCE100	Force port2 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p2_force (13H[2]) is set to 1'b1.	0
14.1	--	P1_FORCE100	Force port1 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p1_force (13H[1]) is set to 1'b1.	0
14.0	--	P0_FORCE100	Force port0 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p0_force (13H[0]) is set to 1'b1.	0

ROM	MII	Pin name	Description	Default
EEPROM registers 15H				
15[7:5]	--	--	Don't care	
15.4	--	P4_FORCE_FULL	Force port4 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (13H[4]) is set to 1'b1. IP175A LF does not support "force 10M half mode".	0
15.3	--	P3_FORCE_FULL	Force port3 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (13H[3]) is set to 1'b1. IP175A LF does not support "force 10M half mode".	0
15.2	--	P2_FORCE_FULL	Force port2 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (13H[2]) is set to 1'b1. IP175A LF does not support "force 10M half mode".	0
15.1	--	P1_FORCE_FULL	Force port1 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (13H[1]) is set to 1'b1. IP175A LF does not support "force 10M half mode".	0
15.0	--	P0_FORCE_FULL	Force port0 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (13H[0]) is set to 1'b1. IP175A LF does not support "force 10M half mode".	0

ROM	MII	Pin name	Description	Default
EEPROM registers 16H				
16[4:0]	17[15:11]	--	Add VLAN tag 16H[0] 1: port0 adds a VLAN tag to each outgoing packet. 0: port0 doesn't add a VLAN tag. 16H[1] 1: port1 adds a VLAN tag to each outgoing packet. 0: port1 doesn't add a VLAN tag. 16H[2] 1: port2 adds a VLAN tag to each outgoing packet. 0: port2 doesn't add a VLAN tag. 16H[3] 1: port3 adds a VLAN tag to each outgoing packet. 0: port3 doesn't add a VLAN tag. 16H[4] 1: port4 adds a VLAN tag to each outgoing packet. 0: port4 doesn't add a VLAN tag.	5'b0

ROM	MII	Pin name	Description	Default
EEPROM registers 17H				
17[4:0]	17[10:6]	--	Remove VLAN tag 17H[0] 1: port0 removes the VLAN tag from each outgoing packet. 0: port0 doesn't remove the VLAN tag. 17H[1] 1: port1 removes the VLAN tag from each outgoing packet. 0: port1 doesn't remove the VLAN tag. 17H[2] 1: port2 removes the VLAN tag from each outgoing packet. 0: port2 doesn't remove the VLAN tag. 17H[3] 1: port3 removes the VLAN tag from each outgoing packet. 0: port3 doesn't remove the VLAN tag. 17H[4] 1: port4 removes the VLAN tag from each outgoing packet. 0: port4 doesn't remove the VLAN tag.	5'b0

ROM	MII	Pin name	Description	Default
EEPROM registers 18H~21H				
18[7:0]	18[7:0]	--	Vlan_tag_0_low This register defines the low byte of VLAN tag for port 0. (i.e. Port 0 vlan_tag[7:0])	8'b0
19[7:0]	18[15:8]	--	Vlan_tag_0_high This register defines the high byte of VLAN tag for port 0. (i.e. Port 0 vlan_tag[15:8])	8'b0
1A[7:0]	19[7:0]	--	Vlan_tag_1_low This register defines the low byte of VLAN tag for port 1. (i.e. Port 1 vlan_tag[7:0])	8'b0
1B[7:0]	19[15:8]	--	Vlan_tag_1_high This register defines the high byte of VLAN tag for port 1. (i.e. Port 1 vlan_tag[15:8])	8'b0
1C[7:0]	1A[7:0]	--	Vlan_tag_2_low This register defines the low byte of VLAN tag for port 2. (i.e. Port 2 vlan_tag[7:0])	8'b0
1D[7:0]	1A[15:8]	--	Vlan_tag_2_high This register defines the high byte of VLAN tag for port 2. (i.e. Port 2 vlan_tag[15:8])	8'b0
1E[7:0]	1B[7:0]	--	Vlan_tag_3_low This register defines the low byte of VLAN tag for port 3. (i.e. Port 3 vlan_tag[7:0])	8'b0
1F[7:0]	1B[15:8]	--	Vlan_tag_3_high This register defines the high byte of VLAN tag for port 3. (i.e. Port 3 vlan_tag[15:8])	8'b0

ROM	MII	Pin name	Description	Default
EEPROM registers 18H~21H				
20[7:0]	1C[7:0]	--	Vlan_tag_4_low This register defines the low byte of VLAN tag for port 4. (i.e. Port 4 vlan_tag[7:0])	8'b0
21[7:0]	1C[15:8]	--	Vlan_tag_4_high This register defines the high byte of VLAN tag for port 4. (i.e. Port 4 vlan_tag[15:8])	8'b0

ROM	MII	Pin name	Description (Testing & verify mode register 3)	Default
EEPROM registers 22H				
22[7:6]	--	--	Reserved	2'b01
22[5:4]	--	--	Reserved	2'b00
22[3:0]	--	--	Reserved	4'b0000

ROM	MII	Pin name	Description (Testing & verify mode register 4)	Default
EEPROM registers 23H				
23[7:0]	--	--	Reserved	8'h00

ROM	MII	Pin name	Description (Testing & verify mode register 5)	Default
EEPROM registers 24H				
24[7:0]	--	--	Reserved	8'h01

4.12 The basic MII registers

Type	Description
R/W	Read/Write
SC	Self-Clearing
RO	Read Only

Type	Description
LL	Latching Low
LH	Latching High

Bit	Function	R/W	Description	Default
MII control register (address 00H)				
15	Reset		Not supported	0
14	Loop back	R/W	1 = Loopback mode 0 = normal operation When this bit set, IP175A LF will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN.	0
13	Speed Selection	RW	1 = 100Mbps 0 = 10Mbps It is valid only if bit 0.12 is set to be 0.	1
12	Auto-Negotiation Enable	RW	1 = Auto-Negotiation Enable 0 = Auto-Negotiation Disable If port 4 is a fiber port, FXSD higher than 0.6v, this bit is fixed at 0.	1
11	Power Down	R/W	Not supported	0
10	Isolate		Not supported	0
9	Restart Auto-Negotiation	RW SC	1 = re-starting Auto-Negotiation 0 = Auto-Negotiation re-start complete Setting this bit to logic high will cause IP175A LF to restart an Auto-Negotiation cycle, but depending on the value of bit 0.12 (Auto-Negotiation Enable). If bit 0.12 is cleared then this bit has no effect, and it is Read Only. This bit is self-clearing after Auto-Negotiation process is completed.	0
8	Duplex mode	R/W	1 = full duplex 0 = half duplex It is valid only if bit 0.12 is set to be 0.	0
7	Collision test	R/W	Not supported	0
6:0	Reserved	R/W	Write as 0, ignore on read	-

Bit	Function	R/W	Description	Default
MII status register (address 01H)				
15	100Base-T4 capable	RO	1 = 100Base-T4 capable 0 = not 100Base-T4 capable IP175A LF does not support 100Base-T4. This bit is fixed to be 0.	0

Bit	Function	R/W	Description	Default
MII status register (address 01H)				
14	100Base-X full duplex Capable	RO	1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable The default of this bit will change depend on the external setting of IP175A LF. If external pin setting without 100Base-X full duplex support, then this bit will change default to logic 0.	1
13	100Base-X half duplex Capable	RO	1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable The default of this bit will change depend on the external setting of IP175A LF. If external pin setting without 100Base-X half duplex support, then this bit will change default to logic 0	1
12	10Base-T full duplex Capable	RO	1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable The default of this bit will change depend on the external setting of IP175A LF. If external pin setting without 100Base-T full duplex support, then this bit will change default to logic 0	1
11	10Base-T half duplex Capable	RO	1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable The default of this bit will change depend on the external setting of IP175A LF. If external pin setting without 100Base-X full duplex support, then this bit will change default to logic 0	1
10:7	Reserved	RO	Ignore on read	-
6	MF preamble Suppression	RO	1 = preamble may be suppressed 0 = preamble always required	1
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0.	0
4	Remote fault	RO LH	1 = remote fault detected 0 = not remote fault detected When read as logic 1, indicates that IP175A LF has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP175A LF reset.	0
3	Auto-Negotiation Ability	RO	1 = Auto-Negotiation capable 0 = not Auto-Negotiation capable When read as logic 1, indicates that IP175A LF has the ability to perform Auto-Negotiation. The value of this bit will depend on the external mode setting of IP175A LF operation mode.	1

Bit	Function	R/W	Description	Default
MII status register (address 01H)				
2	Link Status	RO LL	1 = Link Pass 0 = Link Fail When read as logic 1, indicates that IP175A LF has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.	0
1	Jabber Detect		1 = jabber condition detected 0 = no jabber condition detected When read as logic 1, indicates that IP175A LF has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP113A reset. This bit is set until jabber condition is cleared and reading the contents of the register.	0
0	Extended capability	RO	1 = Extended register capabilities 0 = No extended register capabilities IP175A LF has extended register capabilities.	1

Bit	Function	R/W	Description	Default
PHY Identifier (address 02H)				
15:0	PHY identifier	RO	IP175A LF OUI (Organizationally Unique Identifier) ID, the msb is 3rd bit of IP175A LF OUI ID, and the lsb is 18th bit of IP175A LF OUI ID. IP175A LF OUI is 0090C3.	0243h

Bit	Function	R/W	Description	Default
PHY Identifier (address 03H)				
15:10	PHY identifier	RO	IP175A LF OUI ID, the msb is 19th bit of IP175A LF OUI ID, and lsb is 24th bit of IP175A LF OUI ID.	3h
9:4	Manufacture's Model Number	RO	IP175A LF model number	05h
3:0	Revision Number	RO	IP175A LF revision number	0

Bit	Function	R/W	Description	Default
Auto-Negotiation Advertisement register (address 04H)				
15	Next Page		Not supported	0
14	Reserved	RW	Reserved by IEEE, write as 0, ignore on read	0
13	Remote Fault	R/W	Not supported	0
12:11	Reserved	RO	Reserved for future IEEE use, write as 0, ignore on read	0
10	Pause	RW	1 = Advertises that this device has implemented pause function 0 = No pause function supported	0
9	100BASE-T4	RW	Not supported	0

Bit	Function	R/W	Description	Default
Auto-Negotiation Advertisement register (address 04H)				
8	100BASE-TX full duplex	R/W	1 = 100BASE-TX full duplex is supported 0 = 100BASE-TX full duplex is not supported	1
7	100BASE-TX	R/W	1 = 100BASE-TX is supported 0 = 100BASE-TX is not supported	1
6	10BASE-T full duplex	R/W	1 = 10BASE-T full duplex is supported 0 = 10BASE-T full duplex is not supported	1
5	10BASE-T	R/W	1 = 10BASE-T is supported 0 = 10BASE-T is not supported	1
4:0	Selector Field	R/W	Use to identify the type of message being sent by Auto-Negotiation.	00001

Bit	Function	R/W	Description	Default
Link partner ability register (address 05H) Base Page				
15	Next Page	RO	1 = Next Page ability is supported by link partner 0 = Next Page ability does not supported by link partner	0
14	Acknowledge	RO	1 = Link partner has received the ability data word 0 = Not acknowledge	0
13	Remote Fault	RO	1 = Link partner indicates a remote fault 0 = No remote fault indicate by link partner If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1.	0
12:11	Reserved	RO	Reserved by IEEE for future use, write as 0, read as 0.	0
10	Pause	RO	1 = Link partner support IEEE802.3x 0 = Link partner does not support IEEE802.3x IP175A LF will reload the default value after rest or link failure.	1
9	100BASE-T4	RO	1 = Link partner support 100BASE-T4 0 = Link partner does not support 100BASE-T4	0
8	100BASE-TX full duplex	RO	1 = Link partner support 100BASE-TX full duplex 0 = Link partner does not support 100BASE-TX full duplex	0
7	100BASE-TX	RO	1 = Link partner support 100BASE-TX 0 = Link partner does not support 100BASE-TX	0
6	10BASE-T full duplex	RO	1 = Link partner support 10BASE-T full duplex 0 = Link partner does not support 10BASE-T full duplex	0
5	10BASE-T	RO	1 = Link partner support 10BASE-T 0 = Link partner does not support 10BASE-T	0
4:0	Selector Field	RO	Protocol selector of the link partner	00000

4.13 LED Blink Timming

LED mode	Blinking speed
Active led blink	On -> Off 80ms -> On 20ms -> Off 80ms …
Collision led blink	Off -> On 20ms -> Off 80ms ->On 20ms …
Neon like LED(initial setup LED)	On 250ms -> Off 1.25s -> On 250ms -> Off 1.25s …

5 Electrical Characteristics

5.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	–0.3V to 4.0V
Input Voltage	–0.3V to 5.0V
Output Voltage	–0.3V to 5.0V
Storage Temperature	-65°C to 150°C
Ambient Operating Temperature (Ta)	0°C to 70°C

5.2 DC Characteristic

Operating Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	2.0	2.15	2.625	V	
Supply Voltage	VCC_IO	3.1		3.5	V	Pin 120 REG_OUT is not used.
Supply Voltage	VCC_IO	3.3		3.5	V	Pin 120 REG_OUT is used.
Operation Junction Temperature	Tj	0	70	125	℃	
Power Consumption			1.485		W	VCC=2.25v

Input Clock

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency			25		MHz	
Frequency Tolerance		-50		+50	PPM	

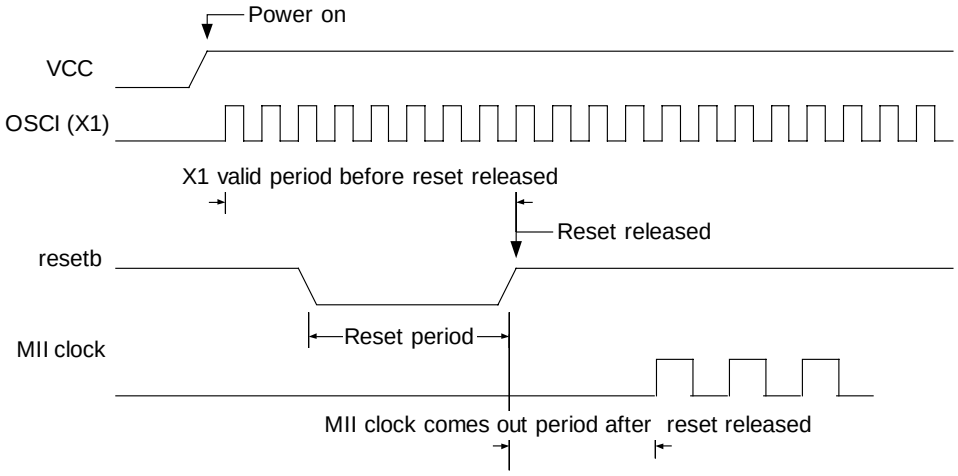
I/O Electrical Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOH=4mA, VCC_IO_x=3.3V
Output High Voltage	VOH	2.4			V	IOL=4mA, VCC_IO_x=3.3V

5.3 AC Timing

5.3.1 Reset Timing

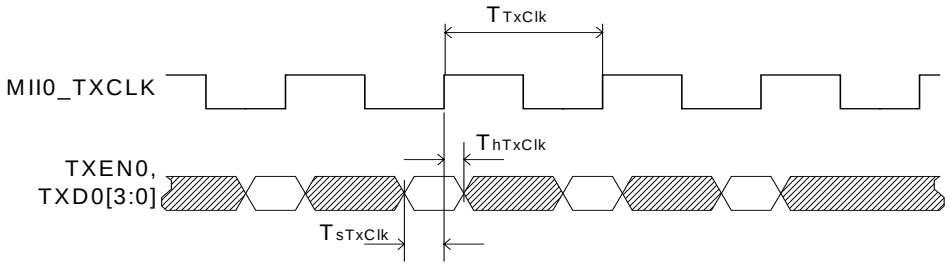
Description	Min.	Typ.	Max.	Unit
X1 valid period before reset released	10	-	-	ms
Reset period	10	-	-	ms
MII clock comes out period after reset released	-	1	-	µs



5.3.2 MII0 PHY Mode Timing

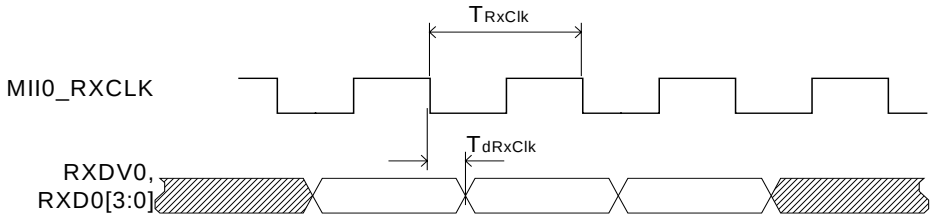
a. Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100M MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10M MII	-	400	-	ns
T_{sTxClk}	TXEN0, TXD0 to MII0_TXCLK setup time	2	-	-	ns
T_{hTxClk}	TXEN0, TXD0 to MII0_TXCLK hold time	0.5	-	-	ns



b. Receive Timing

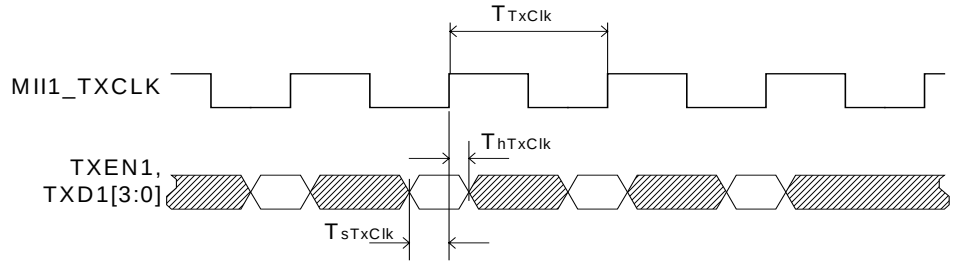
Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100M MII	-	40	-	ns
T_{RxClk}	Receive clock period 10M MII	-	400	-	ns
T_{dRxClk}	MII0_RXCLK falling edge to RXDV0, RXD0	1	-	4	ns



5.3.3 MII1 PHY Mode Timing

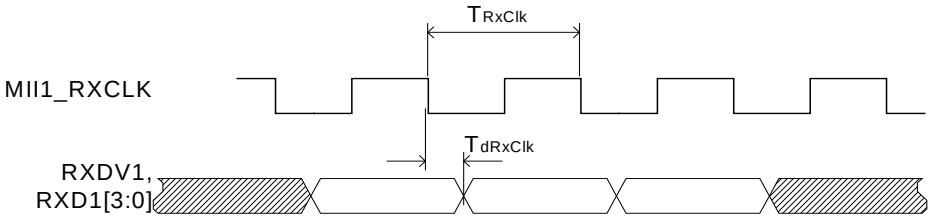
a. Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100M MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10M MII	-	400	-	ns
T_{sTxClk}	TXEN, TXD to MII1_TXCLK setup time	2	-	-	ns
T_{hTxClk}	TXEN, TXD to MII1_TXCLK hold time	0.5	-	-	ns



b. Receive Timing

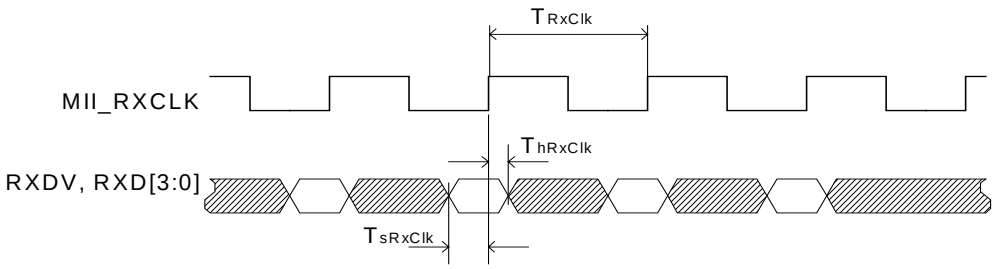
Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100M MII	-	40	-	ns
T_{RxClk}	Receive clock period 10M MII	-	400	-	ns
T_{dRxClk}	MII1_RXCLK falling edge to RXDV1, RXD1	1	-	4	ns



5.3.4 MII0 MAC Mode Timing

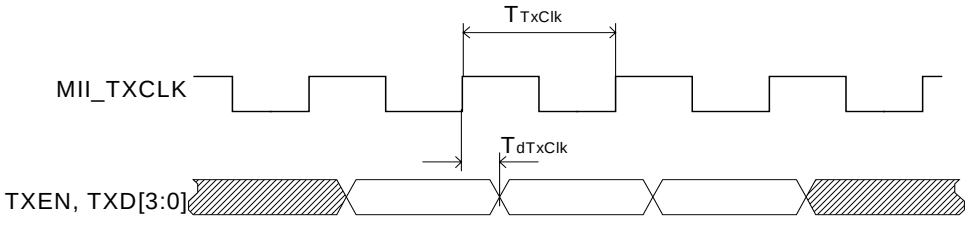
a. Receive Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100M MII	-	40	-	ns
T_{RxClk}	Receive clock period 10M MII	-	400	-	ns
T_{sRxClk}	RXDV, RXD to MII_RXCLK setup time	2	-	-	ns
T_{hRxClk}	RXDV, RXD to MII_RXCLK hold time	0.5	-	-	ns



b. Transmit Timing

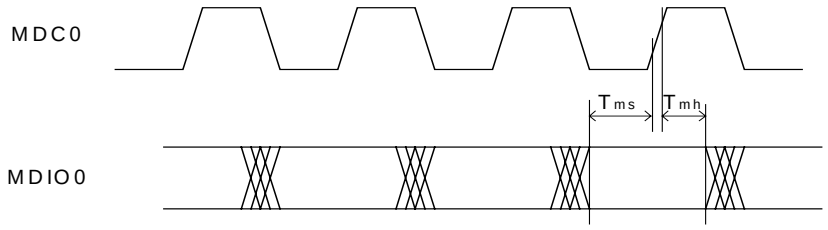
Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100M MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10M MII	-	400	-	ns
T_{dTxClk}	MII_TXCLK rising edge to TXEN, TXD	1	-	4	ns



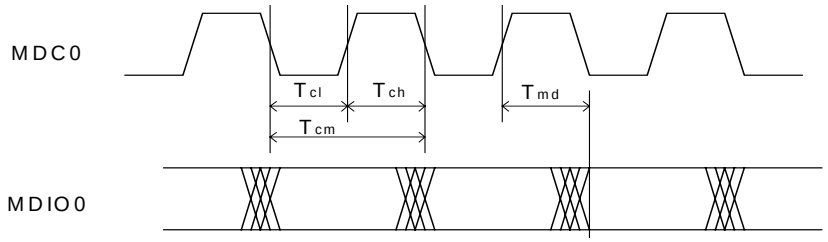
5.3.5 SMI Timing

a. MDC0/MDIO0 Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC0 High Time	40	-	-	ns
T_{cl}	MDC0 Low Time	40	-	-	ns
T_{cm}	MDC0 period	80	-	-	ns
T_{md}	MDIO0 output delay	-	-	5	ns
T_{mh}	MDIO0 setup time	10	-	-	ns
T_{ms}	MDIO0 hold time	10	-	-	ns



Write Cycle

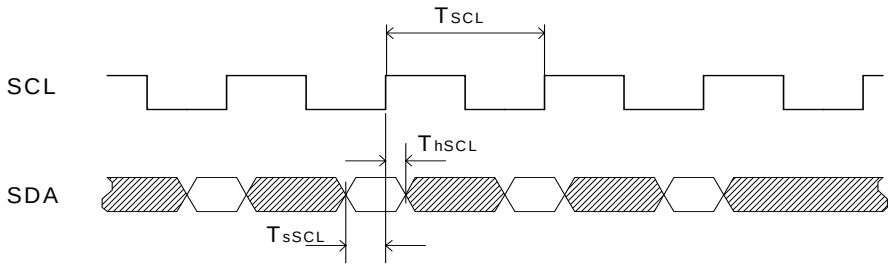


Read Cycle

5.3.6 EEPROM Timing

a.

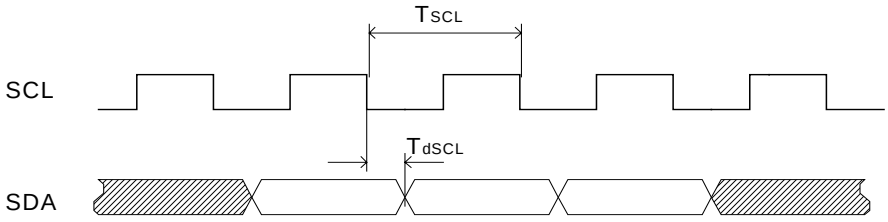
Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	20480	-	ns
T_{sSCL}	SDA to SCL setup time	2	-	-	ns
T_{hSCL}	SDA to SCL hold time	0.5	-	-	ns



Read data cycle

b.

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	20480	-	ns
T_{dSCL}	SCL falling edge to SDA	-	-	5200	ns



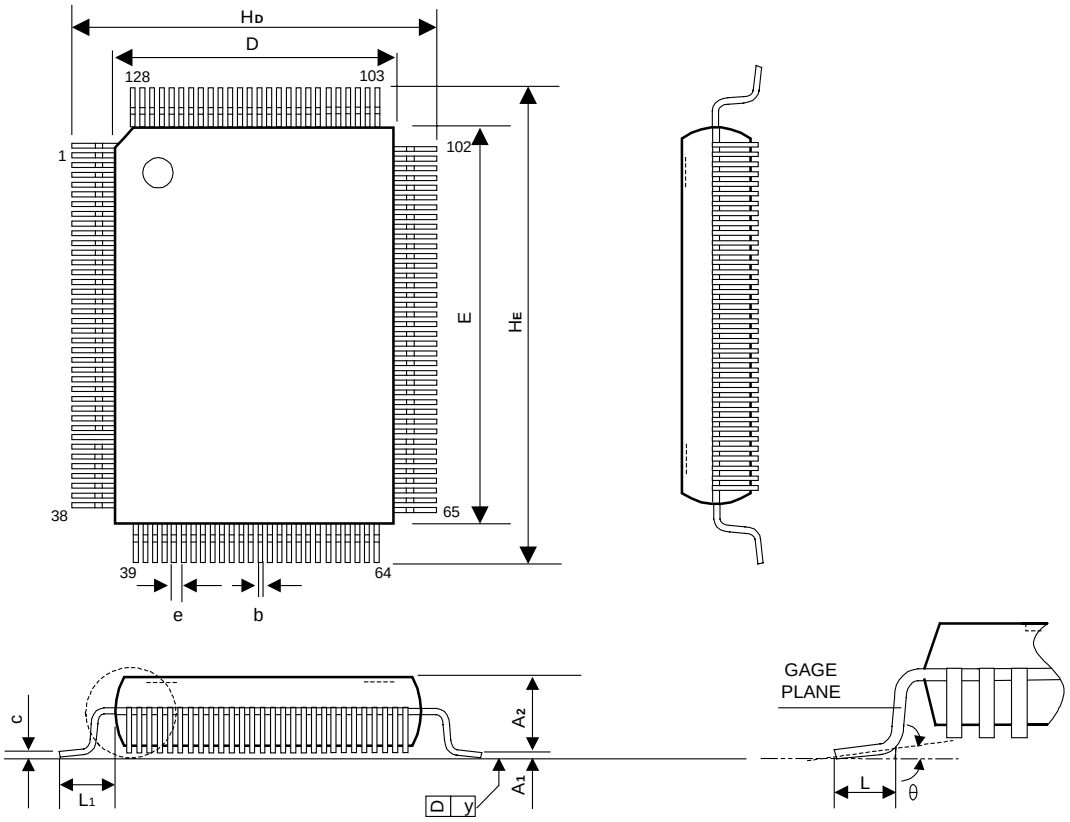
Comand cycle

6 Order Information

Part No.	Package	Notice
IP175A	128-PIN QFP	-
IP175A LF	128-PIN QFP	Lead free

7 Package Detail

128 PQFP Outline Dimensions



Symbol	Dimensions In Inches			Dimensions In mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A1	0.010	0.014	0.018	0.25	0.35	0.45
A2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.09	0.15	0.20
HD	0.669	0.677	0.685	17.00	17.20	17.40
D	0.547	0.551	0.555	13.90	14.00	14.10
HE	0.906	0.913	0.921	23.00	23.20	23.40
E	0.783	0.787	0.791	19.90	20.00	20.10
e	-	0.020	-	-	0.50	-
L	0.025	0.035	0.041	0.65	0.88	1.03
L1	-	0.063	-	-	1.60	-
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Note:
1. Dimension D & E do not include mold protrusion.
2. Dimension B does not include dambar protrusion. Total in excess of the B dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.

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