# 5 Port 10/100 Ethernet Integrated Switch

## Features

- IP175A PCB compatible (pins compatible)
- Built in 6 MAC and 5 PHY
- Each port can be configured to be 10Base-T, 100Base-TX
- 2k MAC address
- Support auto-polarity for 10Mbps
- Filter/ forward reserved address option
- Broadcast storm protection
- Auto MDI-MDIX
- Support three MII/RMII ports
- Support SMI with MDC up to 12.5 Mhz
- Support tagging & un-tagging
- Support Port base VLAN & tag VLAN
- Support CoS
- Support port security option
- Support SMART MAC function
- Support spanning tree protocol
- Max packet length 1552/ 1536 bytes
- Support 8-level bandwidth control
- Support Link quality LED for 100Mbps
- Support direct, serial and dual color mode LED
- Built in linear regulator control circuit
- Low power consumption
- 0.18um, 128-pin PQFP

## General Description

IP175B integrates a 6-port switch controller, SSRAM, and 5 10/100 Ethernet transceivers. Each of the transceivers complies with the IEEE802.3, IEEE802.3u, and IEEE802.3x specifications. The DSP approach is utilized for designing transceivers with 0.18um technology; they have high noise immunity and robust performance.

IP175B operates in store and forward mode. It supports flow control, auto MDI/MDI-X, CoS, port base VLAN, bandwidth control, DiffServ, SMART MAC and LED functions, etc. Each port can be configured to auto-negotiation or forced 10M/100M, full/half duplexmode. Using an EEPROM or pull up/down resistors on specified pins can configure the desired options.

Besides a 5-port switch application, IP175B supports three MII/RMII ports for router application, which supports 4 LAN ports, one WAN port and one HOME/PNA or Access point. The external MAC can monitor or configure IP175B by accessing MII registers through SMI0.

MII/RMII port also can be configured to be MAC mode. It is used to interface an external PHY to work as a 5+1 switch. Through SMI1 IP175B can monitor and configure external PHY.

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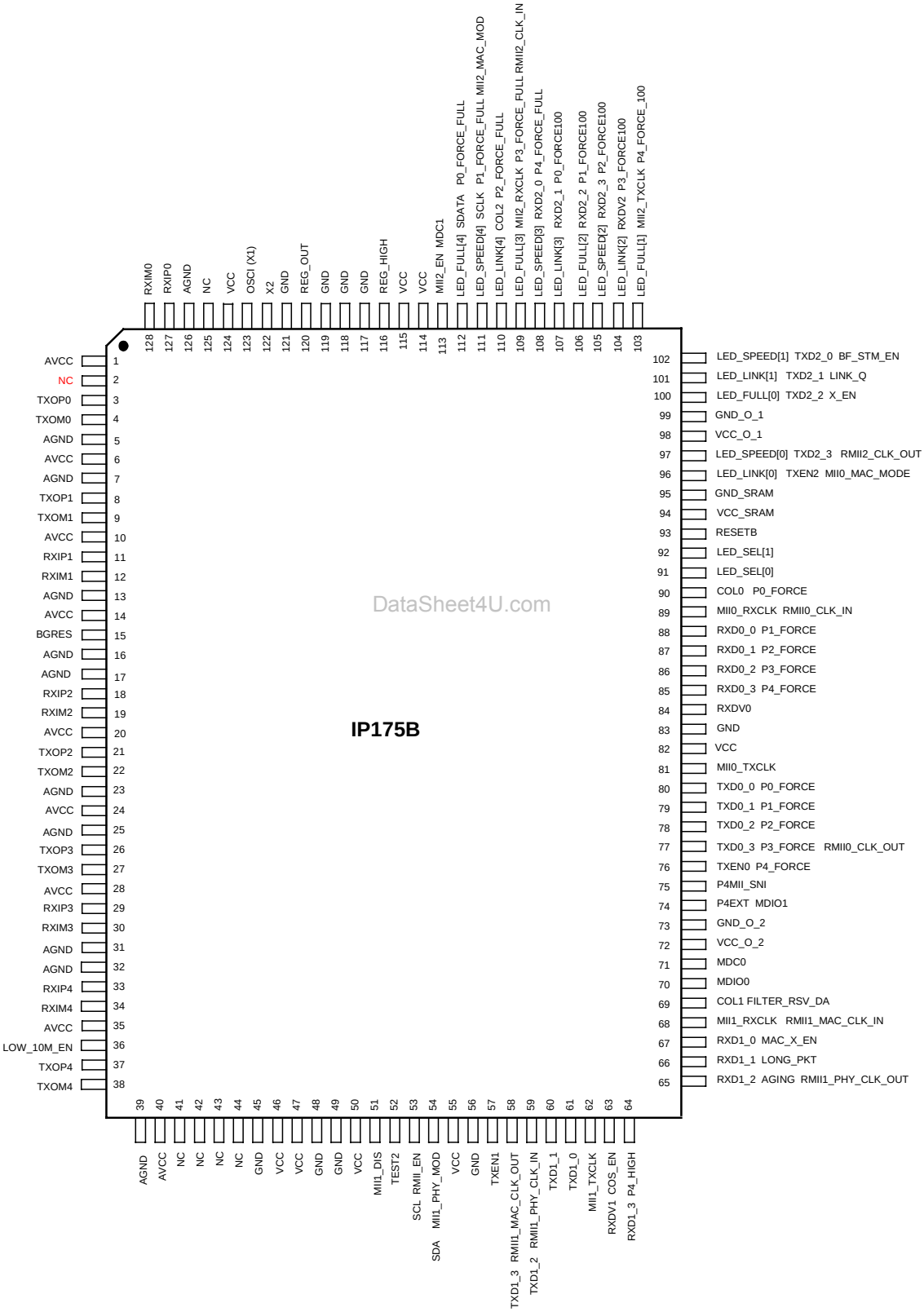
## Revision History

| Revision # | Change Description |
|---|---|
| IP175B-DS-R01 | Advanced Product Information |

## Comparison Table of IP175A & IP175B

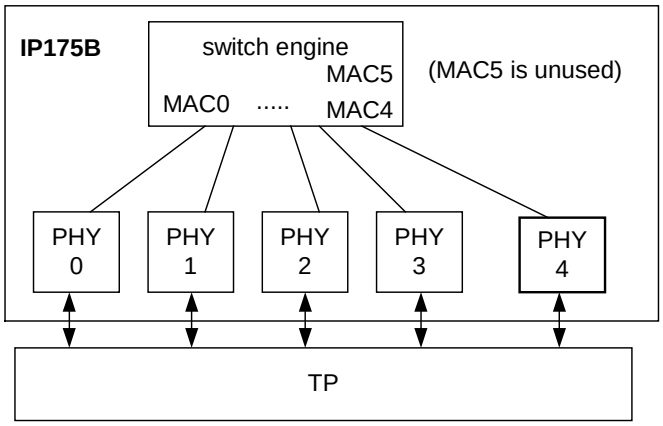
| Item/Part Number | IP175A | IP175B |
|---|---|---|
| **Pin Assignment** | **Compatible** | |
| Process | 0.25um | 0.18um |
| Package Type | 128pin PQFP | 128pin PQFP |
| Major Block | MAC/5ports+PHY/5ports | MAC/6ports+PHY/5ports |
| MAC Address | 1K | 2K |
| AUTO-MDI-MDIX | Yes | Yes |
| 10M/100M Copper (10BT, 100BaseTx) | Yes | Yes |
| 100M Fiber (100BaseFX) | Yes | No |
| Max Frame Size | 1536 | 1536/1552 (Pin Option) |
| 4+1+1: 4Tx+Two MII I/F (RMII I/F) | Yes (No) | Yes (Yes, MII0, 1 & 2) |
| 4+ 3MII | No | Yes |
| 5+1: 5Tx+1 MII I/F | No | Yes |
| SMI I/F(MDC/MDIO) CTRL PHY reg. | Yes (As data Sheet) | Yes (MDC/MDIO*2) |
| SNI I/F | Yes | Yes (MII0/SNI Option) |
| EEPROM I/F (24C01A) | Yes | Yes |
| Flow Control-802.3x | Yes | Yes |
| Flow Control-Backpressure | Yes | Yes |
| Port Base COS | Yes | Yes (Through SMI0) |
| Port Base VLAN | Yes | Yes (Through SMI0) |
| QOS- VLAN tag | Yes | Yes (Through SMI0) |
| Tag VLAN | No | Yes |
| QOS IPV4 TCP/IP Cos | Yes | Yes |
| QOS IPV6 TCP/IP Cos | No | Yes |
| Broadcast Storm Protection | Yes | Yes |
| Power Saving | Yes | Yes |
| Loop Back Test | PHY of port 5 | Each port |
| Port Security Option | No | Yes |
| 8-level Bandwidth Control | No | Yes |
| Link Quantity LED | No | Yes |
| Power down | No | Yes |
| Dual color mode LED | No | Yes |
| Spanning Tree protocol | No | Yes |
| Smart MAC | No | Yes |
| Special address handling | No | Yes |
| Diff serve | No | Yes |
| Direct forwarding | No | Yes |

## Pin diagram



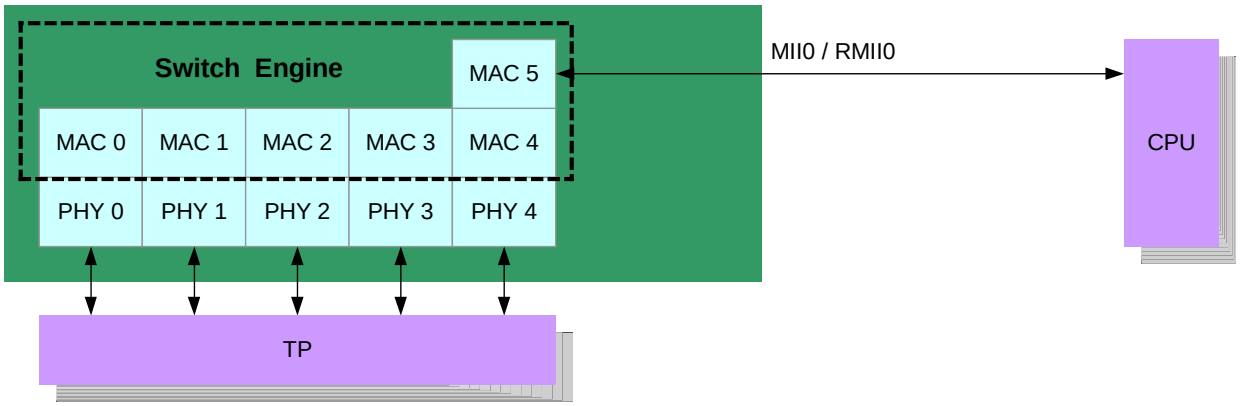
**5-port switch application**

When pin 74 P4EXT is pulled low, all MII/RMII ports are disabled, and IP175B works as a 5-port switch. MAC5 is not used in this application.



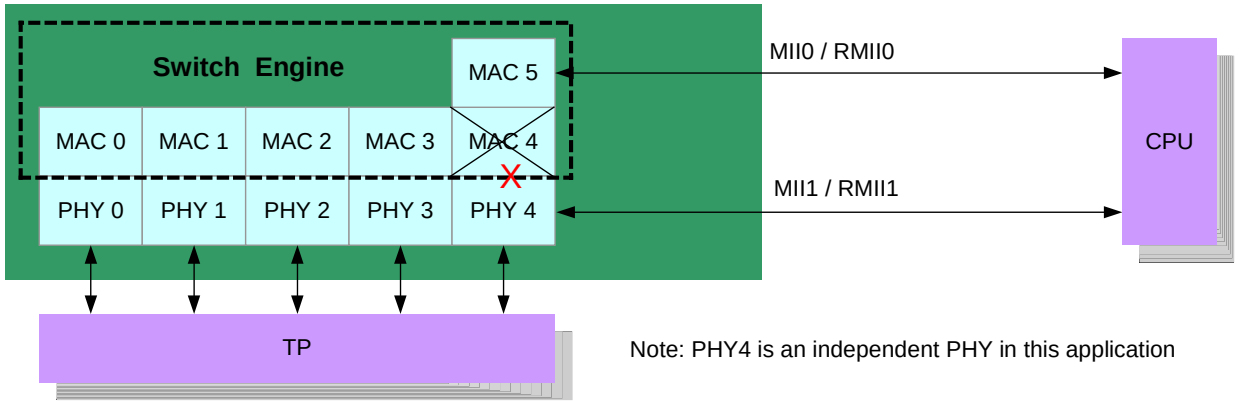
**Router application using one MII/RMII port**
(can be configured to 4LAN+1WAN, 3LAN+2WAN, 2LAN+3WAN or 1LAN+4WAN)

| p4ext | mii1_dis | mii2_en | p4mii_sni | rmii_en | mii0_mac_mod | mii2_mac_mod |
|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | x | 0 | x |




**Router application using two-MII/RMII ports**

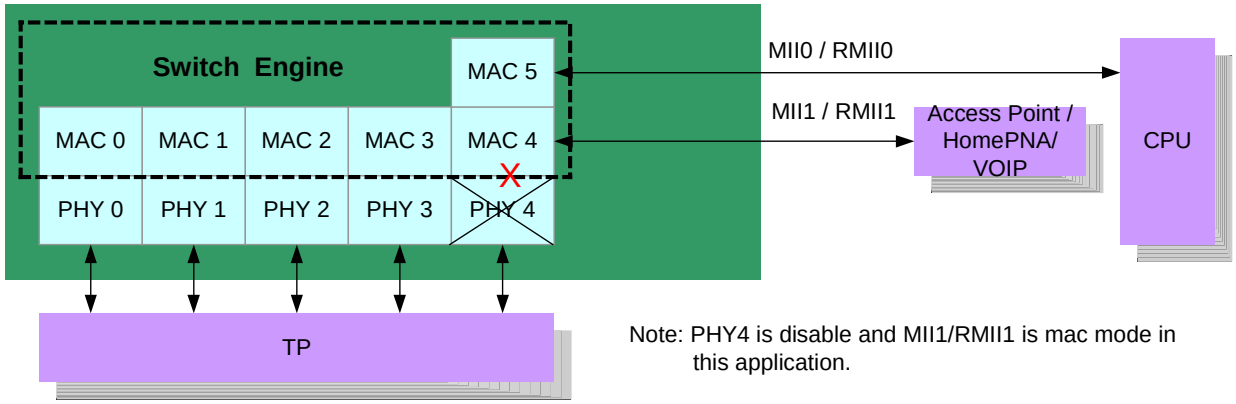
| p4ext | mii1_dis | mii2_en | p4mii_sni | rmii_en | mii0_mac_mod | mii2_mac_mod |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | x | 0 | x |




Note: PHY4 is an independent PHY in this application

**Router application using two-MII/RMII ports (another option)**

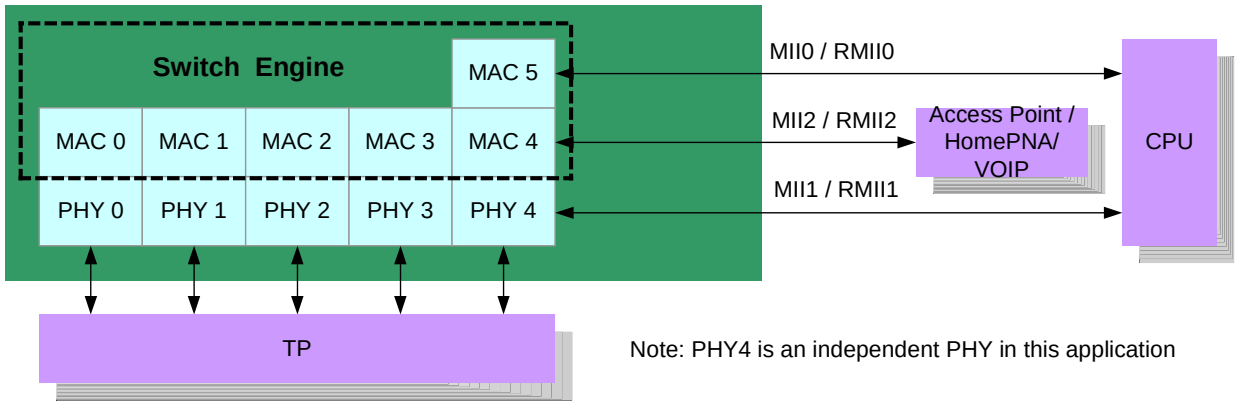
| p4ext | mii1_dis | mii2_en | p4mii_sni | rmii_en | mii0_mac_mod | mii1_phy_mod |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | x | 0 | 0 |




Note: PHY4 is disable and MII1/RMII1 is mac mode in this application.

**Router application using three-MII/RMII ports**

| p4ext | mii1_dis | mii2_en | p4mii_sni | rmii_en | mii0_mac_mod | mii2_mac_mod |
|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | x | 0 | 0 |




Note: PHY4 is an independent PHY in this application

## 1 Pin description

| Type | Description |
|---|---|
| I | Input pin |
| O | Output pin |
| IPL | Input pin with internal pull low |
| IPH | Input pin with internal pull high |

| Type | Description |
|---|---|
| IPL1 | Input pin with internal pull low 22.8k ohm |
| IPH1 | Input pin with internal pull high 22.8k ohm |
| IPL2 | Input pin with internal pull low 92.6k ohm |
| IPH2 | Input pin with internal pull high 113.8k ohm |

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **Analog** | | | |
| 120 | REG_OUT | O | Regulator output<br><br>The internal linear regulator uses this pin to control external transistor to generates a voltage source between 1.70v ~ 1.93v.<br><br>IP175B uses the DVCC/AVCC as feedback voltage. |
| 116 | REG_HIGH | I | Regulator output selection is internally bounded to GND. |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **LED pins used as initial setting (the setting is latched at the end of reset)** | | | |
| 102 | BF_STM_EN | IPL1 | Broadcast storm protection enable<br>1: enable,<br>0: disable (default)<br><br>A port begins to drop packets if it receives broadcast packets more than the threshold defined in MII register 30.11[15:14] bq_stm_thr_sel [1:0] or EEPROM register 59[7:6]. |
| 101 | LINK_Q | IPH1 | Link quality<br>1: enable (default),<br>0: disable<br><br>When the function is enabled, besides link on/off status, activity status, link LED shows link quality. The link LED will be flash (on: 2sec / off: 2sec) when the SNR of received signal is lower than the desired value for normal operation. |
| 100 | X_EN | IPH1 | IEEE802.3X/ back pressure enable<br>1: enable (default),<br>0: disable<br><br>This pin doesn't set the flow control of MII0 port. Pin 67 MAC_X_EN sets the flow control of MII0 port. |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **MII pins used as initial setting (the setting is latched at the end of reset)** | | | |
| 69 | FILTER_RSV _DA | IPL | Filter packets with reserved DA (0180c20002~f)<br>1: Filter the packets,<br>0: Forward the packets (default).<br><br>It is valid only if p4ext is pulled LOW. |
| 66 | LONG_PKT | IPL | Max forwarded packet length<br>1: 1552 bytes<br>0: 1536 bytes (default)<br><br>It is valid only if p4ext is pulled low. |
| 65 | AGING | IPH2 | Address aging enable<br>1: enable, aging time is around 280s (default),<br>0: disable<br><br>It is recommended to disable the aging function, if port-locking function is enabled.<br><br>It is valid only if p4ext is pulled low. |
| 64 | P4_HIGH | IPL2 | Port4 is set to be high priority port<br>1: enable,<br>0: disabled (default)<br><br>Packets received from port4 are handled as high priority packets if the feature is enabled.<br><br>It is valid only if p4ext is pulled low. |
| 63 | COS_EN | IPL2 | Class of service enable<br>1: enable,<br>0: disabled (default)<br><br>Packets with high priority tag are handled as high priority packets for all ports if the feature is enabled.<br><br>It is valid only if p4ext is pulled low. |

**Pin description** (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **Initial setting** | | | |
| 36 | LOW_10M_EN | IPL | 10M low power mode enable<br>1: 10M low power mode, the trasmit amplitude is depressed in 10M mode for power saving.<br>0: 10M normal mode (default) |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External MII port setting (the setting is latched at the end of reset)** | | | |
| 74 | P4EXT | IPL | External MII port enable<br>1: MII interface configuration is enabled.<br>0: External MII interface is disabled and IP175B works as a 5-port switch (default).<br><br>The configuration function of pin Px_FORCE, FILTER_RSV_DA, MAC_X_EN, LONG_PKT, AGING, P4_HIGH and COS_EN are disabled when this pin is pulled high. |
| 53 | RMII_EN | IPL | RMII enable for all MII ports.<br>1: All MII/RMII interfaces work in RMII mode<br>0: All MII/RMII interfaces work in MII mode (default).<br><br>It is valid only if P4EXT is pulled high.<br>This pin defines the initial setting of all MII ports. Each port can be configured as MII or RMII by programming MII register 31.5[10:8]. |
| 67 | MAC_X_EN | IPH2 | Flow control enable for external MII ports<br>1: enable (default),<br>0: disable<br><br>It is valid only if P4EXT is pulled low. |
| 96 | MII0_MAC_MOD | IPL1 | External MII0 port MAC mode<br>MII0 is connected to MAC5 of IP175B.<br>1: MII0 works as a MAC and should be connected to an external PHY.<br>0: MII0 works as a PHY and should be connected to an external MAC device (default).<br><br>It is valid only if P4EXT is pulled high. |
| 54 | MII1_PHY_MOD (SDA) | IPH/O | External MII1 source port selection<br>1: MII1 is connected to PHY4 of IP175B. It should be connected to an external MAC device.<br>0: MII1 is connected to MAC4 of IP175B. It should be connected to an external PHY.<br><br>It is valid only if P4EXT is pulled high and MII1_DIS is pulled low. |
| 111 | MII2_MAC_MOD | IPL | External MII2 port MAC mode<br>MII2 is connected to MAC4 of IP175B.<br>1: MII2 works as a MAC and should be connected to an external PHY.<br>0: MII2 works as a PHY and should be connected to an external MAC device (default).<br><br>It is valid only if P4EXT is pulled high and MII2_EN is pulled high. |
| 113 | MII2_EN | IPL/O | MII2 enable<br>1: MII2 is enabled. It is note that LED is changed to serial mode automatically. User should not enable MII2 if pin 54 MII1_PHY_MOD is pulled low.<br>0: MII2 is disabled (default).<br><br>It is valid only if P4EXT is pulled high.<br>The configuration function of pin Px_FORCE_FULL, Px_FORCE_100, BF_STM_EN, LINK_Q, X_EN, and MII0_MAC_MODE are disabled when this pin is pulled high.<br><br>It becomes an output pin MDC1 after reset. |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External MII port setting** | | | |
| 75 | P4MII_SNI | IPL | SNI enable for MII0<br>1: SNI interface<br>0: MII interface (default).<br><br>It is valid only is P4EXT is pulled high and RMII_EN is pulled low.<br>It is valid for MII0 only. |
| 51 | MII1_DIS | IPL | Disable MII1<br>1: MII1 is disabled. It is for router application with one-MAC CPU.<br>0:.MII1 is enabled. PHY4 is an independent PHY and can be access through MII1. It is for router application with two-MAC CPU (default).<br><br>It is valid only if P4EXT is pulled high. |

**Configuration summary**

| mode | p4ext | mii1_dis | mii2_en | p4mii_sni | rmii_en | mii0_mac_mod | mii2_mac_mod |
|---|---|---|---|---|---|---|---|
| **MII/RMII0** | | | | | | | |
| MII/ PHY mode | 1 | X | X | 0 | 0 | 0 | X |
| MII/ MAC mode | 1 | X | X | 0 | 0 | 1 | X |
| RMII | 1 | X | X | 0 | 1 | X | X |
| SNI/ PHY mode | 1 | X | X | 1 | 0 | 0 | X |
| SNI/ MAC mode | 1 | X | X | 1 | 0 | 1 | X |
| **MII/RMII1** | | | | | | | |
| MII/ PHY mode | 1 | 0 | X | X | 0 | X | X |
| RMII | 1 | 0 | X | X | 1 | X | X |
| **MII/RMII2** | | | | | | | |
| MII/ PHY mode | 1 | X | 1 | X | 0 | X | 0 |
| MII/ MAC mode | 1 | X | 1 | X | 0 | X | 1 |
| RMII | 1 | X | 1 | X | 1 | X | X |

**Note:** RMII_EN takes precedence of P4MII_SNI.

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External MII0 interface (PHY mode, MII0_MAC_MOD=0, P4MII_SNI=0)** | | | |
| 89 | MII0_RXCLK | O | MII receive clock<br><br>MII0_RXCLK and MII0_TXCLK are the same clock source and in phase. |
| 81 | MII0_TXCLK | O | MII transmit clock |
| 80, 79, 78, 77 | TXD0_0, TXD0_1, TXD0_2, TXD0_3 | IPL2 | MII transmit data<br><br>It is sampled at the rising edge of MII0_TXCLK. |
| 76 | TXEN0 | IPL2 | MII transmit enable<br><br>It is used to frame TXD0[3:0]. It is sampled at the rising edge of MII0_TXCLK. |
| 90 | COL0 | O | MII collision<br><br>It is active when MII0 is half duplex and a collision event happens. |
| 84 | RXDV0 | O | MII receive data valid<br><br>It is used to frame RXD0[3:0]. It is sent out at the falling edge of MII0_RXCLK. |
| 88, 87, 86, 85 | RXD0_0, RXD0_1, RXD0_2, RXD0_3 | O | MII receive data<br><br>It is sent out at the falling edge of MII0_RXCLK. |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External MII0 interface (MAC mode, MII0_MAC_MOD=1, P4MII_SNI=0)** | | | |
| 81 | MII0_TXCLK | I | MII transmit clock<br><br>It is an input clock and it is connected to MII_TXCLK of external PHY. |
| 80, 79, 78, 77 | TXD0_0, TXD0_1, TXD0_2, TXD0_3 | O | MII transmit data<br><br>It is connected to MII_TXD of external PHY. It is sent out at the rising edge of MII0_TXCLK. |
| 76 | TXEN0 | O | MII transmit enable<br><br>It is an output signal and is connected to MII_TXEN of external PHY. It is sent out at the rising edge of MII0_TXCLK. |
| 90 | COL0 | IPL2 | MII collision<br><br>It is an input signal and is connected to the MII_COL of external PHY. |
| 84 | RXDV0 | I | MII receive data valid<br><br>It is an input signal and is connected to the MII_RXDV of external PHY. RXDV0 is used to frame RXD0[3:0]. |
| 88, 87, 86, 85 | RXD0_0, RXD0_1, RXD0_2, RXD0_3 | I | Receive data<br><br>It is NRZ data and is connected MII_RXD[3:0] of external PHY. It is received at the rising edge of MII0_RXCLK. |
| 89 | MII0_RXCLK | I | MII receive clock |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External MII1 interface (PHY mode, MII1_PHY_MOD=1, P4EXT=1)** | | | |
| 62 | MII1_TXCLK | O | MII Transmit clock |
| 61, 60, 59, 58 | TXD1_0, TXD1_1, TXD1_2, TXD1_3 | IPL2 | MII transmit data<br><br>It is sampled at the rising edge of MII1_TXCLK. |
| 57 | TXEN1 | IPL2 | MII transmit enable<br><br>It is used to frame TXD1[3:0]. It is sampled at the rising edge of MII1_TXCLK. |
| 69 | COL1 | O | MII collision<br><br>It is active when MII1 is half duplex and a collision event happens. |
| 63 | RXDV1 | O | MII receive data valid<br><br>It is used to frame RXD1[3:0]. It is sent out at the falling edge of MII1_RXCLK. |
| 67, 66, 65, 64 | RXD1_0, RXD1_1, RXD1_2, RXD1_3 | O | MII receive data<br><br>It is sent out at the falling edge of MII1_RXCLK. |
| 68 | MII1_RXCLK | O | MII receive clock |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External MII2 interface (PHY mode, MII2_MAC_MOD=0, MII2_EN=1)** | | | |
| 109 | MII2_RXCLK | O | MII receive clock |
| 103 | MII2_TXCLK | O | MII transmit clock |
| 102, 101,<br>100, 97 | TXD2_0, TXD2_1,<br>TXD2_2, TXD2_3 | IPL2<br>IPH1<br>IPH1<br>IPL2 | MII transmit data<br><br>It is sampled at the rising edge of MII2_TXCLK. |
| 96 | TXEN2 | IPL2 | MII transmit enable<br><br>It is used to frame TXD0[3:0]. It is sampled at the rising edge of MII2_TXCLK. |
| 110 | COL2 | O | MII collision<br><br>It is active when MII2 is half duplex and a collision event happens. |
| 104 | RXDV2 | O | MII receive data valid<br><br>It is used to frame RXD0[3:0]. It is sent out at the falling edge of MII2_RXCLK. |
| 108, 107,<br>106, 105 | RXD2_0, RXD2_1,<br>RXD2_2, RXD2_3 | O | MII receive data<br><br>It is sent out at the falling edge of MII2_RXCLK. |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External MII2 interface (MAC mode, MII2_MAC_MOD=1, MII2_EN=1)** | | | |
| 103 | MII2_TXCLK | I | MII transmit clock<br><br>It is an input clock and it is connected to MII_TXCLK of external PHY. |
| 102, 101, 100, 97 | TXD2_0, TXD2_1, TXD2_2, TXD2_3 | O | MII transmit data<br><br>It is connected to MII_TXD of external PHY. It is sent out at the rising edge of MII2_TXCLK. |
| 96 | TXEN2 | O | MII transmit enable<br><br>It is an output signal and is connected to MII_TXEN of external PHY. It is sent out at the rising edge of MII2_TXCLK. |
| 110 | COL2 | IPL2 | MII collision<br><br>It is an input signal and is connected to the MII_COL of external PHY. |
| 104 | RXDV2 | I | MII receive data valid<br><br>It is an input signal and is connected to the MII_RXDV of external PHY. RXDV2 is used to frame RXD2[3:0]. |
| 108, 107, 106, 105 | RXD2_0, RXD2_1, RXD2_2, RXD2_3 | I | Receive data<br><br>It is NRZ data and is connected MII_RXD[3:0] of external PHY. It is received at the rising edge of MII2_RXCLK. |
| 109 | MII2_RXCLK | I | MII receive clock |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External RMII0 interface (RMII_EN=1, P4EXT=1)** | | | |
| 88, 87 | RXD0_0, RXD0_1 | I | RMII receive data<br><br>It is connected RMII_RXD[1:0] of external PHY or RMII_TXD[1:0] of external MAC. |
| 84 | RXDV0 | I | RMII receive data valid<br><br>It is connected RMII_RXDV of external PHY or RMII_TXEN of external MAC. |
| 80, 79 | TXD0_0, TXD0_1 | O | RMII transmit data<br><br>It is connected RMII_RXD[1:0] of external MAC or RMII_TXD[1:0] of external PHY. |
| 76 | TXEN0 | O | RMII transmit enable<br><br>It is connected RMII_RXDV of external MAC or RMII_TXEN of external PHY. |
| 77 | RMII0_CLK_OUT | O | A 50Mhz reference clock output for other RMII devices |
| 89 | RMII0_CLK_IN | I | 50Mhz RMII reference clock input |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External RMII1 interface (RMII_EN=1, MII1_DIS=0, MII1_PHY_MOD=1, P4EXT=1)** | | | |
| 67, 66 | RXD1_0, RXD1_1 | O | RMII receive data<br><br>It is connected to RMII_TXD[1:0] of external PHY or RMII_RXD[1:0] of external MAC. |
| 63 | RXDV1 | O | RMII receive data valid<br><br>It is connected to RMII_TXEN of external PHY or RMII_RXDV of external MAC. |
| 61, 60 | TXD1_0, TXD1_1 | I | RMII transmit data<br><br>It is connected to RMII_RXD[1:0] of external PHY or RMII_TXD[1:0] of external MAC. |
| 57 | TXEN1 | I | RMII transmit enable<br><br>It is connected to RMII_RXDV of external PHY or RMII_TXEN of external MAC. |
| 65 | RMII1_PHY_CLK_OUT | O | A 50Mhz reference clock output for other RMII devices |
| 59 | RMII1_PHY_CLK_IN | I | 50Mhz RMII reference clock input |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External RMII1 interface (RMII_EN=1, MII1_DIS=0, MII1_PHY_MOD=0, P4EXT=1)** | | | |
| 67, 66 | RXD1_0, RXD1_1 | I | RMII receive data<br><br>It is connected to RMII_RXD[1:0] of external PHY or RMII_TXD[1:0] of external MAC. |
| 63 | RXDV1 | I | RMII receive data valid<br><br>It is connected to RMII_RXDV of external PHY or RMII_TXEN of external MAC. |
| 61, 60 | TXD1_0, TXD1_1 | O | RMII transmit data<br><br>It is connected to RMII_RXD[1:0] of external MAC or RMII_TXD[1:0] of external PHY. |
| 57 | TXEN1 | O | RMII transmit enable<br><br>It is connected to RMII_RXDV of external MAC or RMII_TXEN of external PHY. |
| 58 | RMII1_MAC_CLK_OUT | O | A 50Mhz reference clock output for other RMII devices |
| 68 | RMII1_MAC_CLK_IN | I | 50Mhz RMII reference clock input |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **External RMII2 interface (RMII_EN=1, MII2_EN=1, P4EXT=1)** | | | |
| 108, 107 | RXD2_0, RXD2_1 | I | RMII receive data<br><br>It is connected RMII_RXD[1:0] of external PHY or RMII_TXD[1:0] of external MAC. |
| 104 | RXDV2 | I | RMII receive data valid<br><br>It is connected RMII_RXDV of external PHY or RMII_TXEN of external MAC. |
| 102,101 | TXD2_0, TXD2_1 | O | RMII transmit data<br><br>It is connected RMII_RXD[1:0] of external MAC or RMII_TXD[1:0] of external PHY. |
| 96 | TXEN2 | O | RMII transmit enable<br><br>It is connected RMII_RXDV of external MAC or RMII_TXEN of external PHY. |
| 97 | RMII2_CLK_OUT | O | A 50Mhz reference clock output for other RMII devices |
| 109 | RMII2_CLK_IN | I | 50Mhz RMII reference clock input |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **Force mode (the setting is latched at the end of reset)** | | | |
| 85, 76 | P4_FORCE | IPL2 | Port4 works at force mode.<br>1: force mode, disable port4 NWAY capability<br>0: auto-negotiation with all capability enabled (default)<br><br>It's set by pin 85 if MII0 is in PHY mode and it's set by pin 76 if MII0 is in MAC mode.<br><br>It is valid only if p4ext is pulled low. |
| 86, 77 | P3_FORCE | IPL2 | Port3 works at force mode.<br>1: force mode, disable port3 NWAY capability<br>0: auto-negotiation with all capability enabled (default)<br><br>It's set by pin 86 if MII0 is in PHY mode and it's set by pin 77 if MII0 is in MAC mode.<br><br>It is valid only if p4ext is pulled low. |
| 87, 78 | P2_FORCE | IPL2 | Port2 works at force mode.<br>1: force mode, disable port2 NWAY capability<br>0: auto-negotiation with all capability enabled (default)<br><br>It's set by pin 87 if MII0 is in PHY mode and it's set by pin 78 if MII0 is in MAC mode.<br><br>It is valid only if p4ext is pulled low. |
| 88, 79 | P1_FORCE | IPL2 | Port1 works at force mode.<br>1: force mode, disable port1 NWAY capability<br>0: auto-negotiation with all capability enabled (default)<br><br>It's set by pin 88 if MII0 is in PHY mode and it's set by pin 79 if MII0 is in MAC mode.<br><br>It is valid only if p4ext is pulled low. |
| 90, 80 | P0_FORCE | IPL2 | Port0 works at force mode.<br>1: force mode, disable port0 NWAY capability<br>0: auto-negotiation with all capability enabled (default)<br><br>It's set by pin 90 if MII0 is in PHY mode and it's set by pin 80 if MII0 is in MAC mode.<br><br>It is valid only if p4ext is pulled low. |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **Force mode (the setting is latched at the end of reset)** | | | |
| 103 | P4_FORCE100 | IPL1 | Force port4 work at 100M or 10M.<br>1: force 100M<br>0: force 10M (default)<br><br>It is used to force speed of the sixth switch port (MAC5) if P4EXT is pulled high.<br>The configuration function is disabled when MII2_EN is pulled high. |
| 104 | P3_FORCE100 | IPL1 | Force port3 work at 100M or 10M.<br>1: force 100M<br>0: force 10M (default)<br><br>It is used to force speed of the fifth switch port (MAC4) if P4EXT is pulled high.<br>The configuration function is disabled when MII2_EN is pulled high. |
| 105 | P2_FORCE100 | IPL1 | Force port2 work at 100M or 10M.<br>1: force 100M<br>0: force 10M (default)<br>The configuration function is disabled when MII2_EN is pulled high. |
| 106 | P1_FORCE100 | IPL1 | Force port1 work at 100M or 10M.<br>1: force 100M<br>0: force 10M (default)<br>The configuration function is disabled when MII2_EN is pulled high. |
| 107 | P0_FORCE100 | IPL1 | Force port0 work at 100M or 10M.<br>1: force 100M<br>0: force 10M (default)<br>The configuration function is disabled when MII2_EN is pulled high. |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **Force mode (the setting is latched at the end of reset)** | | | |
| 108 | P4_FORCE_FULL | IPL1 | Force port4 work at full duplex or half duplex<br>1: force full duplex<br>0: force half duplex (default)<br><br>It is used to force duplex of the sixth switch port (MAC5) if P4EXT is pulled high.<br>The configuration function is disabled when MII2_EN is pulled high. |
| 109 | P3_FORCE_FULL | IPL1 | Force port3 work at full duplex or half duplex<br>1: force full duplex<br>0: force half duplex (default)<br><br>It is used to force duplex of the fifth switch port (MAC4) if P4EXT is pulled high.<br>The configuration function is disabled when MII2_EN is pulled high. |
| 110 | P2_FORCE_FULL | IPL1 | Force port2 work at full duplex or half duplex<br>1: force full duplex<br>0: force half duplex (default)<br>The configuration function is disabled when MII2_EN is pulled high. |
| 111 | P1_FORCE_FULL | IPL1 | Force port1 work at full duplex or half duplex<br>1: force full duplex<br>0: force half duplex (default)<br><br>The configuration function is disabled when MII2_EN is pulled high. |
| 112 | P0_FORCE_FULL | IPL1 | Force port0 work at full duplex or half duplex<br>1: force full duplex<br>0: force half duplex (default)<br><br>The configuration function is disabled when MII2_EN is pulled high. |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **Transceiver** | | | |
| 127, 128, 11, 12, 18, 19, 29, 30, 33, 34 | RXIP0, RXIM0, RXIP1, RXIM1, RXIP2, RXIM2, RXIP3, RXIM3, RXIP4, RXIM4 | I | TP receive |
| 3, 4, 8, 9, 21, 22, 26, 27, 37, 38 | TXOP0, TXOM0, TXOP1, TXOM1, TXOP2, TXOM2, TXOP3, TXOM3, TXOP4, TXOM4 | O | TP transmit |
| 15 | BGRES | O | Band gap resister.<br><br>It is connected to GND through a 6.19 k ohm resistor. Please refer to application circuit for more information. |
| 125, 41, 42, 43, 44 | NC | I | |

## Pin description (continued)

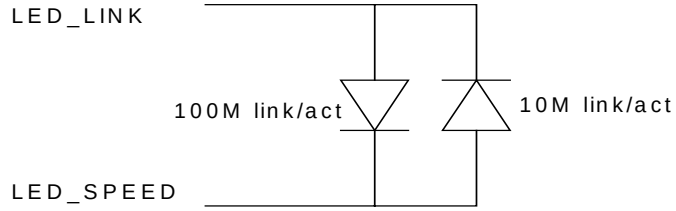
| Pin No. | Label | Type | Description |
|---|---|---|---|
| **Misc.** | | | |
| 123 | X1 | I | System clock input or crystal input<br><br>It is recommended to connect X1 and X2 to a crystal. If the clock source is from another chip, the clock should be active at least for 1ms before pin 93 RESETB de-asserted. |
| 122 | X2 | O | Crystal output |
| 93 | RESETB | I | Reset, low active |
| 52 | TEST2 | IPL | Test mode enable<br><br>It should be connected to GND for normal operation. |
| **EEPROM** | | | |
| 53 | SCL | IPL/O | After reset, it is used as clock pin SCL of EEPROM. Its period is longer than 10us. IP175B stops reading EEPROM if it finds there is no 55AA pattern in address 0. After reading EEPROM, this pin becomes an input pin. |
| 54 | SDA | IPH/O | After reset, it is used as data pin SDA of EEPROM. After reading EEPROM, this pin becomes an input pin. It is pulled up in 24C01A application circuit. |
| **SMI** | | | |
| 71, 70 | MDC0, MDIO0 | IPL | SMI0<br><br>The external MAC device uses the interface to access IP175B's MII registers. |
| 113, 74 | MDC1, MDIO1 | IPL/O | SMI1<br><br>IP175B uses the interface to polling the MII registers of external PHY to get its status. It is active only if p4ext is pulled high.<br><br>If the external PHY doesn't support SMI, the polling result will be 16'hFFFF, and IP175B suppose the link status is good. |

## Pin description (continued)

| Pin No. | Label | Type | Description |
|---|---|---|---|
| **LED** | | | |
| 92, 91 | LED_SEL[1:0] | IPH | LED output mode selection.<br><br>LED_SEL[1:0]=00: LED mode 0,<br>LED_SEL[1:0]=01: LED mode 1, dual color mode<br>LED_SEL[1:0]=10: LED mode 2,<br>LED_SEL[1:0]=11: LED mode 3 (default) |
| 110, 107, 104, 101, 96 | LED_LINK[4:0] | O | Link, Activity (output after reset)<br><br>LED mode0: 100M Link + Activity (same as mode 2)<br>LED mode1:<br>LED mode2, 100M Link + Activity<br>(1: 100M Link fail, 0: 100M Link ok and no activity, flash: 100M Link ok and TX/RX activity)<br>LED mode3: Link + Activity<br>(1: link fail, 0: link ok, flash: Link ok and TX/ RX activity) |
| 111, 108, 105, 102, 97 | LED_SPEED[4:0] | O | Speed (output after reset)<br><br>LED mode0: (1: no collision, flash: collision) (note*)<br>LED mode1:<br>LED mode2: Full/half: (1: half, 0: full, flash: collision)<br>LED mode3: (1: speed=10M, 0: speed=100M) |
| 112, 109, 106, 103, 100 | LED_FULL[4:0] | O | Full/half, Link (output after reset)<br><br>LED mode0, 10M Link + Activity (same as mode 2)<br>LED mode1, same as mode 3<br>LED mode2, 10M Link + Activity<br>(1: 10M Link fail, 0: 10M Link ok and no activity, flash: 10M Link ok and TX/RX activity)<br>LED mode3: Full/half: (1: half, 0: full, flash: collision) |

**Note:** LED_SPEED[0] shows collision information for all ports. LED_SPEED[4:1] is undefined.

## Pin description (continued)

<table>
<tr><th>Pin No.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Dual color mode LED (It is active when LED_SEL[1:0] is {0,1}.)</td></tr>
<tr><td>110, 107, 104, 101, 96</td><td>LED_LINK[4:0]</td><td>O</td><td rowspan="6">Application circuit<br> 

<table>
<tr><th></th><th>Type</th><th>LED_LINK</th><th>LED_SPEED</th></tr>
<tr><td>Link off</td><td>O</td><td>1</td><td>1</td></tr>
<tr><td>100M link</td><td>O</td><td>1</td><td>0</td></tr>
<tr><td>100M link/ Activity</td><td>O</td><td>Flash</td><td>0</td></tr>
<tr><td>10M link</td><td>O</td><td>0</td><td>1</td></tr>
<tr><td>10M link/ Activity</td><td>O</td><td>0</td><td>Flash</td></tr>
</table></td></tr>
<tr><td>111, 108, 105, 102, 97</td><td>LED_SPEED[4:0]</td><td>O</td></tr>
<tr><td>112, 109, 106, 103, 100</td><td>LED_FULL[4:0]</td><td>O</td><td>Full/half, Link (output after reset)<br>Full/half: (1: half, 0: full, flash: collision)</td></tr>
<tr><td colspan="4">Serial LED (MII2_EN=1)</td></tr>
<tr><td>112</td><td>SDATA</td><td>O</td><td>LED serial data</td></tr>
<tr><td>111</td><td>SCLK</td><td>O</td><td>LED serial clock<br><br>Normal mode: 312.5KHz, Speed_up mode: 10MHz</td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="4">Power</td></tr>
<tr><td>72, 98</td><td>VCC_O_1, VCC_O_2</td><td></td><td>3.3V power</td></tr>
<tr><td>1, 6, 10, 14, 20, 24, 28, 35, 40</td><td>AVCC</td><td></td><td>1.8v power</td></tr>
<tr><td>46, 47, 50, 55, 82, 94, 114, 115, 124</td><td>VCC</td><td></td><td>1.8v power</td></tr>
</table>

# 2 Functional Description

## 2.1 Flow control

IP175B supports the standard 802.3X flow control frames on both transmit and receive sides. On the receive side, if IP175B receives a pause control frame, the IP175B will defer transmiting next normal frame; on the transmit side, IP175B issues pause control frame to remote station when the output of the destination port is overflowed.

When CoS is enabled, IP175B may disable the flow control function for a short term to guarantee the bandwidth of high priority packets. A port disables its flow control function for 2 ~ 3 seconds when it receives a high priority packet. It doesn't transmit pause frame or jam pattern during the period but it still responses to pause frame or jam pattern.

## 2.2 Broadcast storm protection

A port of IP175B begins to drops broadcast packets if the received broadcast packets are more than the threshold defined in MII register 30.11[15:14] or EEPROM register 59[7:6] bq_stm_thr_sel [1:0] in 10ms (100Mbps) or 100ms (10Mbps)

The function can be enabled by pulling high pin 102 BF_STM_EN or programming MII register 29.18.11.

## 2.3 Port locking (Port security)

IP175B supports port locking. Each port can be configured individually by programming MII register 30.10[5:0] or EEPROM 57[5:0]. User has to reset IP175B to disable the function by writing 16'h175C to MII register 30.0 after enabling this function. IP175B locks first MAC address if the function is enabled. Any packet with MAC address not equal to the locked one will be dropped. The aging function is recommended to be disabled, if port locking is enabled.

## 2.4 Port base VLAN

IP175B supports port base VLAN functions. It separates IP175B into some groups (VLAN). A port is limited to communicate with other ports within the same group when the function is enabled. Frames will be limited in a VLAN group and will not be forwarded out of this VLAN group. A port can be assigned to one or more VLAN groups. The members (ports) of a VLAN group are assigned by programming EEPROM register 19~21 or MII register 14~18.

## 2.5 Tag VLAN / Tag and un-tag function

### 2.5.1 Tag and un-tag function

IP175B inserts or removes a tag of a frame if tagging/ un-tagging function is enabled. It is enabled by programming MII register 29.23. The operation is illustrated as follows. The tag information is defined in MII register 29.24~29.30 and EEPROM register 24~38.

| Frame type of the received packet | The operation of a port which forwards the packet | |
|---|---|---|
| | Forward to a untagged filed | Forward to a tagged field |
| Untagged | Forward the packet without modification | 1. Insert a tag using the default VLAN tag value of the source port<br>2. Calculate new CRC<br>3. The default VLAN tag value is defined in the MII register 29.24~29.30. |
| Priority-tagged (VLAN ID=0) | 1. Strip tag<br>2. Calculate new CRC | 1. Keep priority field.<br>2. Replace the tag with the default VLAN tag value of the source port<br>3. Calculate new CRC<br>4. The default VLAN tag value is defined in the MII register 29.24~29.30. |
| VLAN-tagged | 1. Strip tag<br>2. Calculate new CRC | Forward the packet without modification |



### 2.5.2 Tag VLAN



If tag VLAN function is enabled (MII register 30.9.7 TAG_VLAN_EN is logic high), IP175B forwards a packet according to MAC address and VLAN output port masks, defined in MII register 30.1~30.8. A tagged packet is forwarded to the ports belonging to the same VLAN of the packet. One of the sixteen VLAN output port masks is selected by VID index, which is four bits selected from VID field in a tag. VID index is defined in MII register 30.9[6:4] VID_IDX_SEL. For example, VLAN output port mask 1 is selected if VID index selected by VID_IDX_SEL is equal to 1.

IP175B handles an un-tagged packet using the default VLAN tag value of its source port. A packet with VID equal to 12'b0 will be handled as un-tag frame.

### 2.5.3 Tag/ un-tag function and Tag VLAN function in a router application

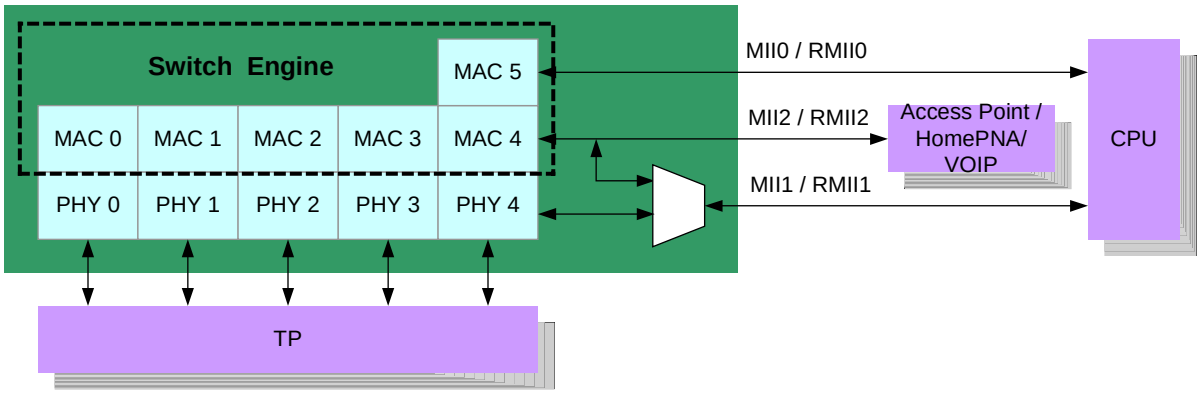
Tag/ un-tag and Tag VALN are necessary in a router application with one-MAC CPU, MII0 is connected to CPU and MII1 is disabled (DIS_MII1=1). PHY0~4 are connected to switching engine MAC 0~4 and MII0 is connected to switching engine MAC5.

In this application, MII0 is defined as a tagged port and the other ports (port 0~4) are defined as un-tagged ports. IP175B inserts VLAN tag into packets withsource port information when it forwards the packets to MII0. The VLAN tags are defined in MII register 29.24~29.30. CPU can identify the source port of a packet by examining the VLAN tag.

CPU inserts VLAN tag into packets with destination port information following the content in MII register 29.24~29.30 when it sends packets to MII0. IP175B forwards a packet from MII0 to the appropriate port according to the MAC address and VLAN tag. IP175B removes the VLAN tag when it forwards the packet.

## 2.6 MII/RMII

IP175B supports three MII/RMII ports. The block diagram and detail configuration are shown below. It is noted that MII2 and MII1 MAC mode can't be enabled at the same time. That is, user should not use MII2 if pin 54 MII1_PHY_MOD is pulled low.




| I/F | mode | Int | ext | p4ext | mii1 _dis | mii2 _en | p4mii _sni | rmii_ en | mii0_mac _mod | mii1_phy _mode | mii2_mac _mod |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **MII0** | | | | | | | | | | | |
| MII | PHY mode | MAC5 | MAC | 1 | X | X | 0 | 0 | 0 | X | X |
| MII | MAC mode | MAC5 | PHY | 1 | X | X | 0 | 0 | 1 | X | X |
| RMII | MAC | MAC5 | Note1 | 1 | X | X | 0 | 1 | X | X | X |
| SNI | PHY mode | MAC5 | MAC | 1 | X | X | 1 | 0 | 0 | X | X |
| SNI | MAC mode | MAC5 | PHY | 1 | X | X | 1 | 0 | 1 | X | X |
| **MII1** | | | | | | | | | | | |
| MII | PHY mode | PHY4 | MAC | 1 | 0 | X | X | 0 | X | 1 | X |
| MII | MAC mode | MAC4 | PHY | 1 | 0 | 0 | X | 0 | X | 0 | X |
| RMII | PHY mode | PHY4 | MAC | 1 | 0 | X | X | 1 | X | 1 | X |
| RMII | MAC mode | MAC4 | PHY | 1 | 0 | 0 | X | 1 | X | 0 | X |
| **MII2** | | | | | | | | | | | |
| MII | PHY mode | MAC4 | MAC | 1 | X | 1 | X | 0 | X | X | 0 |
| MII | MAC mode | MAC4 | PHY | 1 | X | 1 | X | 0 | X | X | 1 |
| RMII | MAC | MAC4 | Note1 | 1 | X | 1 | X | 1 | X | X | X |

**Note1:** The port can be connected to an external PHY or MAC device.
**Note2:** All ports are configured as MII/RMII by pin 113 RMII_EN. Each port can be configured as MII/RMII by programming MII register 31.5[10:8].
**Note3:** RMII_EN takes precedence of P4MII_SNI.
**Abbreviation:**
I/F: the type of interface
Mode: the port works as a MAC or a PHY
Int: the internal block to which the MII port is connected
Ext: the external device to which the MII port is connected
MAC4: the port 4 of switch engine
MAC5: the port 5 of switch engine
PHY4: the port 4 of PHY

**To define the speed, duplex and pause of MII port**

The speed and duplex of MII port can be configured through pins or registers. IP175B's MII register is not fully compatible to IP175A's. User has to fill MII register 29.31 with 16'h175C before accessing MII registers. The details are shown in the following tables.

MII0 PHY mode (interface to an external MAC, MII registers can be accessed via MDC0, MDIO0)

| | Pin | EEPROM | | MII register | | |
|---|---|---|---|---|---|---|
| | | Name | Reg | Name | Phy | Reg |
| MII0 speed | P4_FORCE_100 | P4_FORCE_100 | 22.4 | P4_FORCE_100 | 29 | 22.10 |
| MII0 duplex | P4_FORCE_FULL | P4_FORCE_FULL | 21.4 | P4_FORCE_FULL | 29 | 22.5 |
| MII0 pause | -- | MAC_X_EN | 4.3 | MAC_X_EN | 29 | 18.10 |

MII0 MAC mode (interface to an external PHY), there are two ways to set MII0 speed, duplex and pause.
1. Decided by reading the MII registers 0~5 of external PHY through MDC1, MDIO1.

| | |
|---|---|
| MII0<br>Speed<br>Duplex<br>Pause | 1. IP175B polls the external PHY with address defined in MII register 31.3[4:0]. The default address value is 00001.<br>2. After reset, IP175B writes the speed/duplex/pause capability to the external PHY using the content of MII register 31.3[12:8].<br>3. IP175B reads MII register 0~5 of external PHY as MII0 speed, duplex and pause continuously. |

2. Force mode (MDC1 and MDIO1 are not connected to external PHY)

| | Pin | EEPROM | | MII register | | |
|---|---|---|---|---|---|---|
| | | Name | Reg | Name | Phy | Reg |
| MII0 speed | P4_FORCE_100 | P4_FORCE_100 | 20.4 | P4_FORCE_100 | 29 | 22.10 |
| MII0 duplex | P4_FORCE_FULL | P4_FORCE_FULL | 21.4 | P4_FORCE_FULL | 29 | 22.5 |
| MII0 pause | -- | MAC_X_EN | 4.3 | MAC_X_EN | 29 | 18.10 |

MII1 PHY mode (interface to an external MAC, MII registers can be accessed via MDC0, MDIO0)
The PHY address of MII1 PHY mode is 4.

| | Pin | EEPROM | | MII register | | |
|---|---|---|---|---|---|---|
| | | Name | Reg | Name | Phy | Reg |
| MII1 speed/duplex/ pause | -- | -- | | | 4 | 0~5 |

MII1 MAC mode (interface to an external PHY), there are two ways to set MII1's speed, duplex and pause.

1. IP175B reads the MII registers 0~5 of external PHY through MDC1, MDIO1.

| | |
|---|---|
| MII1<br>Speed<br>Duplex<br>Pause | 1. IP175B polls the external PHY with address defined in MII register 31.4[4:0]. The default address value is 00001.<br>2. After reset, IP175B writes the speed/duplex/pause capability to the external PHY using the content of MII register 31.4[12:8].<br>3. IP175B reads MII register 0~5 of external PHY as MII1 speed, duplex and pause continuously. |

2. Force mode (MDC1 and MDIO1 are not connected to external PHY)

| | Pin | EEPROM | | MII register | | |
|---|---|---|---|---|---|---|
| | | Name | Reg | Name | Phy | Reg |
| MII1 speed | P3_FORCE_100 | P3_FORCE_100 | 20.3 | P3_FORCE_100 | 29 | 22.9 |
| MII1 duplex | P3_FORCE_FULL | P3_FORCE_FULL | 21.3 | P3_FORCE_FULL | 29 | 22.4 |
| MII1 pause | -- | MAC_X_EN | 4.3 | MAC_X_EN | 29 | 18.10 |

MII2 PHY mode (interface to an external MAC, MII registers can be accessed via MDC0, MDIO0)

| | Pin | EEPROM | | MII register | | |
|---|---|---|---|---|---|---|
| | | Name | Reg | Name | Phy | Reg |
| MII2 speed | P3_FORCE_100 | P3_FORCE_100 | 20.3 | P3_FORCE_100 | 29 | 22.9 |
| MII2 duplex | P3_FORCE_FULL | P3_FORCE_FULL | 21.3 | P3_FORCE_FULL | 29 | 22.4 |
| MII2 pause | -- | MAC_X_EN | 4.3 | MAC_X_EN | 29 | 18.10 |

MII2 MAC mode (interface to an external PHY), there are two ways to set MII2 speed, duplex and pause.
1. IP175B reads the MII registers 0~5 of external PHY through MDC1, MDIO1.

| | |
|---|---|
| MII2<br>Speed<br>Duplex<br>Pause | 1. IP175B polls the external PHY with address defined in MII register 31.4[4:0]. The default address value is 00001.<br>2. After reset, IP175B writes the speed/duplex/pause capability to the external PHY using the content of MII register 31.4[12:8].<br>3. IP175B reads MII register 0~5 of external PHY as MII2 speed, duplex and pause continuously. |

2. Force mode (MDC1 and MDIO1 are not connected to external PHY)

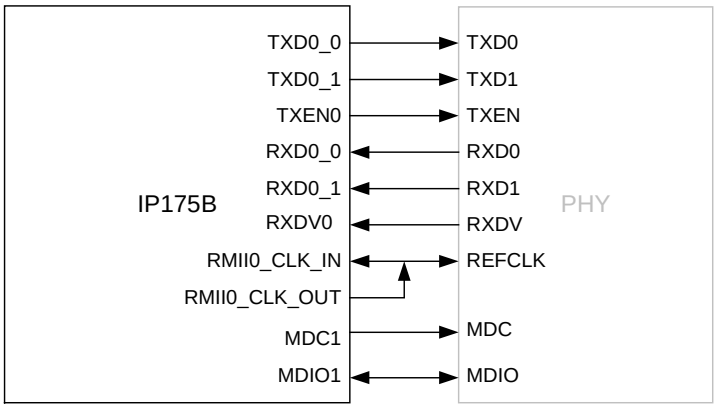
| | Pin | EEPROM | | MII register | | |
|---|---|---|---|---|---|---|
| | | Name | Reg | Name | Phy | Reg |
| MII2 speed | P3_FORCE_100 | P3_FORCE_100 | 20.3 | P3_FORCE_100 | 29 | 22.9 |
| MII2 duplex | P3_FORCE_FULL | P3_FORCE_FULL | 21.3 | P3_FORCE_FULL | 29 | 22.4 |
| MII2 pause | -- | MAC_X_EN | 4.3 | MAC_X_EN | 29 | 18.10 |

**The application circuit of RMII**

(P4EXT=1, P4MII_SNI=0, RMII_EN=1)

When RMII mode is enabled, IP175B supports reference clock RMII_CLK_OUT for each RMII port. The clock is used by the external PHY (or MAC) and 175B itself.

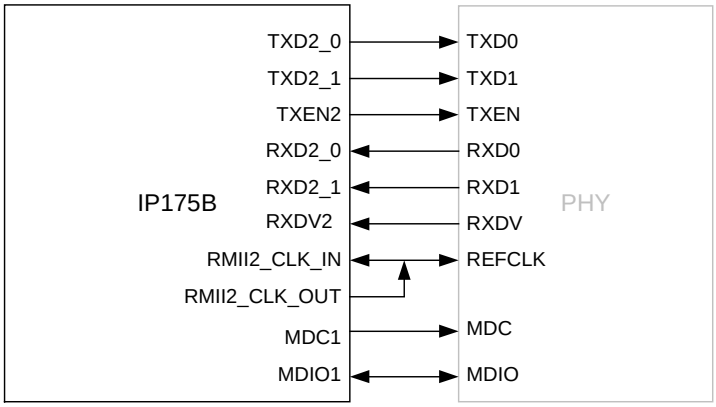
The following circuit diagram is the RMII circuit of MII0.



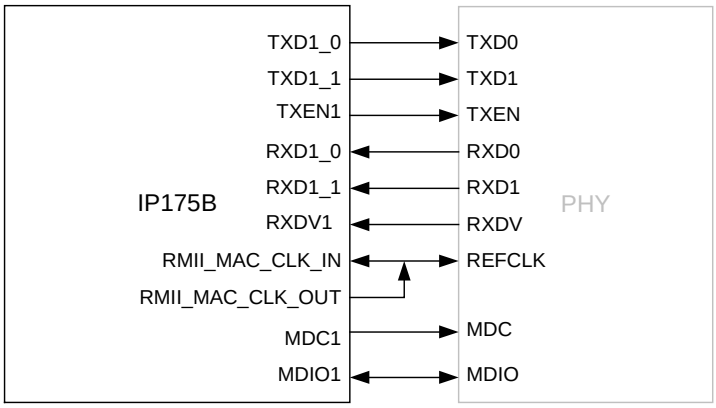



The following circuit diagram is the RMII circuit of MII2.

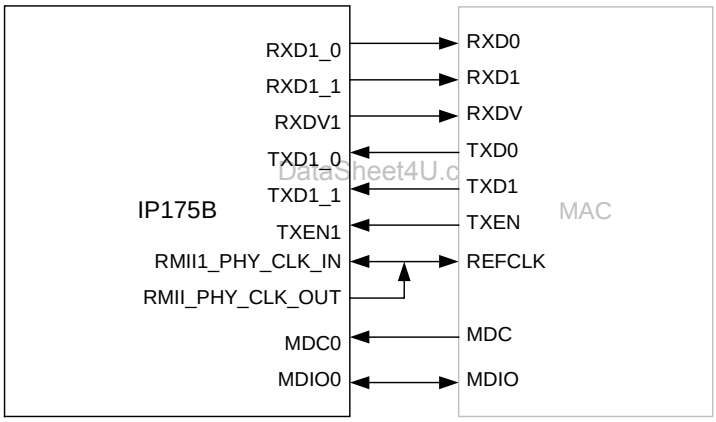




The following circuit diagram is the RMII circuit of MII1 MAC mode.




The following circuit is the RMII circuit of MII1 PHY mode.

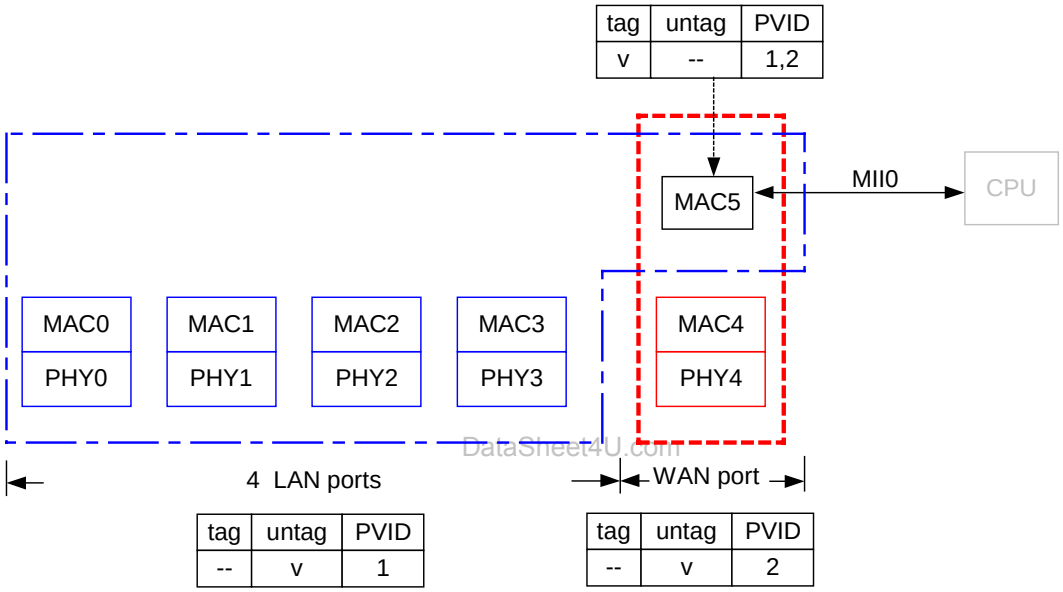


## 2.7 SMART MAC

IP175B supports SMART MAC function to solve locked Card's ID issue. The SMART MAC function can be configured to 4LAN+1WAN, 3LAN+2WAN, 2LAN+3WAN or 1LAN+4WAN. The following example illustrates the behavior of IP175B SMART MAC function for 4LAN + 1WAN.

### 2.7.1 System configuration

The system configuration and its register programming are shown in the following diagram and table.

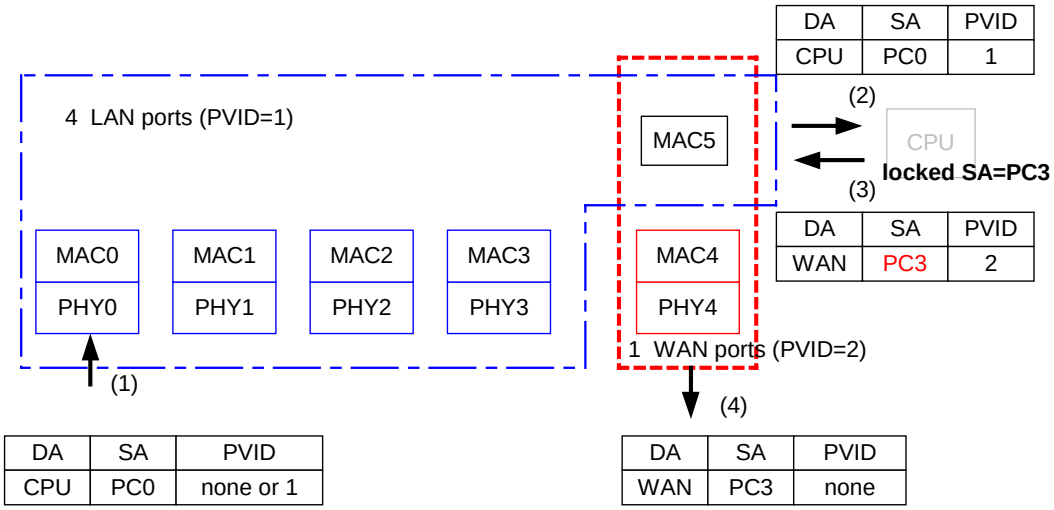


**A programming example of SMART MAC example**

| Register | Content | Description |
|---|---|---|
| **Tag/ un-tag function setup** | | |
| 29.23[0] | 0 | MII0 doesn't strip the tag of an outgoing packet. |
| 29.23[1] | 1 | MII0 adds a tag to an outgoing packet. |
| 29.23[10:6] | 11111 | Port0~4 strip the tag of an outgoing packet. |
| 29.23[15:11] | 00000 | Port0~4 doesn't add a tag to an outgoing packet. |
| **PVID function setup** | | |
| 29.24~27 | 16'h0001 | Define PVID of port0~port3 |
| 29.28 | 16'h0002 | Define PVID of port4 |
| 29.30 | 16'h0002 | Define PVID of MII0 |
| **VLAN Mask function setup** | | |
| 30.1[13:8] | 6'h2f | TAG_VLAN_MASK_1 |
| 30.1[5:0] | 6'h30 | TAG_VLAN_MASK_2 |
| **SMART MAC function setup** | | |
| 30.9[2:0] | 001 | Define 1 LAN group |
| 30.9[3] | 1 | Enable router function |
| 30.9[6:4] | 000 | Define VID index as 000 |
| 30.9[7] | 1 | Enable tag VLAN |
| 30.9[12:8] | 10000 | Define port 4 as a WAN port |

### 2.7.2 Packet from LAN to WAN

1. PC0 sends a packet to a LAN port with SA equal to PC0 without PVID or PVID equal to 1
2. IP175B forwards the packet to CPU (MII0) with PVID equal to 1.
3. CPU replaces the SA with locked address PC3, replaces PVID with 2 and sends it to IP175B.
4. IP175B forwards the packet to port4 (WAN port).

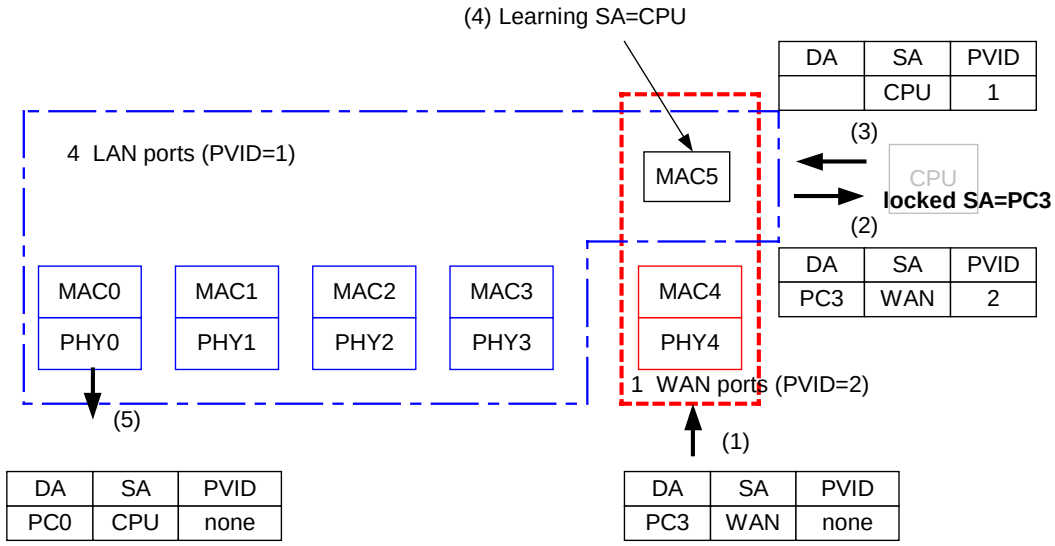





### 2.7.3 Packet from WAN to LAN



1. WAN port receives a packet with locked address PC3.
2. IP175B adds a PVID equal to 2 and forwards the packet to CPU (MII0).
3. CPU updates the DA, replaces PVID with 1 and sends it to IP175B.
4. IP175B learns the SA.
5. IP175B forwards the packet to port0 according to the DA.



## 2.8 Built in regulator

IP175B is built in one linear regulator. It use pin 120 REG_OUT to control an external transistor to generator a stable voltage source. IP175B generates a voltage source between 1.70v ~ 1.93v.

## 2.9 CoS

IP175B supports two type of CoS. One is port base priority and the other is frame base priority. IP175B supports two levels of priority queues.

### 2.9.1 Port base priority

The packets received from high priority port will be handled as high priority frames if the port base priority is enabled. It is enabled by programming the “high priority port enable” bit in MII register 29.19~29.21or EEPROM register 14~18. Each port of IP175B can be configured as a high priority port individually.

### 2.9.2 Frame base priority

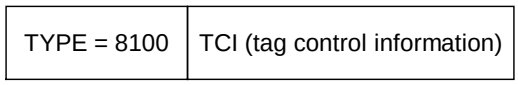
#### 2.9.2.1 VLAN tag and TCP/IP TOS

IP175B examines the specific bits in VLAN tag and TCP/IP TOS for priority frames if the frame base priority is enabled. A high priority packet will be queued into the high priority queue; this action will ensure more bandwidth is allocated for the high priority packets in the transmission. The packets will be handled as high priority frames if the tag value meets the high priority requirement, that is, priority bits in a VLAN tag bigger than 3 or TCP/IP TOS field not equal to 3’b000. It is enabled by programming the “class of service enable” bit in MII register 29.19~29.21 or EEPROM register 14~18. The frame base priority function of each port can be enabled individually.

The ratio of bandwidth of high priority and low priority queue is defined in MII register 30.12[4] or EEPROM 60[4].



VLAN field




byte 12~13 14~15

TCI definition:

Bit[15:13]: User Priority 7~0
Bit 12: Canonical Format Indicator (CFI)
Bit[11~0]: VLAN ID.
IP175C uses bit[15:13] to define priority.

TOS field


byte 12~13 14~15

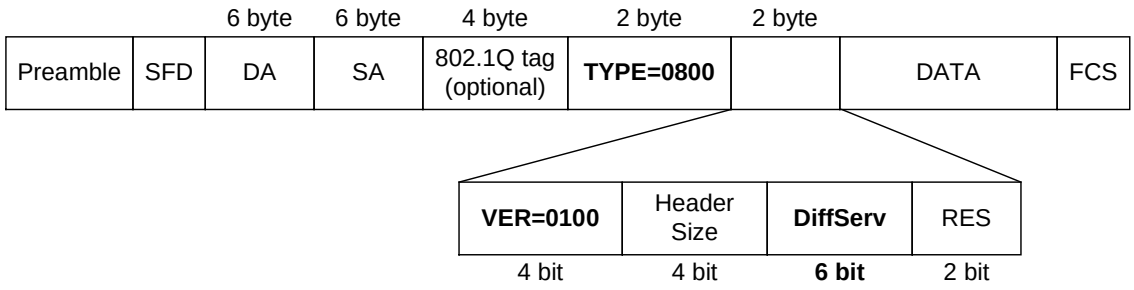
IP header definition:
Byte 14
Bit[7:0]: IP protocol version number & header length.

Byte 15: Service type
Bit[7~5]: IP Priority (Precedence ) from 7~0
Bit 4: No Delay (D)
Bit 3: High Throughput
Bit 2: High Reliability (R)
Bit[1:0]: Reserved
IP175C uses bit[4:2] to define priority.

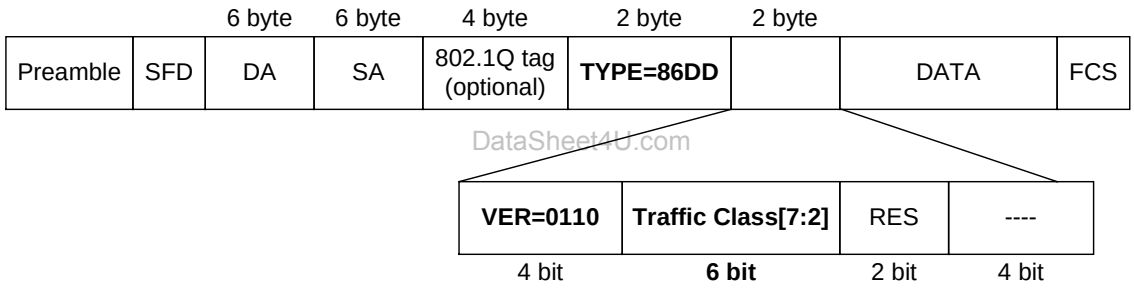
#### 2.9.2.2 IPv4/IPv6 DiffServ

IP175B checks the DiffServ field of a IPv4 frame or Traffic class field [7:2] (TC[7:2]) of a IPv6 frame and uses them to decide the frame's priority if MII register 30.27.0 DIFFSEV_EN is enabled. IP175B uses DiffServ or TC[7:2] as index to select one of 64 bits defined in the MII register 30.28~31 DSCP[63:0]. If the bit is "1", the received frame is handled as a high priority frame.

IPv4 frame format




IPv6 frame format



## 2.10 Spanning tree

IP175B supports spanning tree function with the following features:
1. Detect BPDU frames by examining multicast address (01-80-c2-00-00-00).
2. Forward BPDU packets to CPU through MII0 and add special tag for source port information.
3. Forward BPDU packets from CPU according to the special tag in a frame.
Please refer to section 2.5 “Tag VLAN / Tag and un-tag function”.

### 2.10.1 Port states

To support spanning tree protocol, each port of IP175B provides five port states shown in the following table. Port 0~4 of IP175B can be configured in one of the five spanning tree states individually by programming MII register 30.16 to enable (disable) forwarding and learning function. Port 5 (MII0) is dedicated for CPU.

| State | Fwd BPDU packet to CPU | Fwd BPDU packet from CPU | Address learning | Fwd all packet normally | (Forward enable, Learning enable) |
|---|---|---|---|---|---|
| Disable | X (note 2) | X (note 2) | X | X | (0,0) |
| Blocking | O | X (note 3) | X | X | (0,0) |
| Listening | O | O | X | X | (0,0) |
| Learning | O | O | O | X | (0,1) |
| Forwarding | O | O | O | O | (1,1) |

**Note1:** O: enabled, X: disabled
**Note2:** CPU should not send packets to IP175B and should discard packets from IP175B.
**Note3:** CPU should not send packets to IP175B.

## 2.11 Special tag

IP175B supports special tag function to exchange switching information with CPU without involving VLAN tag information. The special tag function is enabled by programming MII register 30.16.7 STAG_EN.

### 2.11.1 From CPU to switch

When special tag function is enabled, IP175B forwards packets from MII0 (CPU) by checking special tag added by CPU. The tag definition is shown in the following table. IP175B will remove the special tag 81XX and re-calculate CRC when it forwards the packet to a un-tag field. IP175B will update the special tag to 8100 and re-calculate CRC when it forwards the packet to a tag field.

| Preamble | SFD | DA | SA | 81XX(special tag) | Data | CRC |
|---|---|---|---|---|---|---|

| **Special tag 81XX** | | | |
|---|---|---|---|
| **Bit[15:12]** | **bit[11:8]** | **bit[7:5]** | **bit[4:0]** |
| 8 | 1 | 3'b0 | 00001: instruct 175B forwards the packet to port 0<br>00010: instruct 175B forwards the packet to port 1<br>00100: instruct 175B forwards the packet to port 2<br>01000: instruct 175B forwards the packet to port 3<br>10000: instruct 175B forwards the packet to port 4 |



### 2.11.2 From switch to CPU



When special tag function is enabled, IP175B sends packets to MII0 (CPU) with source port information by adding special tag to the frame. IP175B will add the special tag 81XX and re-calculate CRC when it receives the packet from a un-tag field. IP175B will update the tag 8100 to 81XX and re-calculate CRC when it receives the packet from a tag field. The tag definition is shown in the following table.

| **Special tag 81XX** | | | |
|---|---|---|---|
| **Bit[15:12]** | **bit[11:8]** | **bit[7:5]** | **bit[4:0]** |
| 8 | 1 | 3'b0 | 00001: the source port of the packet is port 0<br>00010: the source port of the packet is port 1<br>00100: the source port of the packet is port 2<br>01000: the source port of the packet is port 3<br>10000: the source port of the packet is port 4 |

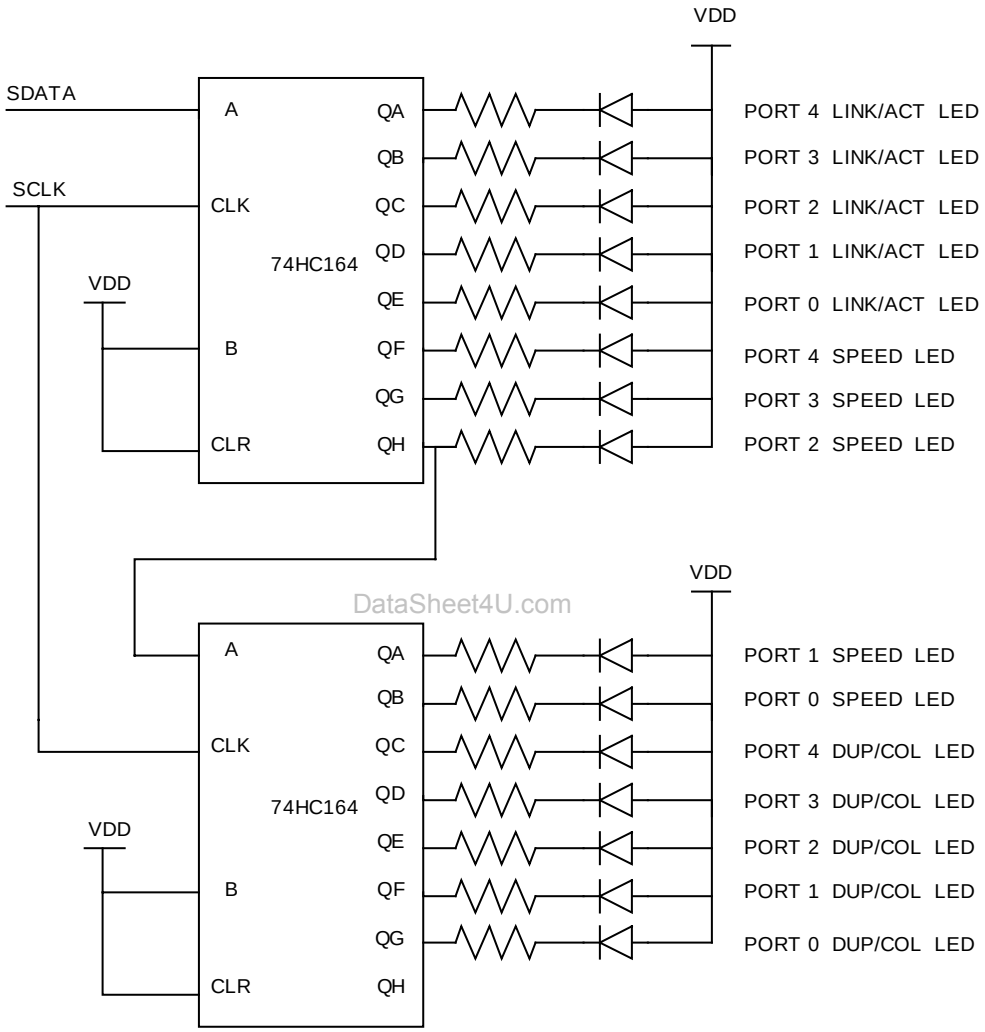
## 2.12 Static MAC address table

IP175B supports a static MAC address table, which contains two MAC address. When IP175B receives a packet whose destination address matches the pre-defined MAC address in the table, it forwards the packets to a specfic port defined in the MII register 30.26[13:8] static_port_mask_1 and 30.26[5:0] static_port_mask_0. Use can setup the MAC address table and static port mask by programming MII register 30.20~30.26.The static MAC address table has precedence over the dynamic DA look up result.

In a spanning tree application, the MII register 30.26[7] static_override_0 is “1”, MII register 30.26[6] static_valid_0 is ”1”, the MII register 30.20~22 MAC address field is 01-80-c2-00-00-00 and the MII register 30.26[5:0] static_port_mask_0 is 6’b100000 (MII0). That is, IP175B will forward BPDU to MII0 (CPU) only in spite of the port states.

## 2.13 Serial mode LED

When MII/RMII2 is enabled, there are no enough pins for LED and IP175B sends out LED information through pin 111 SCLK and pin112 SDATA. It is necessary to use TTL chip to decode and drive LED. The application Icircuit is shown below.



## 2.14 LED Blink Timing

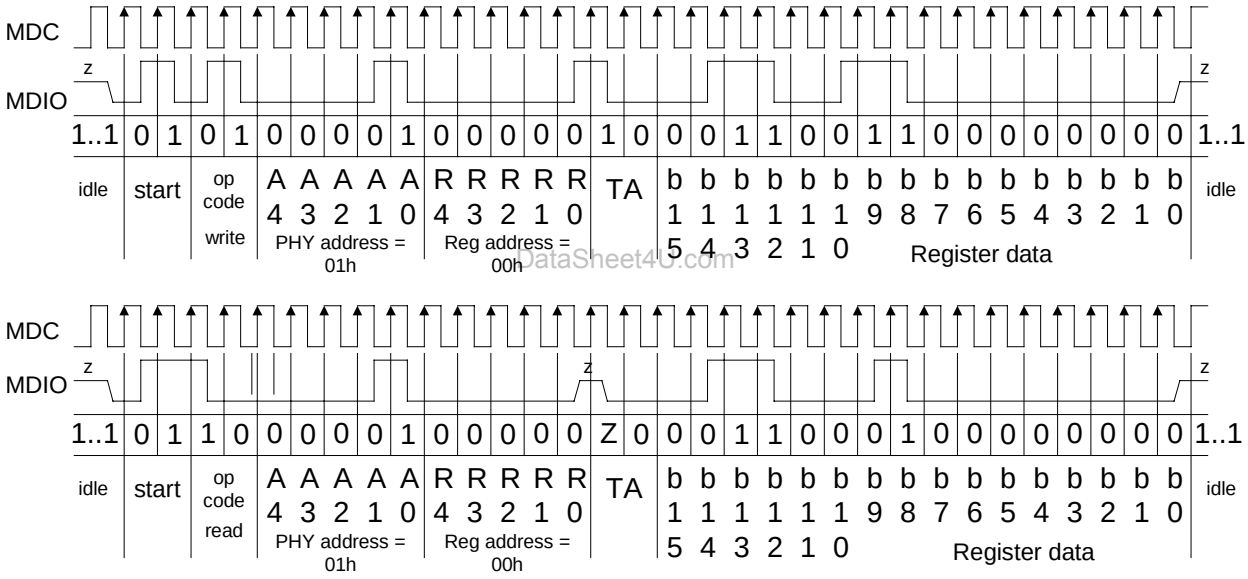
| LED mode | Blinking speed |
|---|---|
| Serial mode update period | 22 ms (44ms/2) |
| Active led blink | On -> Off 44ms -> On 176ms -> Off 44ms … |
| Collision led blink | Off -> On 176ms -> Off 44ms ->On 176ms … |
| Link quality fail blink | On 2s -> Off 2s -> On 2s -> Off 2s … |
| Neon like LED(initial setup LED) | On 286ms -> Off 2s -> On 286ms -> Off 2s … |

## 2.15 Serial management interface

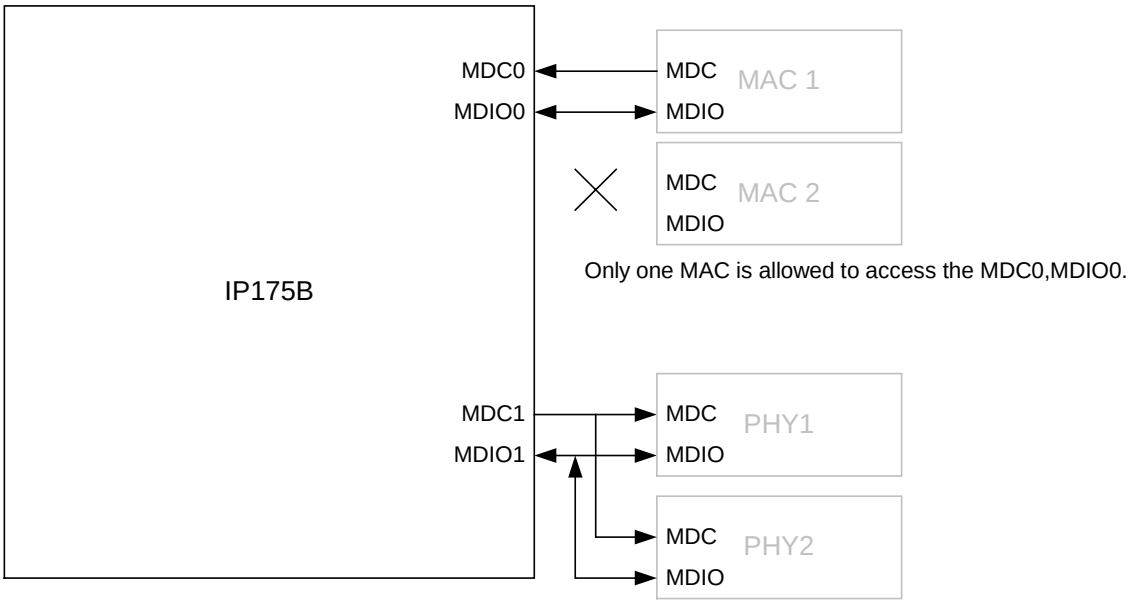
175B supports two serial management interfaces (SMI). User can access IP175B's MII registers through MDC0 and MDIO0. Its format is shown in the following table. To access MII register in IP175B, MDC should be at least one more cycle than MDIO. That is, a complete command consists of 32 bits MDIO data and at least 33 MDC clocks. When the SMI is idle, MDIO is in high impedance.

When IP175B interfaces to an external PHY, it uses MDC1 and MDIO1 to read the status of the external PHY.

| | |
|---|---|
| Frame format | <Idle><start><op code><PHY address><Registers address><turnaround><data><idle> |
| Read Operation | <Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0><$b_{15}$ $b_{14}$ $b_{13}$ $b_{12}$ $b_{11}$ $b_{10}$ $b_9$ $b_8$ $b_7$ $b_6$ $b_5$ $b_4$ $b_3$ $b_2$ $b_1b_0$><Idle> |
| Write Operation | <Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10><$b_{15}$ $b_{14}$ $b_{13}$ $b_{12}$ $b_{11}$ $b_{10}$ $b_9$ $b_8$ $b_7$ $b_6$ $b_5$ $b_4$ $b_3$ $b_2$ $b_1b_0$><Idle> |



**The application of SMI**




Only one MAC is allowed to access the MDC0,MDIO0.

All PHY can be accessed via the MDC1,MDIO1.

## 2.16 Force mode of PHY

| | | | | | |
|---|---|---|---|---|---|
| Px_FORCE | 0 | 1 | 1 | 1 | 1 |
| Px_FORCE_100 | X | 1 | 1 | 0 | 0 |
| Px_FORCE_FULL | X | 1 | 0 | 1 | 0 |
| IP175B's capability | NWAY | 100/Full | 100/Half | 10/Full | 10/Half |
| IP175B's link result | 100/Full | 100/Full | 100/Half | 10/Full | 10/Half |
| Link partner's (Nway enabled with all capability) link result | 100/Full | 100/Half | 100/Half | 10/Half | 10/Half |

Note: Px_FORCE, Px_FORCE_100,and Px_FORCE_full are force mode configuration pins. X is port number. It is from 0 to 4.

## 2.17 Reset

The IP175B supports three kinds of reset function.

**1. Hardware Reset:** Pin 93 RESETB should be asserted LOW at least for 5ms to reset IP175B. The IP175B gets initial values from pins and 24C01A EEPROM after reset.

**2. Software Reset:** After Hardware Reset, user can write 16'h175B to PHY 30 Register 0 via SMI to reset IP175B. The IP175B resets all of PHYs and Switch Engine, but IP175B does not load initial values from pins and 24C01A EEPROM.

**3. PHY Reset:** Please write "1" to bit 15 of MII register 0 to reset the PHY. The PHY address is from 0 to 4 for port 0~4 respectively.

## 2.18 MII registers of PHY

| Register | Description | Default | Note |
|---|---|---|---|
| 0 | Control Register | | X5 |
| 1 | Status Register | | X5 |
| 2 | PHY Identifier 1 Register | | X1 |
| 3 | PHY Identifier 2 Register | | X1 |
| 4 | Auto-Negotiation Advertisement Register | | X5 |
| 5 | Auto-Negotiation Link Partner Ability Register | | X5 |
| 6 | Auto-Negotiation Expansion Registers | | X5 |

X1: 5 ports share the register
X5: Each port has its individual register

## 2.19 Bandwidth control

IP175B provides the bandwidth control mechanism to manage or control the data rate on a limited bandwidth network. By controlling the ingress data rate and the egress data rate, it provides a bandwidth management solution for local area networks and also provides quick and easy allocation of uplink or downlink speeds to meet and guarantee a wide range of customer bandwidth requirements.
IP175B provides the easiest way to allocate bandwidth for each port, which defined in MII registers 31.2 ~ 31.0 or EEPROM registers 95 ~ 90. The ingress/egress data rate control range is from 128 kbps to 8 Mbps for each port.

## Register descriptions

R/W = Read/Write, SC = Self-Clearing, RO = Read Only, LL = Latching Low, LH = Latching High

**MII register 0 of PHY0~4 (Each PHY has its own MII register 0 with different PHY address)**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Control register** | | | | | |
| 4~0 | 0.15 | -- | RW/ SC | Reset<br>The PHY is reset if user write “1” to this bit. The reset period is around 2ms. User has to wait for at least 2ms to access IP175B. | 0 |
| 4~0 | 0.14 | -- | R/W | Loop back<br>1 = Loop back mode<br>0 = normal operation<br>When this bit set, IP175B will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN.<br>Bit 0.12 is cleared automatically, if this bit is set. User has to program bit 0.12 again after loop back test. | 0 |
| 4~0 | 0.13 | -- | RW | Speed Selection<br>1 = 100Mbps<br>0 = 10Mbps<br>It is valid only if bit 0.12 is set to be 0. | 1 |
| 4~0 | 0.12 | -- | RW | Auto-Negotiation Enable<br>1 = Auto-Negotiation Enable<br>0 = Auto-Negotiation Disable | 1 |
| 4~0 | 0.11 | -- | R/W | Power Down<br>1: power down mode<br>0: normal operation | 0 |
| 4~0 | 0.10 | -- | | Isolate<br>IP175B doesn’t support this function. | 0 |
| 4~0 | 0.9 | -- | RW SC | Restart Auto- Negotiation<br>1 = re-starting Auto-Negotiation<br>0 = Auto-Negotiation re-start complete<br>Setting this bit to logic high will cause IP175B to restart an Auto-Negotiation cycle, but depending on the value of bit 0.12 (Auto-Negotiation Enable). If bit 0.12 is cleared then this bit has no effect, and it is Read Only. This bit is self-clearing after Auto-Negotiation process is completed. | 0 |
| 4~0 | 0.8 | -- | R/W | Duplex mode<br>1 = full duplex<br>0 = half duplex<br>It is valid only if bit 0.12 is set to be 0. | 0 |
| 4~0 | 0.7 | -- | R/W | Collision test | 0 |
| 4~0 | 0[6:0] | -- | RO | Reserved | 0 |

**MII register 1 of PHY0~4 (Each PHY has its own MII register 1 with different PHY address)**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Status register** | | | | | |
| 4~0 | 1.15 | -- | RO | 100Base-T4 capable<br>1 = 100Base-T4 capable<br>0 = not 100Base-T4 capable<br>IP175B does not support 100Base-T4. This bit is fixed to be 0. | 0 |
| 4~0 | 1.14 | -- | RO | 100Base-X full duplex Capable<br>1 = 100Base-X full duplex capable<br>0 = not 100Base-X full duplex capable | 1 |
| 4~0 | 1.13 | -- | RO | 100Base-X half duplex Capable<br>1 = 100Base-X half duplex capable<br>0 = not 100Base-X half duplex capable | 1 |
| 4~0 | 1.12 | -- | RO | 10Base-T full duplex Capable<br>1 = 10Base-T full duplex capable<br>0 = not 10Base-T full duplex capable | 1 |
| 4~0 | 1.11 | -- | RO | 10Base-T half duplex Capable<br>1 = 10Base-T half duplex capable<br>0 = not 10Base-T half duplex capable | 1 |
| 4~0 | 1[10:7] | -- | RO | Reserved | 0 |
| 4~0 | 1.6 | -- | RO | MF preamble Suppression<br>1 = preamble may be suppressed<br>0 = preamble always required | 1 |
| 4~0 | 1.5 | -- | RO | Auto-Negotiation Complete<br>1 = Auto-Negotiation complete<br>0 = Auto-Negotiation in progress<br>When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0. | 0 |
| 4~0 | 1.4 | -- | RO LH | Remote fault<br>1 = remote fault detected<br>0 = not remote fault detected<br>When read as logic 1, indicates that IP175B has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP175B reset. | 0 |
| 4~0 | 1.3 | -- | RO | Auto-Negotiation Ability<br>1 = Auto-Negotiation capable<br>0 = not Auto-Negotiation capable<br>When read as logic 1, indicates that IP175B has the ability to perform Auto-Negotiation. | 1 |

**MII register 1 of PHY0~4 (Each PHY has its own MII register 1 with different PHY address)**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Status register** | | | | | |
| 4~0 | 1.2 | -- | RO LL | Link Status<br>1 = Link Pass<br>0 = Link Fail<br>When read as logic 1, indicates that IP175B has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers. | 0 |
| 4~0 | 1.1 | -- | | Jabber Detect<br>1 = jabber condition detected<br>0 = no jabber condition detected<br>When read as logic 1, indicates that IP175B has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP175B reset. When the duration of TXEN exceeds the jabber timer (21ms), the transmission and loop back functions will be disabled and the COL is active. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled. | 0 |
| 4~0 | 1.0 | -- | RO | Extended capability<br>1 = Extended register capabilities<br>0 = No extended register capabilities<br>IP175B has extended register capabilities. | 1 |

**MII register 2 of PHY0~4 (5 PHYs share the MII register)**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **PHY Identifier 1 register** | | | | | |
| 4~0 | 2 | -- | RO | IP175B OUI (Organizationally Unique Identifier) ID, the msb is 3rd bit of IP175B OUI ID, and the lsb is 18th bit of IP175B OUI ID. IP175B OUI is 0090C3. | 16'h0243 |

**MII register 3 of PHY0~4 (5 PHYs share the MII register)**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **PHY Identifier 2 register** | | | | | |
| 4~0 | 3[15:10] | -- | RO | PHY identifier<br>IP175B OUI ID, the msb is 19th bit of IP175B OUI ID, and lsb is 24th bit of IP175B OUI ID. | 6'h03 |
| 4~0 | 3[9:4] | -- | RO | Manufacture's Model Number<br>IP175B model number | 6'h18 |
| 4~0 | 3[3:0] | -- | RO | Revision Number<br>IP175B revision number | 0 |

**MII register 4 of PHY0~4 (Each PHY has its own MII register 4 with different PHY address)**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Auto-Negotiation Advertisement register** | | | | | |
| 4~0 | 4.15 | -- | RO | Next Page<br>Not supported. This bit is fixed to be 0. | 0 |
| 4~0 | 4.14 | -- | RO | Reserved by IEEE, write as 0, ignore on read | 0 |
| 4~0 | 4.13 | -- | R/W | Remote Fault<br>1: Advertises that this port has detected a remote fault.<br>0: There is no remote fault. | 0 |
| 4~0 | 4[12:11] | -- | RO | Reserved for future IEEE use, write as 0, ignore on read | 0 |
| 4~0 | 4.10 | -- | RW | Pause<br>1 = Advertises that this port has implemented pause function<br>0 = No pause function supported | Set by X_EN |
| 4~0 | 4.9 | -- | RO | 100BASE-T4 Not supported | 0 |
| 4~0 | 4.8 | -- | R/W | 100BASE-TX full duplex<br>1 = 100BASE-TX full duplex is supported<br>0 = 100BASE-TX full duplex is not supported | * |
| | | | | FORCE / FORCE100 / FORCE_FULL / Default | |
| | | | | 0 / Don't care / Don't care / 1 | |
| | | | | 1 / 0 / 0 / 0 | |
| | | | | 1 / 0 / 1 / 0 | |
| | | | | 1 / 1 / 0 / 0 | |
| | | | | 1 / 1 / 1 / 1 | |
| 4~0 | 4.7 | -- | R/W | 100BASE-TX<br>1 = 100BASE-TX is supported<br>0 = 100BASE-TX is not supported | * |
| | | | | FORCE / FORCE100 / FORCE_FULL / Default | |
| | | | | 0 / Don't care / Don't care / 1 | |
| | | | | 1 / 0 / 0 / 0 | |
| | | | | 1 / 0 / 1 / 0 | |
| | | | | 1 / 1 / 0 / 1 | |
| | | | | 1 / 1 / 1 / 1 | |
| 4~0 | 4.6 | -- | R/W | 10BASE-T full duplex<br>1 = 10BASE-T full duplex is supported<br>0 = 10BASE-T full duplex is not supported | * |
| | | | | FORCE / FORCE100 / FORCE_FULL / Default | |
| | | | | 0 / Don't care / Don't care / 1 | |
| | | | | 1 / 0 / 0 / 0 | |
| | | | | 1 / 0 / 1 / 1 | |
| | | | | 1 / 1 / 0 / 0 | |
| | | | | 1 / 1 / 1 / 1 | |
| 4~0 | 4.5 | -- | R/W | 10BASE-T<br>1 = 10BASE-T is supported<br>0 = 10BASE-T is not supported | 1 |
| 4~0 | 4[4:0] | -- | RO | Selector Field<br>Use to identify the type of message being sent by Auto-Negotiation. | 5'b00001 |

**MII register 5 of PHY0~4 (Each PHY has its own MII register 5 with different PHY address)**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Auto-Negotiation Link Partner Ability register** | | | | | |
| 4~0 | 5.15 | | RO | Next Page<br>1 = Next Page ability is supported by link partner<br>0 = Next Page ability does not supported by link partner | 0 |
| 4~0 | 5.14 | | RO | Acknowledge<br>1 = Link partner has received the ability data word<br>0 = Not acknowledge | 0 |
| 4~0 | 5.13 | | RO | Remote Fault<br>1 = Link partner indicates a remote fault<br>0 = No remote fault indicate by link partner<br>If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1. | 0 |
| 4~0 | 5[12:11] | -- | RO | Reserved by IEEE for future use, write as 0, read as 0. | 0 |
| 4~0 | 5.10 | -- | RW | Pause<br>1 = Link partner support IEEE802.3x<br>0 = Link partner does not support IEEE802.3x<br>When Nway enabled, this bit reflects link partner ability. (read only)<br>When Nway disabled, this bit can be set by SMI. (read/write)<br>When in 100FX, this bit is set by X_EN or SMI. | 0 |
| 4~0 | 5.9 | -- | RO | 100BASE-T4<br>1 = Link partner support 100BASE-T4<br>0 = Link partner does not support 100BASE-T4 | 0 |
| 4~0 | 5.8 | -- | RO | 100BASE-TX full duplex<br>1 = Link partner support 100BASE-TX full duplex<br>0 = Link partner does not support 100BASE-TX full duplex | 0 |
| 4~0 | 5.7 | -- | RO | 100BASE-TX<br>1 = Link partner support 100BASE-TX<br>0 = Link partner does not support 100BASE-TX<br>For 100FX mode, this bit is set. When Nway is disabled, this bit is set if register 0.13=1. | 0 |
| 4~0 | 5.6 | -- | RO | 10BASE-T full duplex<br>1 = Link partner support 10BASE-T full duplex<br>0 = Link partner does not support 10BASE-T full duplex | 0 |
| 4~0 | 5.5 | -- | RO | 10BASE-T<br>1 = Link partner support 10BASE-T<br>0 = Link partner does not support 10BASE-T<br>When Nway is disabled, this bit is set if register 0.13=0 | 0 |
| 4~0 | 5[4:0] | -- | RO | Selector Field<br>Protocol selector of the link partner | 5'b00000 |

**MII register 6 of PHY0~4 (Each PHY has its own MII register 6 with different PHY address)**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Auto-Negotiation Expansion register** | | | | | |
| 4~0 | 6[15:5] | -- | RO | Reserved | 0 |
| 4~0 | 6.4 | -- | RO | 1: a fault has been detected via parallel detection function.<br>0: a fault has not been detected via parallel detection function. | 0 |
| 4~0 | 6.3 | -- | RO | 1= Link partner is next page able.<br>0= Link partner is not next page able. | 0 |
| 4~0 | 6.2 | -- | RO | 1: IP175B next page able.<br>0: IP175B is not next page able.<br>This bit is fixed to be “0” in IP175B | 0 |
| 4~0 | 6.1 | -- | RO/ LH | 1: A new page has been received.<br>0: A new page has not been received. | 0 |
| 4~0 | 6.0 | -- | RO | If Nway is enabled, this bit means:<br>1: Link partner is Auto-Negotiation able.<br>0: Link partner is not Auto-Negotiation able.<br>In 100FX or Nway disabled, this bit always =0. | 0<br>(Nway)<br>(100FX) |

**MII registers of Switch controller**

<table>
<tr><th>PHY</th><th>MII</th><th>ROM</th><th>R/W</th><th>Description</th><th>Default</th></tr>
<tr><td>29</td><td>18.15<br>18.14</td><td>2.1<br>2.0</td><td>R/W</td><td>LED_SEL [1:0]<br>LED mode selection.<br>LED_SEL[1:0]=2'b00: LED mode 0,<br>LED_SEL[1:0]=2'b01: LED mode 1,<br>LED_SEL[1:0]=2'b10: LED mode 2,<br>LED_SEL[1:0]=2'b11: LED mode 3 (default)<br><br>It is for debug only. User should not update the setting of LED_SEL pins by writing this registers.</td><td>Pin92,<br>Pin91</td></tr>
<tr><td>29</td><td>18.13</td><td>4.7</td><td>R/W</td><td>X_EN<br>IEEE 802.3x flow control enable<br>This signal is used as pause_en for digital parts.<br>1: enable (default), 0:disable
<table>
<tr><td colspan="3">Default value</td></tr>
<tr><td colspan="2">TEST2=0</td><td>TEST2=1</td></tr>
<tr><td>Pin113 MII2_EN=1</td><td>Pin113 MII2_EN=0</td><td></td></tr>
<tr><td>1</td><td>Pin100 X_EN (1)</td><td>1</td></tr>
</table></td><td>*</td></tr>
<tr><td>29</td><td>18.12</td><td>4.4</td><td>R/W</td><td>BK_EN,<br>Backpressure enable<br>1: enable (default), 0: disable
<table>
<tr><td colspan="3">Default value</td></tr>
<tr><td colspan="2">TEST2=0</td><td>TEST2=1</td></tr>
<tr><td>Pin113 MII2_EN=1</td><td>Pin113 MII2_EN=0</td><td></td></tr>
<tr><td>1</td><td>Pin100 X_EN (1)</td><td>1</td></tr>
</table></td><td>*</td></tr>
<tr><td>29</td><td>18.11</td><td>4.2</td><td>R/W</td><td>BF_STM_EN, Broadcast storm enable<br>1: enable<br>Drop the incoming packet if the number of queued broadcast packet is over the threshold. The threshold is defined in MII register 30.11[15:14].<br>0: disable (default)
<table>
<tr><td colspan="4">Default value</td></tr>
<tr><td colspan="3">TEST2=0</td><td>TEST2=1</td></tr>
<tr><td>Pin113=1</td><td colspan="2">Pin113 MII2_EN=0</td><td></td></tr>
<tr><td></td><td>LAT_IN_DIS=1</td><td>LAT_IN_DIS=0</td><td></td></tr>
<tr><td>0</td><td>Pin102<br>BF_STM_EN (0)</td><td>0</td><td>0</td></tr>
</table></td><td>*</td></tr>
<tr><td>29</td><td>18.10</td><td>4.3</td><td>R/W</td><td>MAC_X_EN, flow control enable of MII0 and MII2<br>1: enable (default),<br>0: disable
<table>
<tr><td colspan="3">Default value</td></tr>
<tr><td colspan="2">TEST2=0</td><td>TEST2=1</td></tr>
<tr><td>Pin74 P4EXT=1</td><td>Pin74 P4EXT =0</td><td></td></tr>
<tr><td>1</td><td>Pin67 MAC_X_EN (1)</td><td>0</td></tr>
</table></td><td>*</td></tr>
</table>

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 18.5 | 6.7 | R/W | Reserved<br>The default value must be adopted for normal operation. | 0 |
| 29 | 18.4 | 6.5 | R/W | HASH_MODE<br>It is latched as Hashing algorithm selection for 1st layer and 2nd layer at the end of reset.<br>0: direct and CRC (default)<br>1: direct and CRC | 0 |
| 29 | 18.3 | 6.4 | R/W | AGING<br>Aging time of address table selection<br>An address tag in hashing table will be dropped if this function is turned on and its aging timer expires. Aging =bit[4]<br>0: no aging<br>1: aging time is around 280 sec (default) | * |
| | | | | Default value | |
| | | | | TEST2=0 / Pin74 P4EXT=1: 1<br>TEST2=0 / Pin74 P4EXT=0: Pin65 AGING (1)<br>TEST2=1: 1 | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 19.15 | 14.7 | R/W | Port0 VLAN look up table<br>Port5 and port0 are in the same VLAN | * |
| | | | | Default value | |
| | | | | Testmode38, 39 / Others | |
| | | | | 0 / 1 | |
| | 19.14 | 14.6 | R/W | Port0 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port0 are handled as high priority packets. | * |
| | | | | Default value | |
| | | | | TEST2=0 / TEST2=1 | |
| | | | | P4EXT=1 / P4EXT=0 / | |
| | | | | 0 / Pin63 COS_EN (0) / 0 | |
| | 19.13 | 14.5 | R/W | Port0 high priority port enable<br>1: enable, 0: disabled (default)<br>Packets received from port0 are handled as high priority packets. | 1'b0 |
| | 19[12.8] | 14[4:0] | R/W | Port0 VLAN look up table<br><br>The register defines the ports in the same VLAN as port0. The bit 0~4 are corresponding to port 0~4.<br>1: a port is in the same VLAN as port0<br>0: a port is not in the same VLAN as port0<br><br>Bit8, don't care;<br>Bit9=1, port 1 and port0 are in the same VLAN;<br>Bit10=1, port 2 and port0 are in the same VLAN;<br>Bit11=1, port 3 and port0 are in the same VLAN;<br>Bit12=1, port 4 and port0 are in the same VLAN | * |
| | | | | Default value | |
| | | | | Testmode38, 39 / Testmode47 / Others | |
| | | | | 5'b00111 / 5'b00001 / 5'b11111 | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 19.7 | 15.7 | R/W | Port1 VLAN look up table<br>Port5 and port1 are in the same VLAN | * |
| | | | | Default value | |
| | | | | Testmode38, 39: 0 / Others: 1 | |
| | 19.6 | 15.6 | R/W | Port1 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port1 are handled as high priority packets. | * |
| | | | | Default value | |
| | | | | TEST2=0: P4EXT=1: 0 / P4EXT=0: Pin63 COS_EN (0) / TEST2=1: 0 | |
| | 19.5 | 15.5 | R/W | Port1 high priority port enable<br>1: enable, 0: disabled (default)<br>Packets received from port1 are handled as high priority packets. | 1'b0 |
| | 19[4:0] | 15[4:0] | R/W | Port1 VLAN look up table<br><br>The register defines the ports in the same VLAN as port1. The bit 0~4 are corresponding to port 0~4.<br>1: a port is in the same VLAN as port1<br>0: a port is not in the same VLAN as port1<br><br>Bit0=1, port 0 and port1 are in the same VLAN;<br>Bit1, don't care;<br>Bit2=1, port 2 and port1 are in the same VLAN;<br>Bit3=1, port 3 and port1 are in the same VLAN;<br>Bit4=1, port 4 and port1 are in the same VLAN | * |
| | | | | Default value | |
| | | | | Testmode38, 39: 5'b01110 / Testmode47: 5'b00010 / Others: 5'b11111 | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 20.15 | 16.7 | R/W | Port2 VLAN look up table<br>Port5 and port2 are in the same VLAN<br>Default value<br>Testmode38, 39: 0<br>Others: 1 | * |
| | 20.14 | 16.6 | R/W | Port2 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port2 are handled as high priority packets.<br>Default value<br>TEST2=0: P4EXT=1: 0<br>TEST2=0: P4EXT=0: Pin63 COS_EN (0)<br>TEST2=1: 0 | * |
| | 20.13 | 16.5 | R/W | Port2 high priority port enable<br>1: enable, 0: disabled (default)<br>Packets received from port2 are handled as high priority packets. | 1'b0 |
| | 20[12:8] | 16[4:0] | R/W | Port2 VLAN look up table<br><br>The register defines the ports in the same VLAN as port2. The bit 0~4 are corresponding to port 0~4.<br>1: a port is in the same VLAN as port2<br>0: a port is not in the same VLAN as port2<br><br>Bit8=1, port 0 and port2 are in the same VLAN;<br>Bit9=1, port 1 and port2 are in the same VLAN;<br>Bit10=1, don't care;<br>Bit11=1, port 3 and port2 are in the same VLAN;<br>Bit12=1, port 4 and port2 are in the same VLAN<br>Default value<br>Testmode38, 39: 5'b11100<br>Testmode47: 5'b00100<br>Others: 5'b11111 | * |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 20.7 | 17.7 | R/W | Port3 VLAN look up table<br><br>Port5 and port3 are in the same VLAN | 1'b1 |
| | 20.6 | 17.6 | R/W | Port3 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port3 are handled as high priority packets. | * |
| | | | | Default value | |
| | | | | TEST2=0 / TEST2=1 | |
| | | | | P4EXT=1 / P4EXT=0 / | |
| | | | | 0 / Pin63 COS_EN (0) / 0 | |
| | 20.5 | 17.5 | R/W | Port3 high priority port enable<br>1: enable, 0: disabled (default)<br>Packets received from port3 are handled as high priority packets. | 1'b0 |
| | 20[4:0] | 17[4:0] | R/W | Port3 VLAN look up table<br><br>The register defines the ports in the same VLAN as port3. The bit 0~5 are corresponding to port 0~5.<br>1: a port is in the same VLAN as port3<br>0: a port is not in the same VLAN as port3<br><br>Bit0=1, port 0 and port3 are in the same VLAN;<br>Bit1=1, port 1 and port3 are in the same VLAN;<br>Bit2=1, port 2 and port3 are in the same VLAN;<br>Bit3=1, don't care;<br>Bit4=1, port 4 and port3 are in the same VLAN | * |
| | | | | Default value | |
| | | | | Testmode38, 39 / Testmode47 / Others | |
| | | | | 5'b11000 / 5'b01000 / 5'b11111 | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 21.15 | 18.7 | R/W | Port4 VLAN look up table<br>Port5 and port4 are in the same VLAN | 1'b1 |
| | 21.14 | 18.6 | R/W | Port4 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port4 are handled as high priority packets. | * |
| | | | | Default value | |
| | | | | TEST2=0 / TEST2=1 | |
| | | | | P4EXT=1 / P4EXT=0 / | |
| | | | | 0 / Pin63 COS_EN (0) / 0 | |
| | 21.13 | 18.5 | R/W | Port4 high priority port enable<br>1: enable, 0: disabled (default)<br>Packets received from port4 are handled as high priority packets. | * |
| | | | | Default value | |
| | | | | TEST2=0 / TEST2=1 | |
| | | | | P4EXT=1 / P4EXT=0 / | |
| | | | | 0 / Pin 64 P4_HIGH (0) / 0 | |
| | 21[12:8] | 18[4:0] | R/W | Port4 VLAN look up table<br><br>The register defines the ports in the same VLAN as port4. The bit 0~5 are corresponding to port 0~5.<br>1: a port is in the same VLAN as port4<br>0: a port is not in the same VLAN as port4<br><br>Bit8=1, port 0 and port4 are in the same VLAN;<br>Bit9=1, port 1 and port4 are in the same VLAN;<br>Bit10=1, port 2 and port4 are in the same VLAN;<br>Bit11=1, port 3 and port4 are in the same VLAN;<br>Bit12=1, don't care; | * |
| | | | | Default value | |
| | | | | Testmode38, 39 / Testmode47 / Others | |
| | | | | 5'b10001 / 5'b10000 / 5'b11111 | |

| PHY | MII | ROM | R/W | Description | | | Default |
|---|---|---|---|---|---|---|---|
| 29 | 22.15 | 19.4 | R/W | P4_FORCE<br>Port4 force mode enable<br>1: enable force mode<br>0: disable force mode, port4 NWAY with all capability | | | * |
| | | | | Default value | | | |
| | | | | P4EXT=1 | P4EXT=0 | | |
| | | | | | Pin 96<br>MII0_MAC_MOD=1 | Pin 96<br>MII0_MAC_MOD=0 | |
| | | | | 0 | Pin76 | Pin85 | |
| 29 | 22.14 | 19.3 | R/W | P3_FORCE<br>Port3 force mode enable<br>1: enable force mode<br>0: disable force mode, port3 NWAY with all capability | | | * |
| | | | | Default value | | | |
| | | | | P4EXT=1 | P4EXT=0 | | |
| | | | | | MII0_MAC_MOD=1 | MII0_MAC_MOD=0 | |
| | | | | 0 | Pin77 | Pin86 | |
| 29 | 22.13 | 19.2 | R/W | P2_FORCE<br>Port2 force mode enable<br>1: enable force mode<br>0: disable force mode, port2 NWAY with all capability | | | * |
| | | | | Default value | | | |
| | | | | P4EXT=1 | P4EXT=0 | | |
| | | | | | MII0_MAC_MOD=1 | MII0_MAC_MOD=0 | |
| | | | | 0 | Pin78 (0) | Pin87 (0) | |
| 29 | 22.12 | 19.1 | R/W | P1_FORCE<br>Port1 force mode enable<br>1: enable force mode<br>0: disable force mode, port1 NWAY with all capability | | | * |
| | | | | Default value | | | |
| | | | | P4EXT=1 | P4EXT=0 | | |
| | | | | | MII0_MAC_MOD=1 | MII0_MAC_MOD=0 | |
| | | | | 0 | Pin79 (0) | Pin88 (0) | |
| 29 | 22.11 | 19.0 | R/W | P0_FORCE<br>Port0 force mode enable<br>1: enable force mode<br>0: disable force mode, port0 NWAY with all capability | | | * |
| | | | | Default value | | | |
| | | | | P4EXT=1 | P4EXT=0 | | |
| | | | | | Pin 96<br>MII0_MAC_MOD=1 | Pin 96<br>MII0_MAC_MOD=0 | |
| | | | | 0 | Pin80 (0) | Pin90 (0) | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 22.10 | 20.4 | R/W | P4_FORCE100<br>It is valid only if p4_force (22[15]) is set to 1'b1. | * |
| | | | | Default value | |
| | | | | Pin 113 MII2_EN=1 / Pin 113 MII2_EN=0 | |
| | | | | 0 / Pin103 (0) | |
| P4EXT=0 | | | | P4EXT=1 | |
| 1: force port4 to be 100M<br>0: force port4 to be 10M | | | | 1: force MII0 (PHY mode) to be 100M<br>0: force MII0 (PHY mode) to be 10M | |
| 29 | 22.9 | 20.3 | R/W | P3_FORCE100<br>Force port3 to be 100M<br>1: force to be 100M<br>0: force to be 10M<br>It is valid only if p3_force (22[14]) is set to 1'b1. | * |
| | | | | Default | |
| | | | | MII2_EN=1 / Pin 113 MII2_EN=0 | |
| | | | | Pad 98.5 LAT_IN_DIS=1 / Pad 98.5 LAT_IN_DIS=0 | |
| | | | | 0 / 0 / Pin104 (0) | |
| P4EXT=0 | | | | P4EXT=1 | |
| 1: force port3 to be 100M<br>0: force port3 to be 10M | | | | 1: force MII2 (PHY mode) to be 100M<br>0: force MII2 (PHY mode) to be 10M | |
| 29 | 22.8 | 20.2 | R/W | P2_FORCE100<br>Force port2 to be 100M<br>1: force to be 100M<br>0: force to be 10M<br>It is valid only if p2_force (22[13]) is set to 1'b1. | * |
| | | | | Default | |
| | | | | MII2_EN=1 / Pin 113 MII2_EN=0 | |
| | | | | LAT_IN_DIS=1 / LAT_IN_DIS=0 | |
| | | | | 0 / 0 / Pin105 (0) | |
| 29 | 22.7 | 20.1 | R/W | P1_FORCE100<br>Force port1 to be 100M<br>1: force to be 100M<br>0: force to be 10M<br>It is valid only if p1_force (22[12]) is set to 1'b1. | * |
| | | | | Default | |
| | | | | Pin 113 MII2_EN=1 / Pin 113 MII2_EN=0 | |
| | | | | 0 / Pin106 (0) | |
| 29 | 22.6 | 20.0 | R/W | P0_FORCE100<br>Force port0 to be 100M<br>1: force to be 100M<br>0: force to be 10M<br>It is valid only if p0_force (22[11]) is set to 1'b1. | * |
| | | | | Default | |
| | | | | MII2_EN=1 / Pin 113 MII2_EN=0 | |
| | | | | LAT_IN_DIS=1 / LAT_IN_DIS=0 | |
| | | | | 0 / 0 / Pin107 (0) | |

| PHY | MII | ROM | | Description | | | Default |
|---|---|---|---|---|---|---|---|
| 29 | 22.5 | 21.4 | R/W | P4_FORCE_FULL<br>It is valid only if p4_force (22.15) is set to 1'b1. | | | * |
| | | | | Default | | | |
| | | | | MII2_EN=1 | Pin 113 MII2_EN=0 | | |
| | | | | | Pad 98.5<br>LAT_IN_DIS=1 | Pad 98.5<br>LAT_IN_DIS=0 | |
| | | | | 0 | 0 | Pin108 (0) | |
| P4EXT=0 | | | | P4EXT=1 | | | |
| 1: force port4 to be full duplex<br>0: force port4 to be half duplex | | | | 1: force MII0 (PHY mode) to be full duplex<br>0: force MII0 (PHY mode) to be half duplex | | | |
| 29 | 22.4 | 21.3 | R/W | P3_FORCE_FULL<br>Force port3 to be full duplex<br>1: force full duplex<br>0: force half duplex<br>It is valid only if p4_force (22.14) is set to 1'b1. | | | * |
| | | | | Default | | | |
| | | | | MII2_EN=1 | Pin 113 MII2_EN=0 | | |
| | | | | 0 | Pin109 (0) | | |
| P4EXT=0 | | | | P4EXT=1 | | | |
| 1: force port3 to be full duplex<br>0: force port3 to be half duplex | | | | 1: force MII2 (PHY mode) to be full duplex<br>0: force MII2 (PHY mode) to be half duplex | | | |
| 29 | 22.3 | 21.2 | R/W | P2_FORCE_FULL<br>Force port2 to be full duplex<br>1: force full duplex<br>0: force half duplex<br>It is valid only if p4_force (22.13) is set to 1'b1. | | | * |
| | | | | Default | | | |
| | | | | MII2_EN=1 | Pin 113 MII2_EN=0 | | |
| | | | | | Pad 98.5<br>LAT_IN_DIS=1 | Pad 98.5<br>LAT_IN_DIS=0 | |
| | | | | 0 | 0 | Pin110 (0) | |
| 29 | 22.2 | 21.1 | R/W | P1_FORCE_FULL<br>Force port1 to be full duplex<br>1: force full duplex<br>0: force half duplex<br>It is valid only if p4_force (22.12) is set to 1'b1. | | | * |
| | | | | Default | | | |
| | | | | MII2_EN=1 | Pin 113 MII2_EN=0 | | |
| | | | | | Pad 98.5<br>LAT_IN_DIS=1 | Pad 98.5<br>LAT_IN_DIS=0 | |
| | | | | 0 | 0 | Pin111 (0) | |
| 29 | 22.1 | 21.0 | R/W | P0_FORCE_FULL<br>Force port0 to be full duplex<br>1: force full duplex<br>0: force half duplex<br>It is valid only if p4_force (22.11) is set to 1'b1. | | | * |
| | | | | Default | | | |
| | | | | MII2_EN=1 | Pin 113 MII2_EN=0 | | |
| | | | | 0 | Pin112 (0) | | |

**Tag register 10**

| PHY | MII | ROM | R/W | Description | | Default |
|---|---|---|---|---|---|---|
| 29 | 23[15:11] | 22[4:0] | R/W | ADD_TAG. Add VLAN tag<br>Portx adds a VLAN tag defined in vlan_tag_x to each outgoing packet | | 5'h00 |
| | | | | Bit 11 | 1: port0 adds a VLAN tag to each outgoing packet.<br>0: port0 doesn't add a VLAN tag. | |
| | | | | Bit 12 | 1: port1 adds a VLAN tag to each outgoing packet.<br>0: port1 doesn't add a VLAN tag. | |
| | | | | Bit 13 | 1: port2 adds a VLAN tag to each outgoing packet.<br>0: port2 doesn't add a VLAN tag. | |
| | | | | Bit 14 | 1: port3 adds a VLAN tag to each outgoing packet.<br>0: port3 doesn't add a VLAN tag. | |
| | | | | Bit 15 | 1: port4 adds a VLAN tag to each outgoing packet.<br>0: port4 doesn't add a VLAN tag. | |

**Tag register 11**

| PHY | MII | ROM | R/W | Description | | Default |
|---|---|---|---|---|---|---|
| 29 | 23[10:6] | 23[4:0] | R/W | REMOVE_TAG. Remove VLAN tag | | 5'h00 |
| | | | | Bit 6 | 1: port0 removes the VLAN tag of each outgoing packet.<br>0: port0 doesn't remove the VLAN tag of each outgoing packet. | |
| | | | | Bit 7 | 1: port1 removes the VLAN tag of each outgoing packet.<br>0: port1 doesn't remove the VLAN tag of each outgoing packet. | |
| | | | | Bit 8 | 1: port2 removes the VLAN tag of each outgoing packet.<br>0: port2 doesn't remove the VLAN tag of each outgoing packet. | |
| | | | | Bit 9 | 1: port3 removes the VLAN tag of each outgoing packet.<br>0: port3 doesn't remove the VLAN tag of each outgoing packet. | |
| | | | | Bit 10 | 1: port4 removes the VLAN tag of each outgoing packet.<br>0: port4 doesn't remove the VLAN tag of each outgoing packet. | |
| | | | | Default value | | |
| | | | | Others | Testmode37 | |
| | | | | 5'b00000 | 5'b11111 | |
| | 23.1 | 22.5 | R/W | ADD_TAG. Add VLAN tag<br>1: Port5 adds a VLAN tag to each outgoing packet.<br>0: Port5 doesn't add a VLAN tag. | | * |
| | | | | Default value | | |
| | | | | Others | Testmode37 | |
| | | | | 0 | 1 | |
| | 23.0 | 23.5 | R/W | REMOVE_TAG. Remove VLAN tag<br>1: Port5 removes the VLAN tag of each outgoing packet.<br>0: port5 doesn't remove the VLAN tag of each outgoing packet. | | 1'b0 |

**Tag register 1~9**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 24 | 25[7:0]<br>24[7:0] | R/W | VLAN_TAG_0. Port0 default VLAN tag value<br>This register defines the VLAN tag added to an un-tagged packet from port 0. | 16'h0001 |
| 29 | 25 | 27[7:0]<br>26[7:0] | R/W | VLAN_TAG_1. Port1 default VLAN tag value<br>This register defines the VLAN tag added to an un-tagged packet from port 1. | 16'h0001 |
| 29 | 26 | 29[7:0]<br>28[7:0] | | VLAN_TAG_2. Port2 default VLAN tag value<br>This register defines the VLAN tag added to an un-tagged packet from port 2. | 16'h0001 |
| 29 | 27 | 31[7:0]<br>30[7:0] | R/W | VLAN_TAG_3. Port3 default VLAN tag value<br>This register defines the VLAN tag added to an un-tagged packet from port 3. | 16'h0001 |
| 29 | 28 | 33[7:0]<br>32[7:0] | R/W | VLAN_TAG_4. Port4 default VALN tag value<br>This register defines the VLAN tag added to an un-tagged packet from port 4. | 16'h0002 |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 29[15:8] | 36[7:0] | R/W | REG29SW- reserved | 8'h01 |
| 29 | 29[7:0] | 35[7:0] | R/W | REG29SW- reserved | 8'h00 |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 30 | 38[7:0]<br>37[7:0] | R/W | VLAN_TAG_5. Port5 default VALN tag value<br>This register defines the VLAN tag of an un-tagged packet from port 5. | 16'h0002 |

**IP175B enable register**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 29 | 31 | -- | R/W | IP175B register enable register<br><br>IP175B MII register don't support IP175A compatible mode. If the value of this register is 16'h175A, please fill this register with 16'h175C.<br><br>Note1:<br>The default value is 16'h175A if p4ext is 1, MII1_dis is, 0 and mii1_phy_mod is 1; otherwise the default value is 16'h175C. | Note1 |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 0 | -- | R/W | Software reset register<br>IP175B is reset if uses write “175C”to this register. It is self-cleared. The reset period is around 2ms. User has to wait for at least 2ms to access IP175B.<br>MII registers 29.x, 30.x, 31.x are not reset by software reset. | 16’h00 |

**Tag VLAN register 2**

| PHY | MII | ROM | R/W | Description | | Default |
|---|---|---|---|---|---|---|
| 30 | 1[5:0] | 39[5:0] | R/W | TAG_VLAN_MASK_0[5:0].<br>Tag VLAN 0 output port mask<br><br>The mask is valid only if MII register 9.7 TAG_VLAN_EN is logic high and VID index is 4'b0000.<br><br>When IP175B receives a packet, it examines the VID index to choose a tag VLAN mask and forwards the packets according MAC address table and the mask. | | 6'h3f |
| | | | | Bit0 | 1: port 0 belongs to VLAN 0<br>0: port 0 doesn't belong to VLAN 0 | |
| | | | | Bit1 | 1: port 1 belongs to VLAN 0<br>0: port 1 doesn't belong to VLAN 0 | |
| | | | | Bit2 | 1: port 2 belongs to VLAN 0<br>0: port 2 doesn't belong to VLAN 0 | |
| | | | | Bit3 | 1: port 3 belongs to VLAN 0<br>0: port 3 doesn't belong to VLAN 0 | |
| | | | | Bit4 | 1: port 4 belongs to VLAN 0<br>0: port 4 doesn't belong to VLAN 0 | |
| | | | | Bit5 | 1: port 5 belongs to VLAN 0<br>0: port 5 doesn't belong to VLAN 0 | |

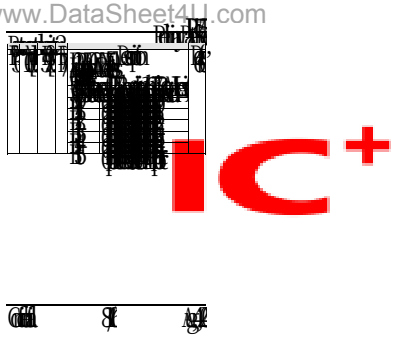
**Tag VLAN register 3~17**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 1[13:8] | 40[5:0] | R/W | TAG_VLAN_MASK_1[5:0]. Tag VLAN 1 output port mask | 6'h2f |
| | 2[13:8] | 42[5:0] | R/W | TAG_VLAN_MASK_3[5:0]. Tag VLAN 3 output port mask | 6'h3f |
| | 2[5:0] | 41[5:0] | R/W | TAG_VLAN_MASK_2[5:0]. Tag VLAN 2 output port mask | 6'h30 |
| | 3[13:8] | 44[5:0] | R/W | TAG_VLAN_MASK_5[5:0]. Tag VLAN 5 output port mask | 6'h3f |
| | 3[5:0] | 43[5:0] | R/W | TAG_VLAN_MASK_4[5:0]. Tag VLAN 4 output port mask | 6'h3f |
| | 4[13:8] | 46[5:0] | R/W | TAG_VLAN_MASK_7[5:0]. Tag VLAN 7 output port mask | 6'h3f |
| | 4[5:0] | 45[5:0] | R/W | TAG_VLAN_MASK_6[5:0]. Tag VLAN 6 output port mask | 6'h3f |
| | 5[13:8] | 48[5:0] | R/W | TAG_VLAN_MASK_9[5:0]. Tag VLAN 9 output port mask | 6'h3f |
| | 5[5:0] | 47[5:0] | R/W | TAG_VLAN_MASK_8[5:0]. Tag VLAN 8 output port mask | 6'h3f |
| | 6[13:8] | 50[5:0] | R/W | TAG_VLAN_MASK_B[5:0]. Tag VLAN b output port mask | 6'h3f |
| | 6[5:0] | 49[5:0] | R/W | TAG_VLAN_MASK_A[5:0]. Tag VLAN a output port mask | 6'h3f |
| | 7[13:8] | 52[5:0] | R/W | TAG_VLAN_MASK_D[5:0]. Tag VLAN d output port mask | 6'h3f |
| | 7[5:0] | 51[5:0] | R/W | TAG_VLAN_MASK_C[5:0]. Tag VLAN c output port mask | 6'h3f |
| | 8[13:8] | 54[5:0] | R/W | TAG_VLAN_MASK_F[5:0]. Tag VLAN f output port mask | 6'h3f |
| | 8[5:0] | 53[5:0] | R/W | TAG_VLAN_MASK_E[5:0]. Tag VLAN e output port mask | 6'h3f |

**Router control register 1**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 9[12:8] | 56[4:0] | R/W | WAN_PORTS[4:0].<br>WAN ports for router application<br><br>It is valid only if router_en is enabled.<br>Bit0: 1: port 0 is a WAN port; 0: port 0 is not a WAN port<br>Bit1: 1: port 1 is a WAN port; 0: port 1 is not a WAN port<br>Bit2: 1: port 2 is a WAN port; 0: port 2 is not a WAN port<br>Bit3: 1: port 3 is a WAN port; 0: port 3 is not a WAN port<br>Bit4: 1: port 4 is a WAN port; 0: port 4 is not a WAN port | 5'h10 |
| 30 | 9.7 | 55.7 | R/W | TAG_VLAN_EN. Enable tag VLAN function<br>1: enable tag VLAN function<br>0: disable tag VLAN function<br>Default value<br>Others: Testmode37<br>0: 1 | * |
| | 9[6:4] | 55[6:4] | R/W | VID_IDX_SEL. VID index selection<br>Select 4 bits out of 12 bits VID as index of tag VLAN groups. The 12 bits of VID can't be all zeros; otherwise, it will be handled as an un-tagged frame.<br><br>000: VID[3:0], 001: VID[4:1], 010: VID[5:2], 011: VID[6:3], 100: VID[7:4], 101: VID[8:5], 110: VID[9:6], 111: VID[10:7]<br><br>An example of vid_idx_sel = 3'b000,<br>VLAN_0: VID[3:0] = 4'b0000<br>VLAN_1: VID[3:0] = 4'b0001<br>VLAN_2: VID[3:0] = 4'b0010<br>VLAN_3: VID[3:0] = 4'b0011<br>….: ….<br>VLAN_e: VID[3:0] = 4'b1110<br>VLAN_f: VID[3:0] = 4'b1111 | 3'b000 |
| 30 | 9.3 | 55.3 | R/W | ROUTER_EN.<br>Enable router function at MII port<br>1: SMART MAC enabled.<br>0: SMART MAC disabled.<br>Default value<br>Others: Testmode37<br>0: 1 | * |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 9[2:0] | 55[2:0] | R/W | LAN_GROUPS[2:0].<br><br>Number of VLAN groups of LAN ports in a router application<br><br>It defines the VLANs used by LAN ports. Each VLAN should contain MII port.<br><br>It is valid only if router_en is enabled.<br><br>000: unsupported value<br>001: 1 VLAN group, (VLAN 1)<br>010: 2 VLAN groups, (VLAN 1~VLAN 2)<br>011: 3 VLAN groups, (VLAN 1~VLAN 3)<br>100: 4 VLAN groups, (VLAN 1~VLAN 4)<br>101: 5 VLAN groups, (VLAN 1~VLAN 5)<br>110: 6 VLAN groups, (VLAN 1~VLAN 6)<br>111: 7 VLAN groups, (VLAN 1~VLAN 7) | 3'b001 |



**Switch control register 3**

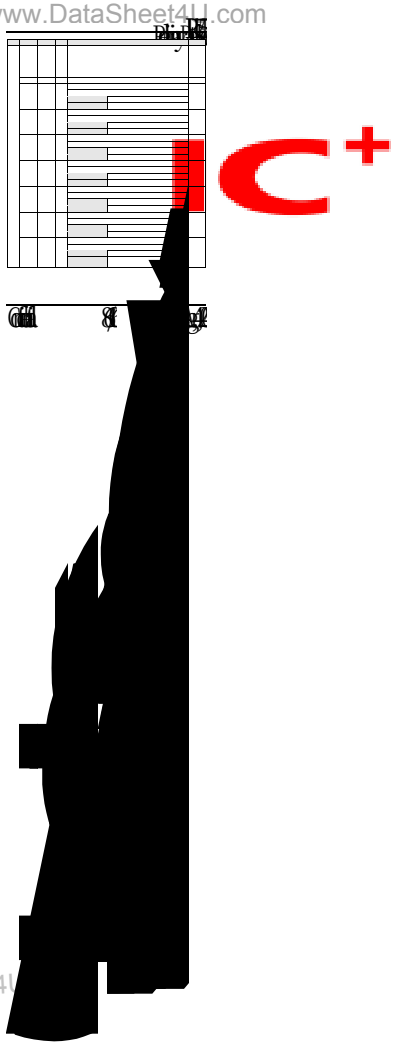
| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 11[15:14] | 59[7:6] | R/W | BF_STM_THR_SEL[1:0].<br>Broadcast storm threshold selection<br>00: 159 packets/10ms for 100Mbps port, or 159 packets/100ms for 10Mbps port,<br>01: 127 packets/10ms for 100Mbps port, or 127 packets/100ms for 10Mbps port,<br>10: 63 packets/10ms for 100Mbps port, or 63 packets/100ms for 10Mbps port,<br>11: 31 packets/10ms for 100Mbps port, or 31 packets/100ms for 10Mbps port, | 2'b00 |
| | 11[13:12] | 59[5:4] | R/W | The default value should be adopted for normal operation. | 2'b00 |
| | 11[11:10] | 59[3:2] | R/W | The default value should be adopted for normal operation. | 2'b00 |
| | 11[9:8] | 59[1:0] | R/W | UNIT_LOW_THR_SEL[1:0]<br>The default value should be adopted for normal operation. | 2'b00 |
| | 11[7:6] | 58[7:6] | R/W | UNIT_HIGH_THR_SEL[1;0].<br>The default value should be adopted for normal operation. | 2'b00 |
| | 11.5 | 58.5 | R/W | BF_STM_EN_QM<br>The default value should be adopted for normal operation. | 1'b0 |
| | 11.4 | 58.4 | R/W | PREDROP_EN<br>1: Drop an incoming broadcast packet if any port is congested.<br>0: forward an incoming broadcast packet to un-congested ports instead of congested ports. | 1'b0 |
| | 11[3:2] | 58[3:2] | R/W | PKT_LOW_THR_SEL[1:0].<br>The default value should be adopted for normal operation. | 2'b00 |
| | 11[1:0] | 58[1:0] | R/W | PKT_HIGH_THR_SEL[1:0].<br>The default value should be adopted for normal operation. | 2'b00 |

<table>
<tr><th>PHY</th><th>MII</th><th>ROM</th><th>R/W</th><th>Description</th><th>Default</th></tr>
<tr><td rowspan="6">30</td><td>12.7</td><td>60.7</td><td>R/W</td><td>LINK_Q_EN, LINK quality enable<br>1: enable (default),<br>0: disable<br>Default value<br>TEST2=0 | TEST2=1<br>Pad 98.5 LAT_IN_DIS=1 | Pad 98.5 LAT_IN_DIS=0 |<br>1 | Pin101 (1) | 1</td><td>*</td></tr>
<tr><td>12.5</td><td>60.5</td><td>R/W</td><td>LONG_PACKET<br>Max forwarded packet length<br>1: 1552 bytes<br>0: 1536 bytes (default)<br>Default value<br>P4EXT=1 | P4EXT=0<br>0 | Pin66 LONG_PKT (0)</td><td>*</td></tr>
<tr><td>12.4</td><td>60.4</td><td>R/W</td><td>PRIORITY_RATE<br>1: 8 packets<br>0: 4 packets<br>Output Queue Scheduling: high priority packet rate</td><td>1’b0</td></tr>
<tr><td>12.1</td><td>60.1</td><td>R/W</td><td>Reserved (Must to be keep at 1’b1)</td><td>1’b1</td></tr>
<tr><td>12.0</td><td>60.0</td><td>R/W</td><td>HP_DIS_FLOW_EN<br>High priority packet to disable flow control<br>1: a port will disable its flow control function for 2 sec if it receives a high priority packet.<br>0: the function is disabled</td><td>1’b0</td></tr>
</table>

| PHY | MII | | R/W | Description | | Default |
|---|---|---|---|---|---|---|
| 30 | 13[3:0] | 96[3:0] | R/W | RESERVED_ADD_FORWARD[3:0] | | * |
| | | | | BIT3 | Reserved MAC address (0180C2000010-0180C20000FF)<br>1: forward (default),<br>0: discard. | |
| | | | | BIT2 | Reserved MAC address (0180C2000002- 0180C200000F)<br>1: forward (default),<br>0: discard.<br>The default value is the inverted value of pin 69 FILTER_RSV_DA. | |
| | | | | BIT1 | Reserved MAC address (0180C2000001)<br>1: forward,<br>0: discard (default) | |
| | | | | BIT0 | Reserved MAC address (0180C2000000)<br>1: forward (default),<br>0: discard | |
| | | | | Default value | | |
| | | | | P4EXT=1 | P4EXT=0 | |
| | | | | 1101 | {1, inv of pin69 FILTER_RSV_DA(0), 0, 1} | |

**Spanning tree register**

| PHY | MII | ROM | | Description | Default |
|---|---|---|---|---|---|
| 30 | 16.15 | -- | RO | Fast mode for simulation,<br>1: Fast mode, 0: normal mode<br>Default value<br>TEST2=0 / TEST2=1<br>0 / Pin 66 FASTMODE (0) | * |
| | 16.12 | 66.4 | R/W | Learning enable<br>1: enable address learning capability of port 4<br>0: disable address learning capability of port 4 | 1 |
| | 16.11 | 66.3 | R/W | Learning enable<br>1: enable address learning capability of port 3<br>0: disable address learning capability of port 3 | 1 |
| | 16.10 | 66.2 | R/W | Learning enable<br>1: enable address learning capability of port 2<br>0: disable address learning capability of port 2 | 1 |
| | 16.9 | 66.1 | R/W | Learning enable<br>1: enable address learning capability of port 1<br>0: disable address learning capability of port 1 | 1 |
| | 16.8 | 66.0 | R/W | Learning enable<br>1: enable address learning capability of port 0<br>0: disable address learning capability of port 0 | 1 |
| | 16.7 | 65.7 | R/W | Stag_en special tagging function enable<br>If this function is enabled, IP175B inserts source port information in tag header.<br>1: enable special tagging function<br>0: disable special tagging function | 0 |
| | 16.4 | 65.4 | R/W | Forward enable<br>1: enable receiving function of port 4<br>0: disable receiving function of port 4 | 1 |
| | 16.3 | 65.3 | R/W | Forward enable<br>1: enable receiving function of port 3<br>0: disable receiving function of port 3 | 1 |
| | 16.2 | 65.2 | R/W | Forward enable<br>1: enable receiving function of port 2<br>0: disable receiving function of port 2 | 1 |
| | 16.1 | 65.1 | R/W | Forward enable<br>1: enable receiving function of port 1<br>0: disable receiving function of port 1 | 1 |
| | 16.0 | 65.0 | R/W | Forward enable<br>1: enable receiving function of port 0<br>0: disable receiving function of port 0 | 1 |



| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 18.15 | -- | RO | mii1_full | 1 |
| | 18.14 | -- | RO | mii1_speed10 | 0 |
| | 18.13 | -- | RO | mii0_full | 0 |
| | 18.12 | -- | RO | mii0_speed10 | 1 |
| | 18.11 | 12.6 | R/W | allpass | 0 |
| | 18.10 | 6.1 | R/W | modbck | 1 |
| | 18.9 | 6.2 | R/W | twopart | 1 |
| | 18.8 | 5.3 | R/W | bp_kind | 0 |
| | 18.7 | 13.7 | R/W | Port5 VLAN look up table<br><br>Port5 and port5 are in the same VLAN. This bit is “don’t care”. It is fixed “1”. | 1’b1 |
| | 18.6 | 13.6 | R/W | Port5 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from Port5 are handled as high priority packets.<br>Default value<br>TEST2=0 / TEST2=1<br>P4EXT=1 / P4EXT=0 / <br>0 / Pin 63 COS_EN (0) / 0 | * |
| | 18.5 | 13.5 | R/W | Port5 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from Port5 are handled as high priority packets. | 1’b0 |
| | 18[4:0] | 13[4:0] | R/W | Port5 VLAN look up table<br><br>The register defines the ports in the same VLAN as port5. The bit 0~5 are corresponding to port 0~5.<br>1: a port is in the same VLAN as Port5<br>0: a port is not in the same VLAN as MI port<br><br>Bit0=1, port 0 and Port5 are in the same VLAN;<br>Bit1=1, port 1 and Port5 are in the same VLAN;<br>Bit2=1, port 2 and Port5 are in the same VLAN;<br>Bit3=1, port 3 and Port5 are in the same VLAN;<br>Bit4=1, port 4 and Port5 are in the same VLAN;<br>Bit5=1, don’t care;<br>Default value<br>Test mode 38,39 / Others<br>6'b100011 / 6'b111111 | * |

| PHY | MII | ROM | R/W | | Default |
|---|---|---|---|---|---|
| 30 | 20 | 68<br>67 | R/W | static_mac_0[15:0] | 16'h0000 |
| 30 | 21 | 70<br>69 | R/W | static_mac_0[31:16] | 16'hc200 |
| 30 | 22 | 72<br>71 | R/W | static_mac_0[47:32] | 16'h0180 |
| 30 | 23 | 74<br>73 | R/W | static_mac_1[15:0] | 16'h0000 |
| 30 | 24 | 76<br>75 | R/W | static_mac_1[31:16] | 16'h0000 |
| 30 | 25 | 78<br>77 | R/W | static_mac_1[47:32] | 16'h0000 |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 26.15 | 80.7 | R/W | static_overide_1<br>1: override the transmission, receiving and learning setting in MII register 30.16.<br>0: not override | 0 |
| 30 | 26.14 | 80.6 | R/W | static_valid_1<br>1: the entry is valid<br>0: the entry is not valid | 0 |
| 30 | 26[13:8] | 80[5:0] | R/W | static_port_mask_1<br>Bit [13]: forward to port 5 (MII0)<br>Bit [12]: forward to port 4<br>Bit [11]: forward to port 3<br>Bit [10]: forward to port 2<br>Bit [9]: forward to port 1<br>Bit [8]: forward to port 0 | 6'b100000 |
| 30 | 26.7 | 79.7 | R/W | static_overide_0<br>1: override the transmission, receiving and Learning setting in MII register 30.16.<br>0: not override | 1 |
| 30 | 26.6 | 79.6 | R/W | static_valid_0<br>1: the entry is valid<br>0: the entry is not valid | 0 |
| 30 | 26[5:0] | 79[5:0] | R/W | static_port_mask_0<br>Bit [5]: forward to port 5 (MII0)<br>Bit [4]: forward to port 4<br>Bit [3]: forward to port 3<br>Bit [2]: forward to port 2<br>Bit [1]: forward to port 1<br>Bit [0]: forward to port 0 | 6'b100000 |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 27.8 | 5.0 | R/W | MBSTM DISABLE<br>Multicast broadcast storm protection disable<br>1: “Broadcast storm protection” does not include multicast packets. IP175B drops the packets with DA = FFFFFFFF only when the broadcast threshold is reached (default),<br>0: “Broadcast storm protection” includes multicast packets. IP175B drops the packets with DA = FFFFFFFF, or multi-cast address when the broadcast threshold is reached.<br><br>“Broadcast storm protection” does not drop packets due to not learned address. | 1 |
| 30 | 27.0 | 81.0 | R/W | DIFFSEV_EN<br>1: DiffServ is enabled, 0: Diffserv is disabled (default) | 0 |
| 30 | 28 | 83, 82 | R/W | DSCP[15:0]<br>Lookup table for DiffServ | 0 |
| 30 | 29 | 85, 84 | R/W | DSCP[31:16]<br>Lookup table for DiffServ | 0 |
| 30 | 30 | 87, 86 | R/W | DSCP[47:32]<br>Lookup table for DiffServ | 0 |
| 30 | 31 | 89, 88 | R/W | DSCP[63:48]<br>Lookup table for DiffServ | 0 |

| PHY | MII | ROM | R/W | Description | | | | | Default |
|---|---|---|---|---|---|---|---|---|---|
| 31 | 2[14:12] | 95[6:4] | R/W | BW_CONTROL_P5_TX[2:0] | | | | | 000 |
| | | | | [2:0] | BW, bps | 64-byte ,bytes | 1518-byte ,bytes | random length ,bytes | |
| | | | | 000 | Full rate | Full rate | Full rate | Full rate | |
| | | | | 001 | 128 Kbps | 13,459 | 79,806 | 48,769 | |
| | | | | 010 | 256 Kbps | 30,281 | 79,807 | 52,955 | |
| | | | | 011 | 512 Kbps | 57,201 | 79,803 | 87,182 | |
| | | | | 100 | 1 Mbps | 111,051 | 159,606 | 148,281 | |
| | | | | 101 | 2 Mbps | 225,400 | 319,249 | 273,923 | |
| | | | | 110 | 4 Mbps | 447,478 | 558,556 | 508,248 | |
| | | | | 111 | 8 Mbps | 898,330 | 1,037,449 | 1,009,446 | |
| 31 | 2[10:8] | 95[2:0] | R/W | BW_CONTROL_P5_RX[2:0] | | | | | 000 |
| | | | | [2:0] | BW, bps | 64-byte ,bytes | 1518-byte ,bytes | random length ,bytes | |
| | | | | 000 | Full rate | Full rate | Full rate | Full rate | |
| | | | | 001 | 128Kbps | 20,187 | 159,622 | 92,156 | |
| | | | | 010 | 256Kbps | 37,009 | 159,621 | 100,183 | |
| | | | | 011 | 512Kbps | 63,994 | 159,610 | 131,723 | |
| | | | | 100 | 1 Mbps | 117,431 | 239,414 | 192,672 | |
| | | | | 101 | 2 Mbps | 231,780 | 399,013 | 314,536 | |
| | | | | 110 | 4 Mbps | 454,295 | 638,412 | 561,996 | |
| | | | | 111 | 8 Mbps | 905,064 | 1,117,149 | 1,062,681 | |
| 31 | 2[6:4] | 94[6:4] | R/W | BW_CONTROL_P4_TX[2:0] | | | | | 000 |
| 31 | 2[2:0] | 94[2:0] | R/W | BW_CONTROL_P4_RX[2:0] | | | | | 000 |
| 31 | 1[14:12] | 93[6:4] | R/W | BW_CONTROL_P3_TX[2:0] | | | | | 000 |
| 31 | 1[10:8] | 93[2:0] | R/W | BW_CONTROL_P3_RX[2:0] | | | | | 000 |
| 31 | 1[6:4] | 92[6:4] | R/W | BW_CONTROL_P2_TX[2:0] | | | | | 000 |
| 31 | 1[2:0] | 92[2:0] | R/W | BW_CONTROL_P2_RX[2:0] | | | | | 000 |
| 31 | 0[14:12] | 91[6:4] | R/W | BW_CONTROL_P1_TX[2:0] | | | | | 000 |
| 31 | 0[10:8] | 91[2:0] | R/W | BW_CONTROL_P1_RX[2:0] | | | | | 000 |
| 31 | 0[6:4] | 90[6:4] | R/W | BW_CONTROL_P0_TX[2:0] | | | | | 000 |
| 31 | 0[2:0] | 90[2:0] | R/W | BW_CONTROL_P0_RX[2:0] | | | | | 000 |

**MII0 MAC mode register**

| PHY | MII | | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 3.15 | -- | RO | Flow control capability of the link partner of external PHY on MII0<br>1: link partner supports flow control,<br>0: link partner does not support flow control | 1 |
| 31 | 3.14 | -- | RO | Mac_force[0]<br>1: MII0's speed and duplex are forced because IP175B finds external PHY doesn't support SMI<br>0: MII0 polls external PHY through SMI to decide its speed and duplex. | |
| 31 | 3.13 | -- | RO | MII0_link<br>1: link ok, 0: un-link | |
| 31 | 3[12:8] | 98[4:0] | R/W | Capability of external PHY on MII0<br>bit12: flow control ability,<br>bit11: 100M full duplex,<br>bit10 : 100M half duplex,<br>bit9 : 10M full duplex,<br>bit8: 10M half duplex | 11111 |
| 31 | 3.7 | -- | RO | Speed of external PHY on MII0<br>1: 10M,<br>0: 100M | 0 |
| 31 | 3.6 | -- | RO | Duplex of external PHY on MII0<br>1: full duplex,<br>0: half duplex | 0 |
| 31 | 3.5 | -- | RO | Link status of external PHY on MII0<br>1: link on,<br>0: link off | 0 |
| 31 | 3[4:0] | 97[4:0] | R/W | MII0_mac_phy_addr | 00000 |

**MII1 MAC mode or MII2 MAC mode register (Only one is active at the same time.)**

| PHY | MII | ROM | R/W | | Default |
|---|---|---|---|---|---|
| 31 | 4.15 | -- | RO | Flow control capability of the link partner of external PHY on MII1 MAC or MII2 MAC<br>1: link partner supports flow control,<br>0: link partner does not support flow control | 1 |
| 31 | 4.14 | -- | RO | Mac_force[1]<br>1: MII1orMII2's speed and duplex are forced because IP175B finds external PHY doesn't support SMI<br>0: MII1orMII2 polls external PHY through SMI to decide its speed and duplex. | |
| 31 | 4.13 | -- | RO | MII1orMII2 _link<br>1: link ok, 0: un-link | |
| 31 | 4[12:8] | 100[4:0] | R/W | Capability of external PHY on MII1 MAC or MII2 MAC<br>bit12: flow control ability,<br>bit11: 100M full duplex,<br>bit10 : 100M half duplex,<br>bit9 : 10M full duplex,<br>bit8: 10M half duplex | 11111 |
| 31 | 4.7 | -- | RO | Speed of external PHY on MII1 MAC or MII2 MAC<br>1: 10M,<br>0: 100M | 0 |
| 31 | 4.6 | -- | RO | Duplex of external PHY on MII1 MAC or MII2 MAC<br>1: full duplex,<br>0: half duplex | 0 |
| 31 | 4.5 | -- | RO | Link status of external PHY on MII1 MAC or MII2 MAC<br>1: link on,<br>0: link off | 0 |
| 31 | 4[4:0] | 99[4:0] | R/W | MII1orMII2_mac_phy_addr | 00001 |

**MII1, MII1 and MII2 control register**

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 5.15 | 7.0 | R/W | P4EXT<br>1: enable<br>0: disable (default) | Pin74 |
| 31 | 5.14 | -- | RO | SMI0_polling<br>1: MII0 MAC mode, 0: MII0 PHY mode | |
| 31 | 5.13 | -- | RO | SMI1_polling<br>1: MII1 MAC mode, 0: MII1 PHY mode | |
| 31 | 5.12 | 7.4 | R/W | MII1_PHY_MOD<br>1: MII1 is connected to PHY4.0: MII1 is connected to MAC4. | Pin54(1) |
| 31 | 5.11 | 60.2 | R/W | MII0_mac_mode_en<br>External MII0 port MAC mode<br>1: MII0 works as a MAC and should be connected to an external PHY.<br>0: MII0 works as a PHY and should be connected to an external MAC device (default).<br>This bit does not affect MII1 port.<br>Default value<br>MII2_EN=1 / MII2_EN=0<br>0 / Pin96 MII0_MAC_MODE (0) | * |
| 31 | 5.10 | 60.3 | R/W | MII0_RMII_EN<br>1: MII0 RMII interface enabled<br>0: MII0 RMII interface disabled (default).<br>Default value<br>P4EXT=1 & RMII_EN=1 / Others<br>1 / 0 | Pin(0) |
| 31 | 5.9 | 3.5 | R/W | MII2_RMII_EN<br>1: MII2 RMII interface enabled<br>0: MII2 RMII interface disabled (default).<br>Default value<br>P4EXT=1 & RMII_EN=1 & MII2_EN=1 / Others<br>1 / 0 | * |
| 31 | 5.8 | 3.4 | R/W | MII1_RMII_EN<br>1: MII1 RMII interface enabled<br>0: MII1 RMII interface disabled (default).<br>Default value<br>P4EXT=1 & RMII_EN=1 & MII1_DIS=0 / Others<br>1 / 0 | * |
| 31 | 5.7 | 3.3 | R/W | MII1OR2_MAC_REPEATER<br>1: external PHY 's TXEN does not loop back to CRS (default)<br>0: external PHY 's TXEN loop back to CRS | 1 |
| 31 | 5.6 | 3.2 | R/W | MII0_MAC_REPEATER<br>1: external PHY 's TXEN does not loop back to CRS (default)<br>0: external PHY 's TXEN loop back to CRS | 1 |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 5.5 | 3.1 | R/W | MII2_PHY_COL_DELAY<br>0: no delay,<br>1: collision delay 24 clocks (default)<br>It is valid only if MII2 is enabled and it works at PHY mode. | 1 |
| 31 | 5.4 | 3.0 | R/W | MII0_PHY_COL_DELAY<br>0: no delay,<br>1: collision delay 24 clocks (default)<br>It is valid only if MII0 is enabled and it works at PHY mode. | 1 |
| 31 | 5.2 | 2.4 | R/W | MII2_EN<br>1: enable, 0: disable (default) | Pin113(0) |
| 31 | 5.1 | 2.3 | R/W | Reserved | 0 |
| 31 | 5.0 | 2.2 | R/W | MII2_MAC_MOD<br>1: MII2 works in MAC mode<br>0: MII2 works in PHY mode (default) | Pin111(0) |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 6[15] | -- | RO | MII1 flow control ability<br>1: enable, 0: disable | |
| 31 | 6[14] | -- | RO | MII0 flow control ability<br>1: enable, 0: disable | |
| 31 | 6.1 | 9.1 | R/W | MDIX_FORCE<br>1: enable (default),<br>0: disable | 1 |
| 31 | 6.0 | 9.0 | R/W | EN_AUTOMDIX<br>1: enable auto mdi/mdix function (default),<br>It is valid only if MII 31.6.1 mdix_force is equal to 1 or Nway is enabled.<br>0: disable auto mdi/mdix function | * |
| | | | | Default value | |
| | | | | TEST2=0 / TEST2=1 | |
| | | | | 1 / Pin57 MDI_MDIX (0) | |

# 3 Electrical Characteristics

## 3.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

| | |
|---|---|
| Supply Voltage | –0.3V to 4.0V |
| Input Voltage | –0.3V to 5.0V |
| Output Voltage | –0.3V to 5.0V |
| Storage Temperature | -65°C to 150°C |
| Ambient Operating Temperature (Ta) | 0°C to 70°C |

## 3.2 DC Characteristic

**Operating Conditions**

| Parameter | Sym. | Min. | Typ. | Max. | | Conditions |
|---|---|---|---|---|---|---|
| Supply Voltage | VCC | 1.71 | 1.8 | 1.89 | V | |
| Supply Voltage | VCC_O | 3.135 | 3.3 | 3.465 | V | |
| Regout Voltage | REG_OUT | 1.71 | 1.82 | 1.91 | V | The linear regulator generates a 1.82v (± 6% )voltage source. |
| Power Consumption | | | 1 | | W | VCC=1.8v |



**Input Clock**



| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Frequency | | | 25 | | MHz | |
| Frequency Tolerance | | -50 | | +50 | PPM | |

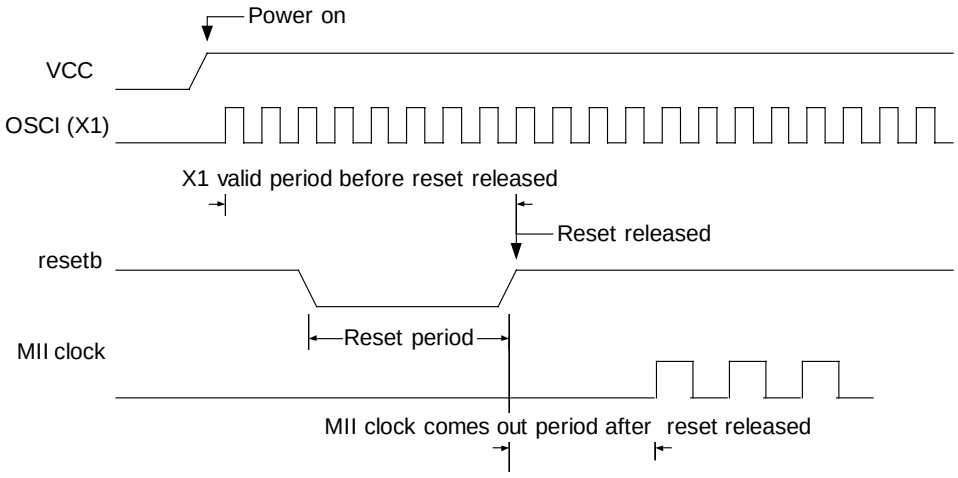
**I/O Electrical Characteristics**

| Parameter | Sym. | Min. | Typ. | Max. | | Conditions |
|---|---|---|---|---|---|---|
| Input Low Voltage | VIL | | | 0.8 | V | When VCC_IO = 3.3v |
| Input High Voltage | VIH | 2.1 | | | V | When VCC_IO = 3.3v |
| Input Low Voltage | VIL | | | 0.7 | V | When VCC_IO = 1.95v |
| Input High Voltage | VIH | 1.4 | | | V | When VCC_IO = 1.95v |
| Output Low Voltage | VOL | | | 0.4 | V | IOH=4mA, VCC_O_x=3.3V |
| Output High Voltage | VOH | 2.4 | | | V | IOL=4mA, VCC_O_x=3.3V |

## 3.3 AC Timing

### 3.3.1 Reset Timing

| Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| X1 valid period before reset released | 10 | - | - | ms |
| Reset period | 10 | - | - | ms |
| MII clock comes out period after reset released | - | 1 | - | µs |

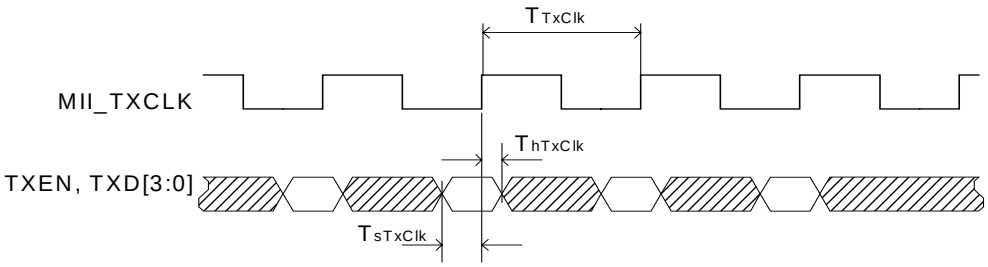





### 3.3.2 PHY Mode MII Timing

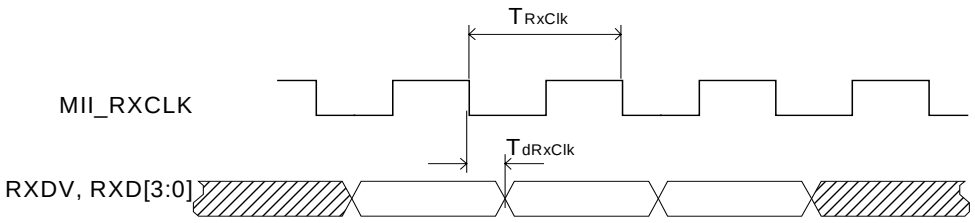
#### a. Transmit Timing Requirements

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{TxClk}$ | Transmit clock period 100M MII | - | 40 | - | ns |
| $T_{TxClk}$ | Transmit clock period 10M MII | - | 400 | - | ns |
| $T_{sTxClk}$ | TXEN, TXD to MII_TXCLK setup time | 2 | - | - | ns |
| $T_{hTxClk}$ | TXEN, TXD to MII_TXCLK hold time | 0.5 | - | - | ns |



### b. Receive Timing

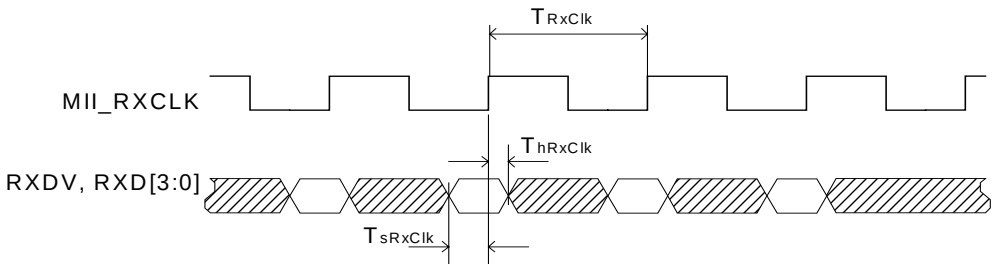
| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{RxClk}$ | Receive clock period 100M MII | - | 40 | - | ns |
| $T_{RxClk}$ | Receive clock period 10M MII | - | 400 | - | ns |
| $T_{dRxClk}$ | MII_RXCLK falling edge to RXDV, RXD | 1 | - | 4 | ns |



### 3.3.3 MAC Mode MII Timing

#### a. Receive Timing Requirements

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{RxClk}$ | Receive clock period 100M MII | - | 40 | - | ns |
| $T_{RxClk}$ | Receive clock period 10M MII | - | 400 | - | ns |
| $T_{sRxClk}$ | RXDV, RXD to MII_RXCLK setup time | 2 | - | - | ns |
| $T_{hRxClk}$ | RXDV, RXD to MII_RXCLK hold time | 0.5 | - | - | ns |

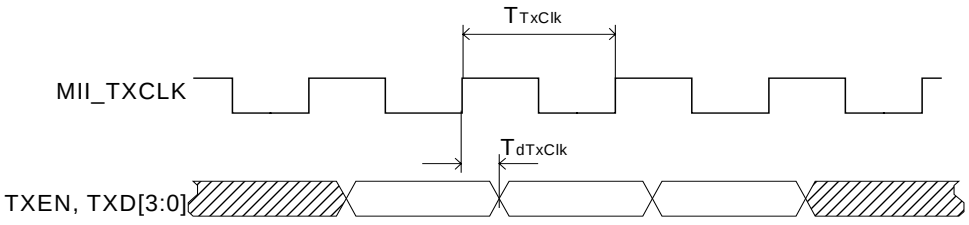





#### b. Transmit Timing



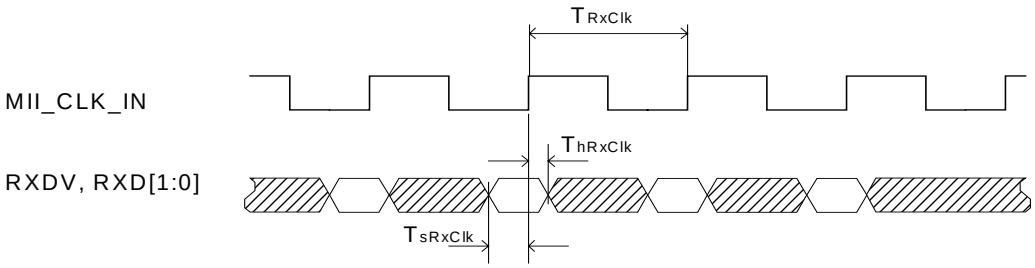
| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{TxClk}$ | Transmit clock period 100M MII | - | 40 | - | ns |
| $T_{TxClk}$ | Transmit clock period 10M MII | - | 400 | - | ns |
| $T_{dTxClk}$ | MII_TXCLK rising edge to TXEN, TXD | 1 | - | 4 | ns |



### 3.3.4 RMII Timing

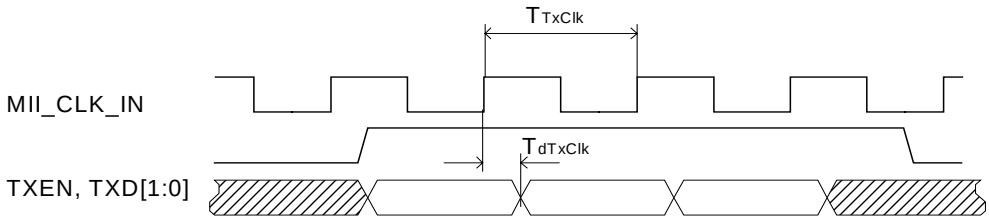
#### a. Receive Timing Requirements

| Symbol | Description | Min. | | Max. | Unit |
|---|---|---|---|---|---|
| $T_{RxClk}$ | Receive clock period | - | 20 | - | ns |
| $T_{sRxClk}$ | RXDV, RXD to MII_CLK_IN setup time | 2 | - | - | ns |
| $T_{hRxClk}$ | RXDV, RXD to MII_CLK_IN hold time | 0.5 | - | - | ns |




#### b. Transmit Timing

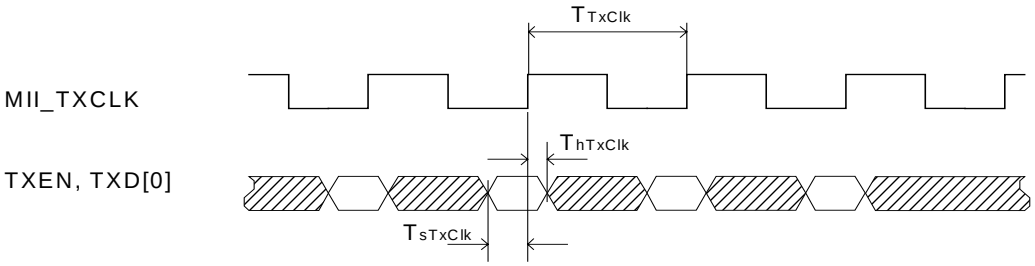
| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{TxClk}$ | Transmit clock period | - | 20 | - | ns |
| $T_{dTxClk}$ | MII_CLK_IN rising edge to TXEN, TXD | 1 | - | 4 | ns |



### 3.3.5 SNI Timing

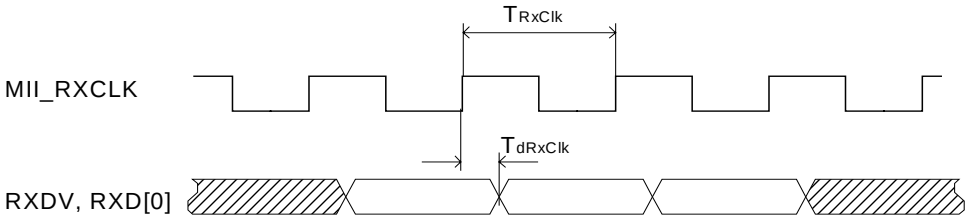
#### a. Transmit Timing Requirements

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{TxClk}$ | Transmit clock period | - | 100 | - | ns |
| $T_{sTxClk}$ | TXEN, TXD to MII_TXCLK setup time | 2 | - | - | ns |
| $T_{hTxClk}$ | TXEN, TXD to MII_TXCLK hold time | 0.5 | - | - | ns |




#### b. Receive Timing

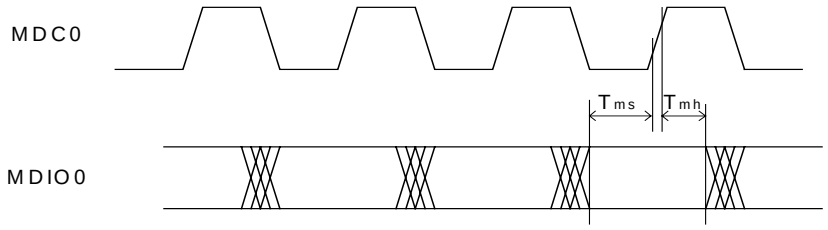
| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{RxClk}$ | Receive clock period | - | 100 | - | ns |
| $T_{dRxClk}$ | MII_RXCLK rising edge to RXDV, RXD | 1 | - | 4 | ns |



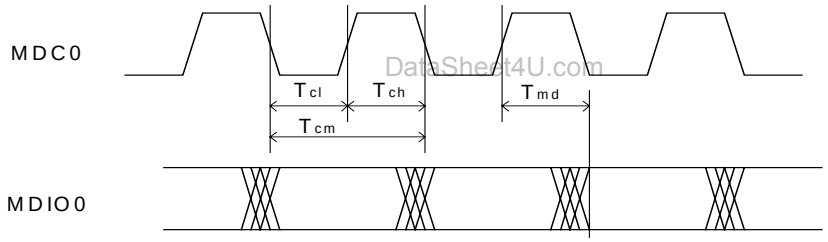
### 3.3.6 SMI Timing

#### a. MDC0/MDIO0 Timing

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{ch}$ | MDC0 High Time | 40 | - | - | ns |
| $T_{cl}$ | MDC0 Low Time | 40 | - | - | ns |
| $T_{cm}$ | MDC0 period | 80 | - | - | ns |
| $T_{md}$ | MDIO0 output delay | - | - | 5 | ns |
| $T_{mh}$ | MDIO0 setup time | 10 | - | - | ns |
| $T_{ms}$ | MDIO0 hold time | 10 | - | - | ns |



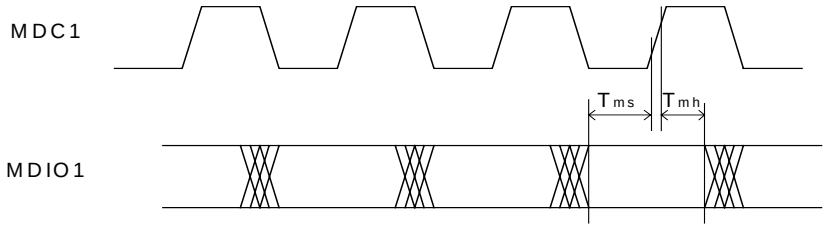

**Write Cycle**



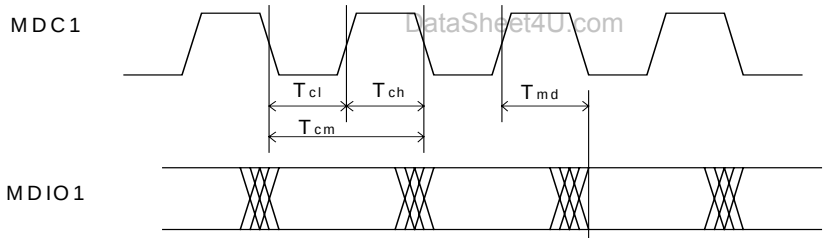

**Read Cycle**

### b. MDC1/ MDIO1 Timing

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{ch}$ | MDC1 High Time | 40 | - | - | ns |
| $T_{cl}$ | MDC1 Low Time | 40 | - | - | ns |
| $T_{cm}$ | MDC1 period | 80 | - | - | ns |
| $T_{md}$ | MDIO1 output delay | - | - | 5 | ns |
| $T_{ms}$ | MDIO1 setup time | 10 | - | - | ns |
| $T_{mh}$ | MDIO1 hold time | 10 | - | - | ns |




**Write Cycle**

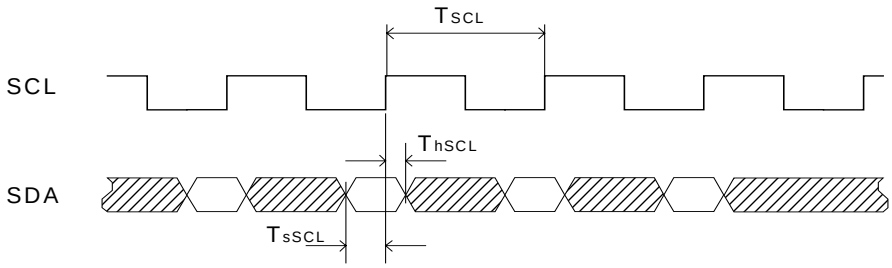



**Read Cycle**

### 3.3.7 EEPROM Timing

**a.**

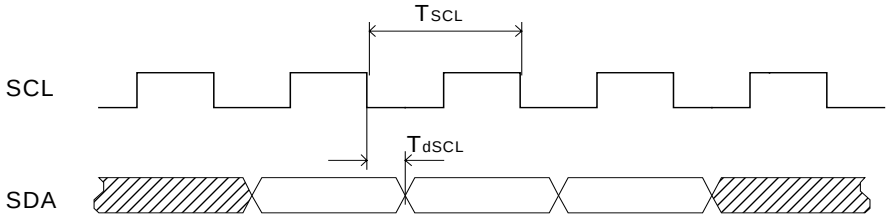
| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{SCL}$ | Receive clock period | - | 20480 | - | ns |
| $T_{sSCL}$ | SDA to SCL setup time | 2 | - | - | ns |
| $T_{hSCL}$ | SDA to SCL hold time | 0.5 | - | - | ns |




Read data cycle

**b.**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{SCL}$ | Transmit clock period | - | 20480 | - | ns |
| $T_{dSCL}$ | SCL falling edge to SDA | - | - | 5200 | ns |




Comand cycle

## 3.4 Thermal Data

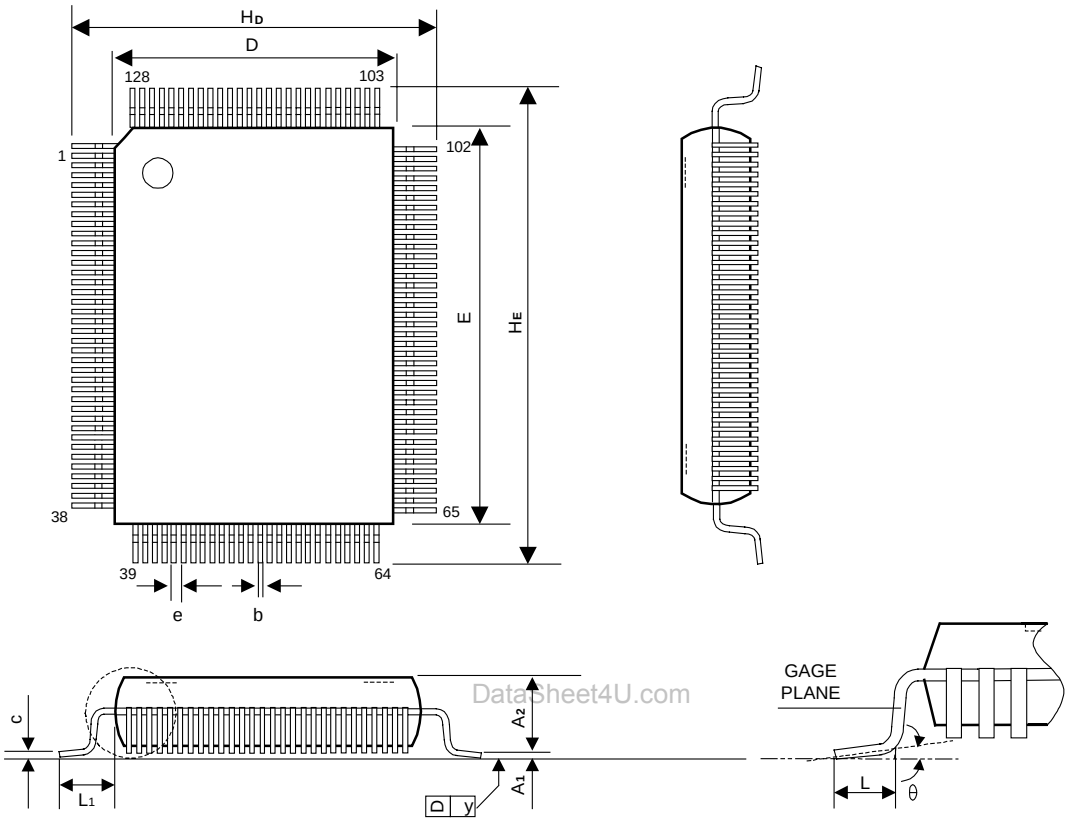
| Theta Ja | Theta Jc | Conditions | Units |
|---|---|---|---|
| 38.2 | -- | 2 Layer PCB | $^{o}$C/W |

# 4 Order Information

| Part No. | Package | Notice |
|---|---|---|
| IP175B | 128-PIN PQFP | - |

# 5 Package Detail

## 128 PQFP Outline Dimensions




| Symbol | Dimensions In Inches | | | Dimensions In mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A1 | 0.010 | 0.014 | 0.018 | 0.25 | 0.35 | 0.45 |
| A2 | 0.107 | 0.112 | 0.117 | 2.73 | 2.85 | 2.97 |
| b | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| c | 0.004 | 0.006 | 0.008 | 0.09 | 0.15 | 0.20 |
| HD | 0.669 | 0.677 | 0.685 | 17.00 | 17.20 | 17.40 |
| D | 0.547 | 0.551 | 0.555 | 13.90 | 14.00 | 14.10 |
| HE | 0.906 | 0.913 | 0.921 | 23.00 | 23.20 | 23.40 |
| E | 0.783 | 0.787 | 0.791 | 19.90 | 20.00 | 20.10 |
| e | - | 0.020 | - | - | 0.50 | - |
| L | 0.025 | 0.035 | 0.041 | 0.65 | 0.88 | 1.03 |
| L1 | - | 0.063 | - | - | 1.60 | - |
| y | - | - | 0.004 | - | - | 0.10 |
| θ | 0° | - | 12° | 0° | - | 12° |

Note:
1. Dimension D & E do not include mold protrusion.
2. Dimension B does not include dambar protrusion. Total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

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