



8 Port 10/100 Ethernet Integrated Switch

(Port Mirror, TCP/UDP QoS & VIP Port QoS)

Features

- Wide operating temperature range
 - IP178D LF (0°C to 70°C)
 - IP178D LFI (-40°C to 85°C)
- IP178C pin to pin compatible
- Support 2k MAC address
- Support auto-polarity for 10 Mbps
- Support filter/forward special DA option
- Support broadcast storm protection
- Auto MDI-MDIX option
- Two queues per port for QoS purposes
- Support Port based QoS
- Support 802.1p & DiffServ based QoS
- QoS
 - Port base
 - 802.1p
 - IP DiffServ IPV4/IPV6
 - TCP/UDP port number
 - Pins configure ports priority (VIP port)
- Support max forwarding packet length 1552/1536 bytes option
- Support port mirror function
- Support two dynamic fiber ports for Hot Plug
- Built in linear regulator control circuit
- Support Lead Free package (Please refer to the Order Information)
- 0.16um Process

General Description

IP178D integrates an 8-port switch controller, SSRAM, and 8 10/100 Ethernet transceivers. Each of the transceivers complies with the IEEE 802.3, IEEE 802.3u, and IEEE 802.3x specifications. The transceivers are designed in DSP approach in 0.16um technology; they have high noise immunity and robust performance.

IP178D supports a lot of QoS function, including 802.1p, DiffServ, TCP/UDP port number and High priority port. User could enable QoS function from Pin or EEPROM.

IP178D also supports port mirror function for each port. User could monitor RX and TX port.

There are two fiber ports, port 6 and port 7, could be enable and disable from pin.

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Revision History

Revision #	Change Description
IP178D-DS-R01	Initial release



The difference in pin definition between IP178C/IP178CH and IP178D

Pin	IP178C/IP178CH			IP178D		
	Function	Configure	Type	Function	Configure	Type
36	NC(IP178C) FXSD6(IP178CH)			FXSD6		
53	TEST1	EXTMII_EN	IPL	TEST1	HIGH_PRI[2]	IPL
56	RXCLK		IPH	TEST2		IPH
57	GND(IP178C) FXSD7(IP178CH)			FXSD7		
72	SPEED_LED1	RMII_MII	IPL	SPEED_LED1	REDUCE_IPG_DIS	IPL
73	SPEED_LED0	SCA_SEL	IPL	SPEED_LED0	PS_MODE_0_100	IPL
75	RXDV/FDX_LED7	X_EN	IPH	FDX_LED7	X_EN	IPH
76	RXD3/FDX_LED6	AGING	IPH	FDX_LED6	AGING	IPH
77	RXD2/FDX_LED5	BCSTF	IPL	FDX_LED5	BCSTF	IPL
78	RXD1/FDX_LED4	FILTER_DA	IPL	FDX_LED4	FILTER_DA	IPL
79	RXD0/FDX_LED3	VLAN_ON	IPL	FDX_LED3	HIGH_PRI[1]	IPL
80	TXEN	LED_SEL[1]	IPH		LED_SEL[1]	IPH
81	TXD3	LED_SEL[0]	IPH		LED_SEL[0]	IPH
84	LOW_10M_DIS/ SCA_DIS		IPH	LOW_10M_DIS		IPH
85	TXD2/FDX_LED2	FX7_EN (for IP178CH only)	IPL	FDX_LED2	LPP_AGING_EN (Note1)	IPL
86	TXD1/FDX_LED1	FX7_HALF (for IP178CH only)	IPL	FDX_LED1	FX_HALF7	IPL
87	TXD0/FDX_LED0	APS_DIS	IPL	FDX_LED0	APS_DIS	IPL
96	LINK_LED3	FX6_HALF (for IP178CH only)	IPL	LINK_LED3	FX_HALF6	IPL
97	LINK_LED2	FX6_EN (for IP178CH only)	IPL	LINK_LED2	PORT_MIRROR0_7 (Note1)	IPL
100	LINK_LED0	P6_7_HIGH	IPL	LINK_LED0	HIGH_PRI[0]	IPL
101	TXCLK	LONG_PKT_DIS	IPH		LONG_PKT_DIS	IPH
104	SCL	MII_MAC	IPL	SCL		IPL

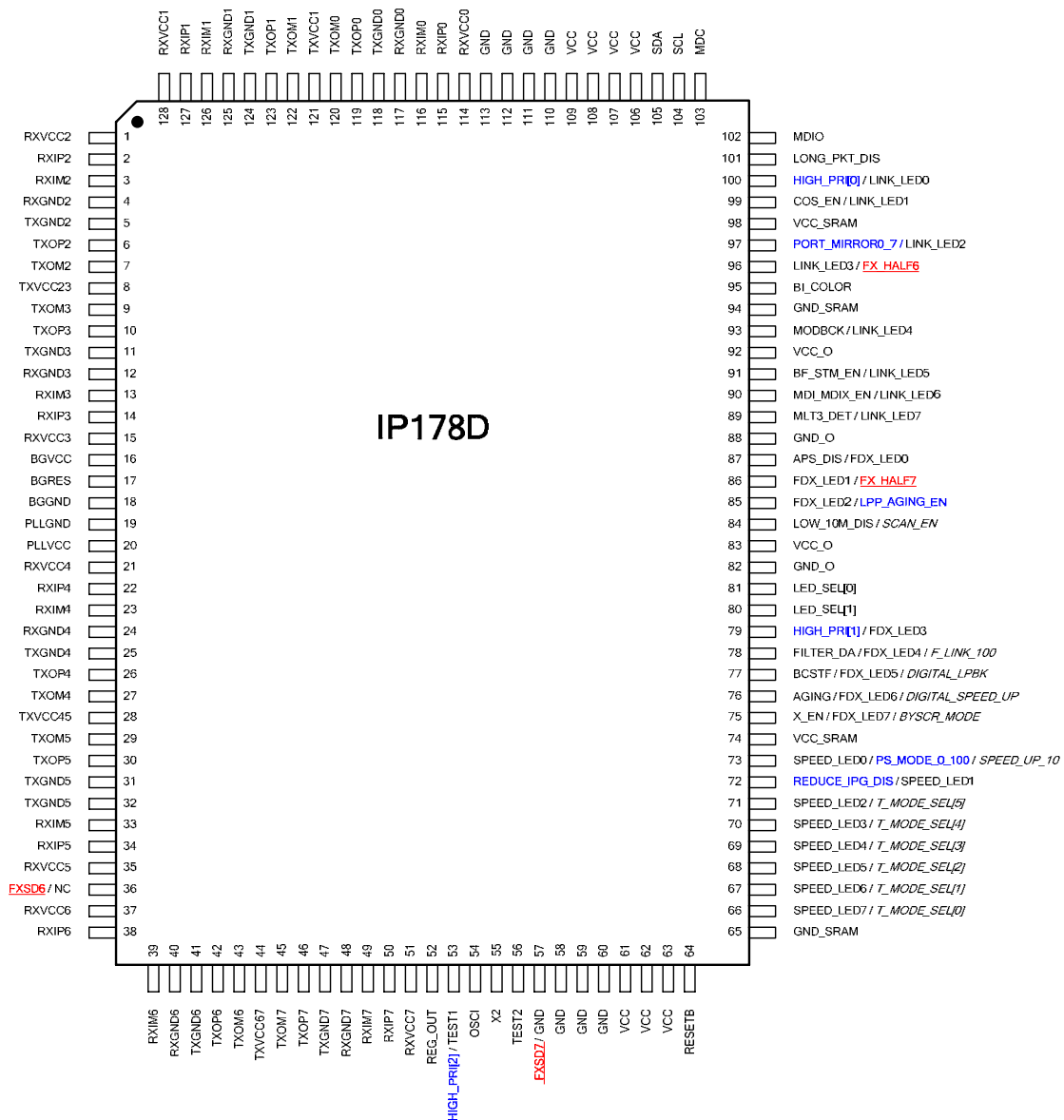
Note1: FXx_EN not require in IP178D fiber design. Please check chapter **4.6 Fiber port configuration**



Features comparison between IP178C and IP178D

Function	IP178C	IP178D
Process	0.18 um	0.16 um
Switch structure	8 TP + 1* MII (MII related pins: 53, 72 & 104)	8 TP
Port based priority	Yes	Yes
802.1p priority	Yes	Yes
Support Fiber function	X	2 ports with FXSD
VLAN	Port base and Tag base VLAN	No
IP DiffServ Priority	Yes	Yes
SCA (Smart Cable Analysis)	Yes	No
Port mirroring	No	Yes
Pins configure for port-priority	No	Yes
Reduce IPG function	No	Yes
TCP/UDP port number priority	No	Yes
Fiber support	No	Yes

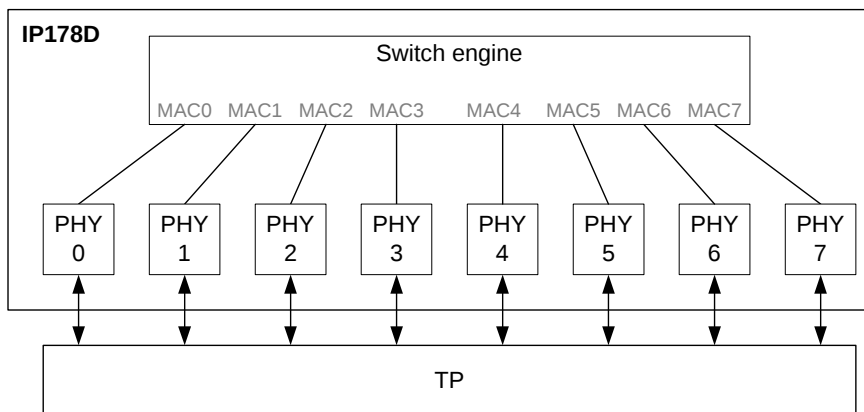
1 Pin diagram



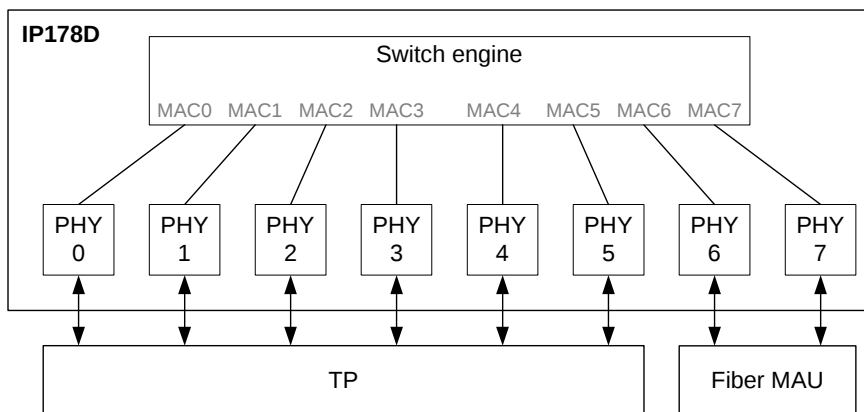
2 IP178D application diagram

2.1 An 8 TP port switch application

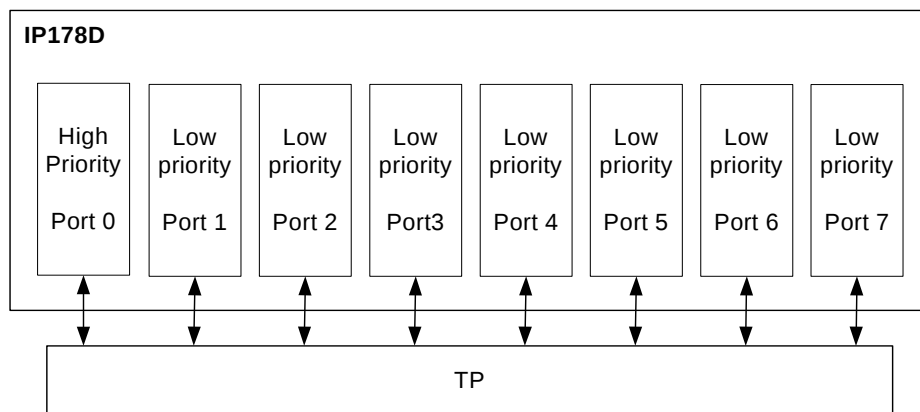
Here shows the application diagram of 8-port switch.



2.2 An 8-port switch mixed with two fiber ports

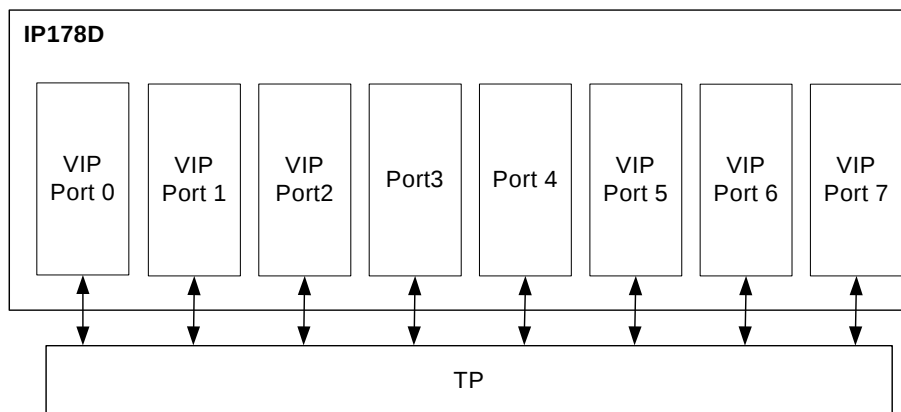


2.3 TCP/UDP QoS Switch for time-sensitive application from pin setting



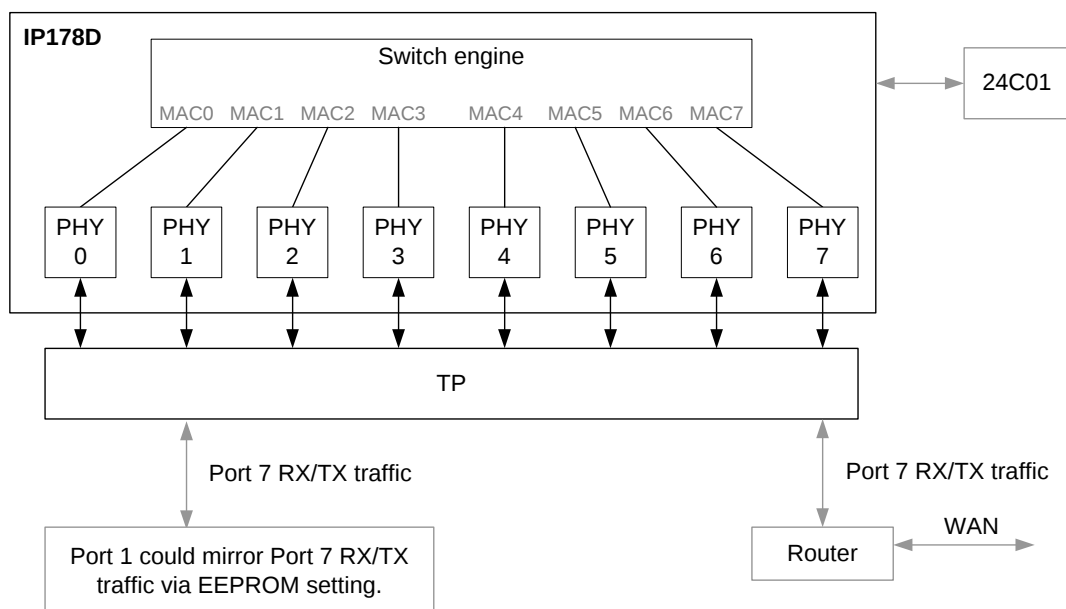
Port 0 received packet with reserved TCP/UDP port number, port 0 will enable its ingress port as a high priority port for 300 seconds.
If the other ports received packets with the same reserved port number, it also has the same behavior as port 0.

2.4 Switch with VIP ports for specific users from Pin setting



Pin 53 , 79, 100	High Priority Port (VIP port)
0,0,1	6, 7
0,1,0	5,6,7
0,1,1	7
1,0,1	0,1
1,1,0	0,1,2
1,1,1	0

2.5 A 8-port Switch with Port mirror capability setting from EEPROM



3 Pin description

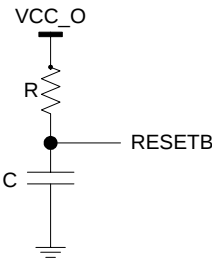
Type	Description
I	Input pin
O	Output pin
IPL	Input pin with internal pull low
IPH	Input pin with internal pull high

Type	Description
IPL1	Input pin with internal pull low 22.8k ohm
IPH1	Input pin with internal pull high 22.8k ohm
IPL2	Input pin with internal pull low 92.6k ohm
IPH2	Input pin with internal pull high 113.8k ohm

3.1 Analog pins

Pin No.	Label	Type	Description
52	REG_OUT	O	Regulator output voltage The internal regulator uses pin 83 / pin 92 VCC_O as reference voltage to control external transistor to generate a voltage source between 1.80v ~ 2.05v.
17	BGRES	I	Band gap resister It is connected to GND through a 6.19k (1%) resistor in application circuit.
115, 116, 127, 126, 2, 3, 14, 13, 22, 23, 34, 33, 38, 39, 50, 49	RXIP0~7 RXIM0~7	I	TP receive
119, 120, 123, 122, 6, 7, 10, 9, 26, 27, 30, 29, 42, 43, 46, 45	TXOP0~7 TXOM0~7	O	TP transmit
96	FX_HALF6	IPL1, O	Port 6 fiber port half duplex setting pin 1: port 6 is half duplex in fiber mode 0: port 6 is full duplex in fiber mode
86	FX_HALF7	IPL1, O	Port 7 fiber port half duplex setting pin 1: port 7 is half duplex in fiber mode 0: port 7 is full duplex in fiber mode
36	FXSD6	I	Fiber signal detection of port 6 This pin is a direct input pin for fiber signal detection
57	FXSD7	I	Fiber signal detection of port 7 This pin is a direct input pin for fiber signal detection

3.2 System clock & reset pins

Pin No.	Label	Type	Description
54	OSCI	I	25MHz system clock It is recommended to connect OSCI and X2 to a 25MHz crystal. If the clock source is from another chip or oscillator, the clock should be active at least for 1ms before pin 64 RESETB de-asserted. Pin 55 X2 should be left open in this application.
55	X2	O	Crystal pin A 25Mhz crystal can be connected to OSCI and X2.
64	RESETB	I	Reset It is a low active input pad with Schmitt trigger. The reset time must be hold for more than 1 ms. If an R/C reset circuit is used, the capacitor should be connected to VCC_O as shown in the figure. 



3.3 EEPROM interface

Pin No.	Label	Type	Description
105	SDA	IPH2, O	EEPROM serial address/data I/O After reset, it is used as data pin SDA of EEPROM. After reading EEPROM, this pin becomes an input pin.
104	SCL	IPL2, O	EEPROM serial clock input After reset, it is used as clock pin SCL of EEPROM. After reading EEPROM, this pin becomes an input pin. Its period is longer than 10us. IP178D stops reading the rest data in EEPROM if the first two bytes in EEPROM aren't 55AA.

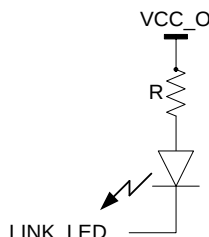
3.4 Serial Management Interface

	Label	Type	Description
103	MDC	IPL2	SMI management data clock Sourced continuously from the external device that needs to access the internal registers of IP178D. The external device uses SMI interface to access the internal registers of IP178D. IP178D doesn't access the MII registers of external PHY.
102	MDIO	IPH2 ,O	SMI management data input/output A bi-directional multi-drop bus for accessing the internal registers.

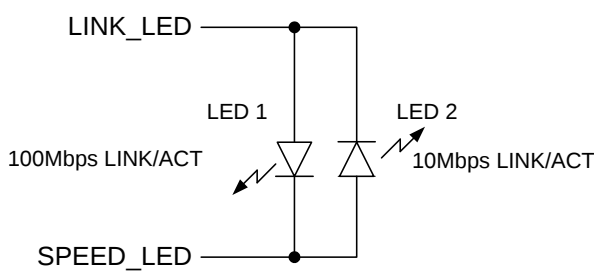
3.5 Boundry scan & test mode

Pin No.	Label	Type	Description
103	SCAN_CLK	IPL2	Boundry scan clock input
84	SCAN_EN	IPH2	Boundry scan enable To enter the scan mode, pin 53 and 56 should be pulled low at the same time with SCAN_EN is enabled.
71	T_MODE_SEL[5]	IPL1, O	Test mode pin 5 This pin is a speed LED of port 2 after reset.
70	T_MODE_SEL[4]	IPL1, O	Test mode pin 4 This pin is a speed LED of port 3 after reset.
69	T_MODE_SEL[3]	IPL1, O	Test mode pin 3 This pin is a speed LED of port 4 after reset.
68	T_MODE_SEL[2]	IPL1, O	Test mode pin 2 This pin is a speed LED of port after reset.
67	T_MODE_SEL[1]	IPL1, O	Test mode pin 1 This pin is a speed LED of port 6 after reset.
66	T_MODE_SEL[0]	IPL1, O	Test mode pin 0 This pin is a speed LED of port 7 after reset.

3.6 LED interface (I)

Pin no.	Label	Type	Description	
89, 90, 91, 93, 96, 97, 99, 100	LINK_LED[7:0]	O	LINK LED The detail functions are illustrated in the following table. It should be connected to VCC_O through a LED and a resistor. Application circuit 	
66, 67, 68, 69, 70, 71, 72, 73	SPEED_LED[7:0]	O	SPEED LED The detail functions are illustrated in the following table. It should be connected to VCC_O through a LED and a resistor.	
75, 76, 77, 78, 79, 85, 86, 87	FDX_LED[7:0]	O	FDX LED The detail functions are illustrated in the following table. It should be connected to VCC_O through a LED and a resistor.	
80, 81	LED_SEL[1:0]	IPH2	LED function selection The data on these pins are latched at the end of reset to select LED modes. The default value is mode 3. The detail functions are illustrated in the following table.	
LED_SEL[1:0]	LED mode	LINK_LED[7:0]	SPEED_LED[7:0]	FDX_LED[7:0]
00	Mode 0	Off: link fail On: 10 Mbps link ok Flash: TX/RX	Off: link fail On: 100 Mbps link ok Flash: TX/RX	Off: half duplex On: full duplex
01	Mode 1	Off: link fail On: link ok Flash: RX	Off: 10 Mbps On: 100 Mbps	Off: half duplex On: full duplex Flash: collision
10	Mode 2	Off: link fail On: 10 Mbps link ok Flash: TX/RX	Off: link fail On: 100 Mbps link ok Flash: TX/RX	Off: half duplex On: full duplex Flash: collision
11 (default)	Mode 3	Off: link fail On: link ok Flash: TX/RX	Off: 10 Mbps On: 100 Mbps	Off: half duplex On: full duplex Flash: collision

3.7 LED interface (II)

Pin no.	Label	Type	Description	
95	BI_COLOR	IPL2	Bi-color LED mode enable 1: Bi-color mode LED enabled. LED_LINK[7:0] and LED_SPEED[7:0] are used to drive dual color LED. The functions are defined in the following table. The behavior of FDX_LED[7:0] is the same as that in mode3 on the previous page. 0: Bi-color mode LED disabled.(default) Please refer to pin description of LED_SEL[1:0] for LED functions. This pin takes precedence of LED_SEL[1:0]. Application circuit 	
Bi-color LED definition				
Status	LINK_LED[7:0]	SPEED_LED[7:0]	LED 1	LED 2
Link off	1	1	Off	Off
100 Mbps link ok	1	0	On	Off
100 Mbps link ok/ activity	1	Clock	Flash	Off
10 Mbps link ok	0	1	Off	On
10 Mbps link ok/ activity	Clock	1	Off	Flash

3.8 Frame priority setting pins

Pin no.	Label	Type	Description
100	HIGH_PRI[0]	IPL1, O	Port based priority setting, bit 0 1: enable 0: disabled (default) It is an input signal during reset and its value is latched at the end of reset. It acts as a link LED of port 0 after reset. VIP port setting as follow, pin 53, 79, 100



3.9 Miscellaneous setting pins (I)

Pin no.	Label	Type	Description
101	LONG_PKT_DIS	IPH2	Max packet size option 1: Drop packets with length longer than 1536 bytes (default) 0: Drop packets with length longer than 1552 bytes
97	PORT_MIRROR_0_7	IPL1, O	Mirror port 0 traffic to port 7 When enabled, the traffic (RX path) to port 0 will mirror to port 7. 1: mirror port 0 RX traffic to port 7 0: disable mirror function (default) This pin is a link LED of port 2 after reset.
93	MODBCK	IPH1, O	Aggressive back off enable IP178D adopts modified (aggressive) back off algorithm if this function is enabled. The maximum back off period is limited to 8-slot time. It makes IP178D have higher transmission priority in a collision event. 1: aggressive mode enable (default), 0: standard back off This pin is a link LED of port 4 after reset.
91	BF_STM_EN	IPL1, O	Broadcast storm enable 1: enable 0: disable (default) A port begins to drop packets if it receives broadcast packets more than the threshold defined in MII register 31.9[15:14] BQ_STM_THR_SEL [1:0] or EEPROM register 83[7:6]. This pin is a link LED of port 5 after reset.
90	MDI_MDIX_EN	IPH1, O	MDI/MDI-X enable MDI/MDI-X auto cross over 1: enable (default) 0: disable It is an input signal during reset and its value is latched at the end of reset to set auto MDI/MDIX function. This pin is a link LED of port 6 after reset.
89	MLT3_DET	IPL1, O	Ability for detecting MLT3 (for 10 Mbps switch to 100 Mbps) 1: enable MLT3 detection ability 0: disable MLT3 detection ability (default) MLT3_DET is link LED of port 7 after reset.

3.10 Miscellaneous setting pins (II)

Pin no.	Label	Type	Description
87	APS_DIS	IPL1, O	Disable advance power saving mode 1: disable advance power saving mode 0: enable advance power saving mode (default) APS_DIS is full duplex LED of port 0 after reset.
84	LOW_10M_DIS	IPH2	LOW_10M_DIS 1: disable power saving mode. (default) 0: enable power saving mode
79	PORT_MIRROR0_7	IPL1, O	Mirror port 0 traffic to port 7 Mirror the ingress and egress traffic to port 7. To reduce the traffic congestion at port 7, do not use it as a normal operation port. 1: enable 0: disable (default) This pin is a duplex LED of port 3 after reset.
78	FILTER_DA	IPL1, O	Reserved address forward option Filter packets with specific DA (Destination Address) from 01:80:C2:00:00:02 to 01:80:C2:00:00:0F. Packets with specific DA equal to 01:80:C2:00:00:01 are always filtered regardless the setting of this pin. 1: filter 0: forward (default) This pin is a duplex LED of port 4 after reset.
77	BCSTF	IPL1, O	Broadcast frame option 1: Packets with DA equal to FF:FF:FF:FF:FF:FF are handled as broadcast frame in broadcast protection function, 0: Packets with DA equal to FF:FF:FF:FF:FF:FF or multi-cast frames are handled as broadcast frame in broadcast protection function. This pin is a duplex LED of port 5 after reset.
76	AGING	IPH1, O	Aging enable 1: enable 300s aging timer (default) 0: disable aging function This pin is a duplex LED of port 6 after reset.

3.11 Miscellaneous setting pins (III)

Pin no.	Label	Type	Description
75	X_EN	IPH1, O	Flow control enable 1: enable IEEE802.3x & back pressure (default) 0: disable IEEE802.3x & back pressure The function is valid only if pin 53 is pulled low. This pin is a duplex LED of port 7 after reset.
73	PS_MODE_0_100	IPL1, O	Power saving mode 1: power saving mode for 0 to 100 mA 0: power saving mode for 40 to 100 mA (default) This pin is a speed LED of port 0 after reset.
72	REDUCE_IPG_DIS	IPL1, O	Reduce IPG function This function reduce the IPG by random from 0 ~ 20 PPM. 1: disable reduce IPG function 0: enable reduce IPG function This pin is a speed LED of port 1 after reset.

3.12 Power & ground pins

Pin no.	Label	Type	Description
16	BGVCC	I	Power of band gap circuit
18	BGGND	I	Power of band gap circuit
19	PLLGND	I	Ground of PLL circuit
20	PLLVCC	I	Power of PLL circuit
58, 59, 60, 110, 111, 112, 113	GND	I	Ground of internal logic
61, 62, 63, 106, 107, 108, 109,	VCC	I	Power of internal logic
65, 94,	GND_SRAM	I	Ground of internal SRAM
74, 98,	VCC_SRAM	I	Power of internal SRAM
82, 88,	GND_O	I	Ground for LED and EEPROM
83, 92,	VCC_O	I	Power for LED and EEPROM (3.3V or 2.5V)
114, 128, 1, 15, 21, 35, 37, 51	RXVCC0~7	I	Power of analog receive block
117, 125, 4, 12, 24, 32, 40, 48,	RXGND0~7	I	Ground of analog receive block
118, 124, 5, 11, 25, 31, 41, 47,	TXGND0~7	I	Ground of analog transmit buffer
121, 8, 28, 44,	TXVCC01 TXVCC23 TXVCC45 TXVCC67	I	Power of analog transmit buffer

4 Functional Description

4.1 LED display (normal operation)

Normal operation			
LED_O_SEL[1:0]	LINK_LED	SPEED_LED	FDX_LED
00	Off: link fail On: 10 Mbps link ok Flash: TX/RX	Off: link fail On: 100 Mbps link ok Flash: TX/RX	Off: half duplex On: full duplex
01	Off: link fail On: link ok Flash: RX	Off: 10 Mbps On: 100 Mbps	Off: half duplex On: full duplex Flash: collision
10	Off: link fail On: 10 Mbps link ok Flash: TXRX	Off: link fail On: 100 Mbps link ok Flash: TX/RX	Off: half duplex On: full duplex Flash: collision
11	Off: link fail On: link ok Flash: TX/RX	Off: 10 Mbps On: 100 Mbps	Off: half duplex On: full duplex Flash: collision
Flash behavior: Off 44ms → On 176ms → Off 44ms → ...			

4.2 Flow control

IP178D jams or pauses a port, which causes output queue over the threshold. Its link partner will defer transmission after detecting the jam or pause frame. A port of IP178D defers transmission when it receives a jam or a pause frame. The source address (SA) of pause control frame will be { IP178D OUI (0090C3), port number}. For example, the SA of port 1 pause control frame will be "00 90 C3 00 00 01".

When CoS is enabled, IP178D may disable the flow control function for a short term to guarantee the bandwidth of high priority packets. A port disables its flow control function for 2 ~ 3 seconds when it receives a high priority packet. It doesn't transmit pause frame or jam pattern during the period but it still responses to pause frame or jam pattern.

The flow control function can be enabled by pulling up pin 75 X_EN or by programming MII register 30.1.10.

4.3 Broadcast storm protection

A port of IP178D begins to drops broadcast packets if the received broadcast packets are more than the threshold defined in MII register 31.9[15:14] or EEPROM register 83[7:6] BQ_STM_THR_SEL [1:0] in 10ms (100Mbps) or 100ms (10Mbps)

The function can be enabled by pulling high pin 91 BF_STM_EN or programming MII register 30.1[6].

IP178D handles multicast frame as a broadcast frame in broadcast storm protection function if pin 77 BCSTF is pulled low.

4.4 CoS

IP178D supports two types of CoS. One is port base priority function and the other is frame base priority function. IP178D supports two levels of priority queues. A high priority packet will be queued to the high priority queue to share more bandwidth. The ratio of bandwidth of high priority and low priority queue is defined in MII register 30.1[15] or EEPROM 3[7].

4.4.1 Port base priority

The packets received from high priority port will be handled as high priority frames if the port base priority is enabled. It is enabled by programming the corresponding bit in MII register 31.0[9] ~ 31.7[9] or EEPROM register 65[1] ~ 79[1]. Each port of IP178D can be configured as a high priority port individually.

4.4.2 VIP ports

This port based priority function can active either by register or pin setting. There are three pins dedicate for enabling the port based priority function. The follow illustration shows the pin setting part of the port based priority function.

pin number	53	79	100
name	HIGH_PRI[2]	HIGH_PRI[1]	HIGH_PRI[0]

HIGH[2:0]	High priority port
001	6, 7
010	5, 6, 7
011	7
101	0, 1
110	0, 1, 2
111	0
others	reserved

4.4.3 Frame base priority

4.4.3.1 VLAN tag and TCP/IP TOS

IP178D examines the specific bits of VLAN tag and TCP/IP TOS for priority frames if the frame base priority is enabled. The packets will be handled as high priority frames if the tag value meets the high priority requirement, that is, VLAN tag bigger than 3 or TCP/IP TOS field not equal to 3'b000. It is enabled by programming the corresponding bit in MII register 31.0[10]~31.7[10] or EEPROM register 65[2]~79[2]. The frame base priority function of each port can be enabled individually.

IP178D supports an easy way to enable a sub set of CoS function without programming EEPROM or MII registers. Frame base priority function of all ports is enabled if pin 99 COS_EN is pulled high. The setting in register takes precedence of the setting on pins.

VLAN field

TYPE = 8100	TCI (tag control information)
byte 12~13	14~15

TCI definition:

Bit[15:13]: User Priority 7~0
 Bit 12: Canonical Format Indicator (CFI)
 Bit[11~0]: VLAN ID.
 IP178D uses bit[15:13] to define priority.

TOS field

TYPE = 0800	IP HEADER
byte 12~13	14~15

IP header definition:

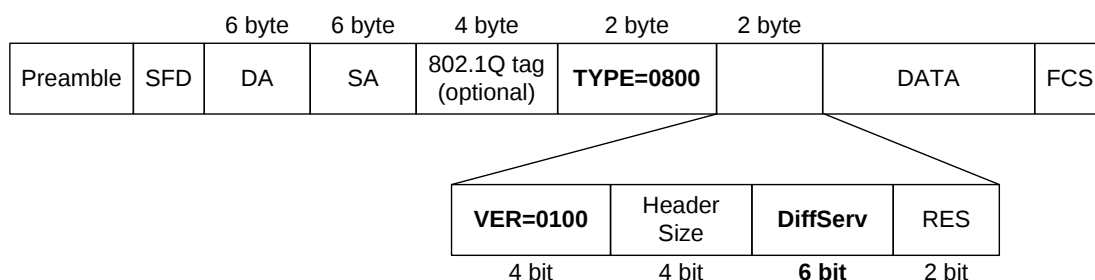
Byte 14
 Bit[7:0]: IP protocol version number & header length.
 Byte 15: Service type
 Bit[7~5]: IP Priority (Precedence) from 7~0
 Bit 4: No Delay (D)
 Bit 3: High Throughput
 Bit 2: High Reliability (R)
 Bit[1:0]: Reserved
 IP178D uses bit[7:5] to define priority.
 0~3: low priority
 4~7: high priority

4.4.3.2 IPv4/IPv6 DiffServ

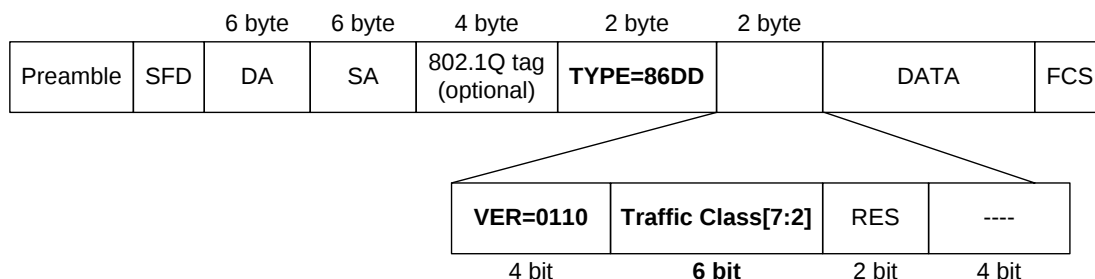
IP178D checks the DiffServ field of a IPv4 frame or Traffic class field [7:2] (TC[7:2]) of a IPv6 frame and uses them to decide the frame's priority if MII register 31.30.[13] DIFFSERV_EN is enabled. IP178D uses DiffServ or TC[7:2] as index to select one of 64 bits. If the bit is "1", the received frame is handled as a high priority frame. IP178D recognize the following DSCP (Differentiated Service Code Point) Octet as high priority frame.

6'b101110
6'b001010
6'b010010
6'b011010
6'b100010
6'b11x000

IPv4 frame format



IPv6 frame format



4.4.3.3 TCP/UDP logical port priority

IP178D can configure the ingress port frame priority by using the TCP/UDP frame logical port number. When the incoming IP packet with TCP or UDP protocols, the 16 bits destination or source port field in the TCP/UDP header can be used for assign the frame priority. It means the source's logical port or the destination's logical port in the incoming packet match any of the pre-defined logical ports, the incoming frame will give a high priority mark and put it in the high priority queue.

TCP/UDP logical port priority function of all ports is enabled if pin 99 COS_EN is pulled high. The logical port priority of each pre-defined port number or user defined range of logical port number can be enabled individually by programming the corresponding bit in the MII register 30.14[5:0] or EEPROM register 10[5:0].

■ Pre-defined logical ports list

Service	TCP	Description
SSH	22	secure shell
HTTPs	443	secure HTTP (SSL)
RDP	3389	Windows Remote Desktop Protocol
XWIN	6000	X11 – used for X-Windows

These pre-defined logical ports can be enable individually by programming MII register 30.14[3:0] or EEPROM register 10[3:0].

■ User defined range logical ports list (defaulting setting)

Service	TCP	Description
telnet	23	Remote terminal protocol
VNC	5800	VNC remote desktop protocol

For the user defined range logical ports, it contains two set of range and can be changed by programming via MII register or EEPROM register. Each range consists of a high and low limit register to set the TCP or UDP logical port range. The high limit port number can not large than the low limit port number. The default logical port number of range 0 and 1 are default set to 23 and 5800, for this case the high and low limit port number is the same value. If an incoming IP frame with TCP/UDP port number is between the low and high limit, it will be treated as a high priority frame.

4.5 Port Mirroring

There are some circumstances that the network administrator requires to monitor the network status. The port mirroring function can help the network administrator diagnose the network.

A port mirroring function can be accomplished by assigning a monitored port and a snooping port. The IP178D supports four kinds of monitoring methods: source port, destination port, one port of source and destination, source-destination pair. This function can be enabled by programming the corresponding bit in MII registers 30.3~30.4.

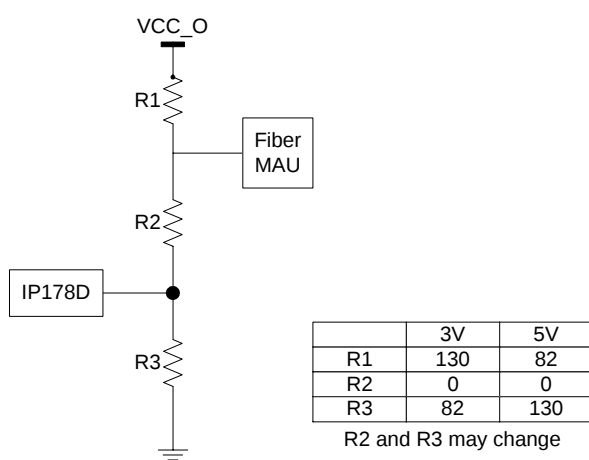
4.6 Buffer Aging

When buffer aging was enabled, a frame stayed in output port for transmission is discarded if buffer aging time has exceeded one second. The buffer aging time is the maximum delay time for transmission on output port. This function can be set from MII register 30.13.13.

4.7 Fiber port configuration

Port 6 and 7 of IP178D can be configured to be a fiber port or a TP port individually. A port becomes a fiber port if its FXSDx is connected to a fiber MAU or pulled to high. A port becomes a TP port if it's FXSDx is pulled low.

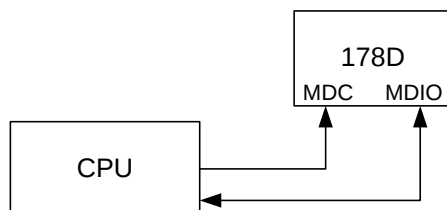
Voltage on FXSDx	TP port	Fiber port	Fiber signal detect	Condition
< 0.6 V	Yes	--	--	
> 0.6 V < 1.2 V	--	Yes	Off	Fiber unplugged
> 1.2 V	--	Yes	On	Fiber plugged



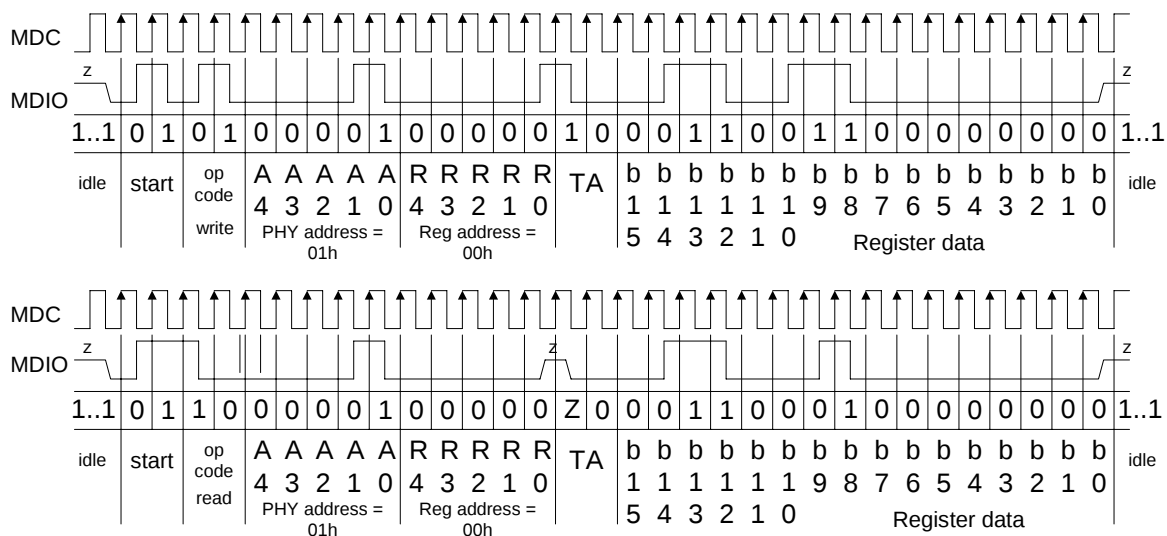
4.8 Serial management interface

User can access IP178D's MII registers through serial management interface with pin MDC and MDIO. Its format is shown in the following table. To access MII register in IP178D, MDC should be at least one more cycle than MDIO. That is, a complete command consists of 32 bits MDIO data and at least 33 MDC clocks. When the SMI is idle, MDIO is in high impedance.

System diagram



Frame format	<Idle><start><op code><PHY address><Registers address><turnaround><data><idle>
Read Operation	<Idle><01><10><A ₄ A ₃ A ₂ A ₁ A ₀ ><R ₄ R ₃ R ₂ R ₁ R ₀ ><Z0> <b ₁₅ b ₁₄ b ₁₃ b ₁₂ b ₁₁ b ₁₀ b ₉ b ₈ b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀ ><Idle>
Write Operation	<Idle><01><01><A ₄ A ₃ A ₂ A ₁ A ₀ ><R ₄ R ₃ R ₂ R ₁ R ₀ ><10> <b ₁₅ b ₁₄ b ₁₃ b ₁₂ b ₁₁ b ₁₀ b ₉ b ₈ b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀ ><Idle>





5 Register descriptions

5.1 Register map

5.1.1 EEPROM map

	7	6	5	4	3	2	1	0
0~1	Load EEPROM (55AA)							
2	bp_k ind	bf_st m_e n	mlk3 _det _en	aps_ dis	aging		mod bck	drop extra long packet
3	priori ty_ra te	led_o_sel		reduce _lpg	drop16	x_en	mod_c arrier_ algorit hm	bk_en
4	input_f ilter	hash_mode						bi_col or
5	tmode_sel						mdi_ mdix _en	
6	port_m irror_e n	port_mirror_mod e				sel_mirror_port		
7	sel_rx_port_mirror							
8	sel_tx_port_mirror							
9	fiber_duplex[7:6]							
10			userdef_ran ge_en[1:0]		predef_port_en[3:0]			
11	userdef_range0_high[7:0]							
12	userdef_range0_high[15:8]							
13	userdef_range0_low[7:0]							
14	userdef_range0_low[15:8]							
15	userdef_range1_high[7:0]							
16	userdef_range1_high[15:8]							
17	userdef_range1_low[7:0]							
18	userdef_range1_low[15:8]							
19	lpp_aging_en_[7:0]							
20 ~ 64								
65						port0_ cos_e n	port0_ high_p riority	
66								
67						port1_ cos_e n	port1_ high_p riority	

	7	6	5	4	3	2	1	0
68								
69						port2_ cos_e n	port2_ high_p riority	
70								
71						port3_ cos_e n	port3_ high_p riority	
72								
73						port4_ cos_e n	port4_ high_p riority	
74								
75						port5_ cos_e n	port5_ high_p riority	
76								
77						port6_ cos_e n	port6_ high_p riority	
78								
79						port7_ cos_e n	port7_ high_p riority	
80 ~ 81								
82	unit_high_thr_sel			predro p_en	pkt_low_thr_sel	pkt_high_thr_sel		
83	bf_stm_thr_sel	share_full_thr_sel		unit_default_thr_sel		unit_low_thr_sel		
84 ~ 124								
125	diffser v_en		bf_ffft only	special_add_forward				



5.1.2 MII register map

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
30.0	Software Reset Register(55AA)															
30.1	priority_rate	led_o_sel		reduce_ipg	drop16	x_en	modify_carrier_algorithm	bk_en	bp_ki nd	bf_stm_en	mlt3_det_e n	aps_d is	aging		modb ck	drop_ex tra_long _packet
30.2	tmode_sel					mdi_md ix_en			input _filetr	hash_mode						bi_col or
30.3	port_mi rror_en	port_mirror_mode							sel_rx_port_mirror							
30.4	sel_mirror_port								sel_tx_port_mirror							
30.12																
30.13	fiber_duple x[7]	fiber_duple x[6]						port_backpress_en								
30.14	lpp_aging_en[7:0]										userdef_range_en[1 :0]		predef_port_en[3:0]			
30.15	userdef_range0_high[15:0]															
30.16	userdef_range0_low[15:0]															
30.17	userdef_range1_high[15:0]															
30.18	userdef_range1_low[15:0]															



	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31.0						port0_c os_en	port 0_high_ priority									
31.1						port1_c os_en	port 1_high_ priority									
31.2						port2_c os_en	port 2_high_ priority									
31.3						port3_c os_en	port 3_high_ priority									
31.4						port4_c os_en	port 4_high_ priority									
31.5						port5_c os_en	port 5_high_ priority									
31.6						port6_c os_en	port 6_high_ priority									
31.7						port7_c os_en	port 7_high_ priority									
31.8																
31.9	bf_stm_thr_sel		share_full_thr_sel		unit_default_thr_sel		unit_low_thr_sel		unit_high_thr_sel			predrop_en	pkt_low_thr_sel		pkt_high_thr_sel	
31.10~29																
31.30			diffse rv_en	bf_fff f_onl y	special_add_forward											



5.2 PHY registers

R/W = Read/Write, SC = Self-Clearing, RO = Read Only, LL = Latching Low, LH = Latching High

5.2.1 Basic MII registers of port 0

5.2.1.1 MII control registers (address 00)

PHY	MI	ROM	R/W	Description	Default
0	0.15	--		Reset	0
0	0.14	--	R/W	Loop back 1 = Loop back mode 0 = normal operation When this bit set, IP178D will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN.	0
0	0.13	--	RW	Speed Selection 1 = 100 Mbps 0 = 10 Mbps It is valid only if bit 0.12 is set to be 0.	1
0	0.12	--	RW	Auto-Negotiation Enable 1 = Auto-Negotiation Enable 0 = Auto-Negotiation Disable	1
0	0.11	--	R/W	Power Down	0
0	0.10	--		Isolate	0
0	0.9	--	RW SC	Restart Auto- Negotiation 1 = re-starting Auto-Negotiation 0 = Auto-Negotiation re-start complete Setting this bit to logic high will cause IP178D to restart an Auto-Negotiation cycle, but depending on the value of bit 0.12 (Auto-Negotiation Enable). If bit 0.12 is cleared then this bit has no effect, and it is Read Only. This bit is self-clearing after Auto-Negotiation process is completed.	0
0	0.8	--	R/W	Duplex mode 1 = full duplex 0 = half duplex It is valid only if bit 0.12 is set to be 0.	0
0	0.7	--	R/W	Collision test	0
0	0[6:0]	--	R/W	Write as 0, ignore on read	-



5.2.1.2 MII status registers (address 01)

PHY	MII	ROM	R/W	Description	Default
0	1.15	--	RO	100Base-T4 capable 1 = 100Base-T4 capable 0 = not 100Base-T4 capable IP178D does not support 100Base-T4. This bit is fixed to be 0.	0
0	1.14	--	RO	100Base-X full duplex Capable 1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable The default of this bit will change depend on the external setting of IP178D. If external pin setting without 100Base-X full duplex support, then this bit will change default to logic 0.	1
0	1.13	--	RO	100Base-X half duplex Capable 1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable The default of this bit will change depend on the external setting of IP178D. If external pin setting without 100Base-X half duplex support, then this bit will change default to logic 0	1
0	1.12	--	RO	10Base-T full duplex Capable 1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable The default of this bit will change depend on the external setting of IP178D. If external pin setting without 100Base-T full duplex support, then this bit will change default to logic 0	1
0	1.11	--	RO	10Base-T half duplex Capable 1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable The default of this bit will change depend on the external setting of IP178D. If external pin setting without 100Base-X full duplex support, then this bit will change default to logic 0	1
0	1[10:7]	--	RO	Reserved Ignore on read	-
0	1.6	--	RO	MF preamble Suppression 1 = preamble may be suppressed 0 = preamble always required	1
0	1.5	--	RO	Auto-Negotiation Complete 1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0.	0



PHY	MII	ROM	R/W	Description	Default
0	1.4	--	RO LH	Remote fault 1 = remote fault detected 0 = not remote fault detected When read as logic 1, indicates that IP178D has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP178D reset.	0
0	1.3	--	RO	Auto-Negotiation Ability 1 = Auto-Negotiation capable 0 = not Auto-Negotiation capable When read as logic 1, indicates that IP178D has the ability to perform Auto-Negotiation. The value of this bit will depend on the external mode setting of IP178D operation mode.	1
0	1.2	--	RO LL	Link Status 1 = Link Pass 0 = Link Fail When read as logic 1, indicates that IP178D has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.	0
0	1.1	--		Jabber Detect 1 = jabber condition detected 0 = no jabber condition detected When read as logic 1, indicates that IP178D has detected a jabber condition. This bit is always 0 for 100 Mbps operation and is cleared after IP178D reset. This bit is set until jabber condition is cleared and reading the contents of the register.	0
0	1.0	--	RO	Extended capability 1 = Extended register capabilities 0 = No extended register capabilities IP178D has extended register capabilities.	1



5.2.1.3 PHY Identifier (address 02)

PHY	MII	ROM	R/W	Description	Default
0	2	--	RO	IP178D OUI (Organizationally Unique Identifier) ID, the MSB is 3rd bit of IP178D OUI ID, and the LSB is 18th bit of IP178D OUI ID. IP178D OUI is 0090C3.	0243h

5.2.1.4 PHY Identifier (address 03)

PHY	MII	ROM	R/W	Description	Default
0	3[15:10]	--	RO	PHY identifier IP178D OUI ID, the MSB is 19th bit of IP178D OUI ID, and LSB is 24th bit of IP178D OUI ID.	3h
0	3[9:4]	--	RO	Manufacture's Model Number IP178D model number	18h
0	3[3:0]	--	RO	Revision Number IP178D revision number	0



5.2.1.5 Auto-Negotiation Advertisement registers (address 04)

PHY	MII	ROM	R/W	Description	Default
0	4.15	--		Next Page Not supported	0
0	4.14	--	RW	Reserved by IEEE, write as 0, ignore on read	0
0	4.13	--	R/W	Remote Fault Not supported	0
0	4[12:11]	--	RO	Reserved for future IEEE use, write as 0, ignore on read	0
0	4.10	--	RW	Pause 1 = Advertises that this device has implemented pause function 0 = No pause function supported	0
0	4.9	--	RW	100BASE-T4 Not supported	0
0	4.8	--	R/W	100BASE-TX full duplex 1 = 100BASE-TX full duplex is supported 0 = 100BASE-TX full duplex is not supported	1
0	4.7	--	R/W	100BASE-TX 1 = 100BASE-TX is supported 0 = 100BASE-TX is not supported	1
0	4.6	--	R/W	10BASE-T full duplex 1 = 10BASE-T full duplex is supported 0 = 10BASE-T full duplex is not supported	1
0	4.5	--	R/W	10BASE-T 1 = 10BASE-T is supported 0 = 10BASE-T is not supported	1
0	4[4:0]	--	R/W	Selector Field Use to identify the type of message being sent by Auto-Negotiation.	00001



5.2.1.6 Link partner ability registers (address 05)

PHY	MII	ROM	R/W	Description	Default
0	5.15		RO	Next Page 1 = Next Page ability is supported by link partner 0 = Next Page ability does not supported by link partner	0
0	5.14		RO	Acknowledge 1 = Link partner has received the ability data word 0 = Not acknowledge	0
0	5.13		RO	Remote Fault 1 = Link partner indicates a remote fault 0 = No remote fault indicate by link partner If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1.	0
0	5[12:11]	--	RO	Reserved by IEEE for future use, write as 0, read as 0.	0
0	5.10	--	RO	Pause 1 = Link partner support IEEE802.3x 0 = Link partner does not support IEEE802.3x IP178D will reload the default value after rest or link failure.	1
0	5.9	--	RO	100BASE-T4 1 = Link partner support 100BASE-T4 0 = Link partner does not support 100BASE-T4	0
0	5.8	--	RO	100BASE-TX full duplex 1 = Link partner support 100BASE-TX full duplex 0 = Link partner does not support 100BASE-TX full duplex	0
0	5.7	--	RO	100BASE-TX 1 = Link partner support 100BASE-TX 0 = Link partner does not support 100BASE-TX	0
0	5.6	--	RO	10BASE-T full duplex 1 = Link partner support 10BASE-T full duplex 0 = Link partner does not support 10BASE-T full duplex	0
0	5.5	--	RO	10BASE-T 1 = Link partner support 10BASE-T 0 = Link partner does not support 10BASE-T	0
0	5[4:0]	--	RO	Selector Field Protocol selector of the link partner	00000



5.2.2 Basic MII registers of port 1-7

PHY	MII	ROM	R/W	Description	Default
Port 1 MII register 0~5					
1	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 2 MII register 0~5					
2	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 3 MII register 0~5					
3	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 4 MII register 0~5					
4	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 5 MII register 0~5					
5	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 6 MII register 0~5					
6	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 7 MII register 0~5					
7	0~5	--		Please refer to MII registers 0.0~0.5.	



5.3 Switch control registers (I)

PHY	MII	ROM	R/W	Description	Default
EEPROM enable register / Software reset register					
30	--	1, 0		EEPROM enable register This register should be filled with 55AA in EEPROM register 0 and 1. IP178D will examine the specified pattern to confirm if there is a valid EEPROM. The initial setting is updated with the content of EEPROM only if the specified pattern 55AA is found.	
30	0	--	R/W	Software reset register MII register 0 is software reset register. User can reset IP178D by writing 55AA to this register.	
30	0[15]	--	R	BFLI_FULL, free buffer is full 1: full, 0: not full This bit is for debug only.	
30	0[14]			Reserved	
30	0[13]	--	R	Empty, all output queue is empty 1: empty 0: not empty This bit is for debug only.	
30	0[12:0]			Reserved	

5.4 Switch control registers (II)

PHY	MII	ROM	R/W	Description	Default
30	1[15]	3[7]	R/W	PRIORITY_RATE 1: 8 packets 0: 16 packets Output Queue Scheduling: high priority packet rate	1'b0
30	1[14:13]	3[6:5]	R/W	LED_O_SEL LED mode selection	P(1,1)
				LINK_LED SPEED_LED FDX_LED	
				00 Off: link fail On: 10 Mbps link ok Flash: TX/RX Off: link fail On: 100 Mbps link ok Flash: TX/RX Off: half duplex On: full duplex	
				01 Off: link fail On: link ok Flash: RX Off: 10 Mbps On: 100 Mbps Off: half duplex On: full duplex Flash: collision	
				10 Off: link fail On: 10 Mbps link ok Flash: TX/RX Off: link fail On: 100 Mbps link ok Flash: TX/RX Off: half duplex On: full duplex Flash: collision	
				11 Off: link fail On: link ok Flash: TX/RX Off: 10 Mbps On: 100 Mbps Off: half duplex On: full duplex Flash: collision	
30	1[12]	3[4]	R/W	REDUCE_IPG This function reduce the IPG by random from 0 ~ 20 PPM. 1: enable, 0:disable	1'b1
30	1[11]	3[3]	R/W	Drop16 1: enable, 0:disable	1'b0
30	1[10]	3[2]	R/W	X_EN IEEE 802.3x flow control enable 1: enable, 0:disable	P(1)
30	1[9]	3[1]	R/W	MOD_CARRIER_ALGORITHM Modified carrier based collision algorithm 1: enable, 0:disable	1'b0
30	1[8]	3[0]	R/W	BK_EN, Backpressure enable 1: enable, 0: disable	P(1)
30	1[7]	2[7]	R/W	BP_KIND, Backpressure type selection It is valid only if BK_EN is set to 1'b1. 0: carrier base backpressure 1: reserved	1'b0
30	1[6]	2[6]	R/W	BF_STM_EN, Broadcast storm enable 1: enable IP178D drops the incoming packet if the number of broadcast packet in queue is over the threshold. 0: disable	P(0)



5.5 Switch control registers (III)

PHY	MII	ROM	R/W	Description	Default
30	1[5]	2[5]	R/W	MLT3_DET Ability for detecting MLT3 (for 10 Mbps switch to 100 Mbps) 0: disable MLT3 detection ability (default) 1: enable MLT3 detection ability.	P(0)
30	1[4]	2[4]	R/W	APS_DIS Disable advanced power saving mode 0: enable advance power saving mode (default) 1: disable advance power saving mode	P(0)
30	1[3:2]	2[3:2]	R/W	AGING. Aging time of address table selection An address tag in hashing table will be removed if this function is turned on and its aging timer expires.	P(1,0)
				Aging time	
				00	no aging
				01	30s
				10	300s
				11	reserved
30	1[1]	2[1]	R/W	MODBCK. Turn on modified back off algorithm The maximum back off period is limited to 8-slot time if this function is turned on. 1: turn on, 0: turn off	P(1)
30	1[0]	2[0]	R/W	Drop extra long packet Max forwarded packet length 0: 1536 bytes (default) 1: 1552 bytes	P(0)



5.6 Test mode control registers

PHY	MII	ROM	R/W	Description	Default
Test mode control registers					
30	2[15:10]	5[7:2]	R/W	TMODE_SEL. Test mode selection This function is for testing only. The default value must be adopted for normal operation.	6'b0
30	2[9]	5[1]	R/W	MDI_MDIX_EN. Auto MDIMDIX enable 1: Auto MDIMDIX (default) 0: fixed MDI Note: IP178D always uses a MDIX transformer.	P(1)
30	2[8]			Reserved	
30	2[7]	4[7]	R/W	INPUT_FILTER Packet is filtered in input port. 1: perform input filtering when queue full 0: no operation (default)	0
30	2[6:5]	4[6:5]	R/W	HASH_MODE MAC address table hashing mode 00: direct + CRC mapping (default) 11: direct mapping	2'b00
30	2[4:1]			Reserved	
30	2[0]	4[0]	R/W	BI_COLOR Bi-color LED mode 0: disable (default) 1: enable	P(0)



5.7 Port mirroring control registers

PHY	MII	ROM	R/W	Description	Default
30	3[15]	6[7]	R/W	PORT_MIRROR_EN	1'b0
	3[14:13]	6[6:5]	R/W	PORT_MIRROR_MODE Select a mirror mode to monitor 00: mirror one port of RX (default) 01: mirror one port of TX 10: mirror source-destination pair (TX and RX port should be different) 11: mirror one port of TX and RX (TX and RX port must be the same)	2'b00
	3[12:8]			Reserved	
	3[7:0]	7[7:0]	R/W	SEL_RX_PORT_MIRROR Select the source (receive) port to be mirrored 0000_0001: port 0 (default) 0000_0010: port 1 0000_0100: port 2 0000_1000: port 3 0001_0000: port 4 0010_0000: port 5 0100_0000: port 6 1000_0000: port 7	8'h01
	4[15:13]	6[2:0]	R/W	SEL_MIRROR_PORT Select a mirror port to monitor any other port 000: port 0 001: port 1 010: port 2 011: port 3 100: port 4 101: port 5 110: port 6 111: port 7 (default)	3'b111
	4[12:8]			Reserved	
	4[7:0]	8[7:0]	R/W	SEL_TX_PORT_MIRROR Select the destination (transmit) port to be mirrored 0000_0001: port 0 (default) 0000_0010: port 1 0000_0100: port 2 0000_1000: port 3 0001_0000: port 4 0010_0000: port 5 0100_0000: port 6 1000_0000: port 7	8'h01

5.8 Fiber duplex setting registers

PHY	MII	ROM	R/W	Description	Default
30	13[15:14]	9[7:6]	R/W	FIBER_DUPLEX Fiber duplex setting for each port. 1: fiber port is full-duplex 0: fiber port is half_duplex bit[15]: port 7 duplex ability setting bit[14]: port 6 duplex ability setting	2'b11
30	13.13	9[5]	R/W	BUF_AGING_EN	1'b0
30	13.12	9[4]	R/W	SRC_BLK_PROTECT	1'b1
30	13[13:8]			Reserved	

5.9 Backpressure setting registers

PHY	MII	ROM	R/W	Description	Default
30	13[7:0]	--	R/W	PORT_BACKPRESSURE_EN Backpressure ability setting at half-duplex mode for each port. To ensure this function works correctly, BK_EN (backpressure enable, reg 30.1[8]) should set to logic zero first. 1: enable backpressure ability 0: disable bit[7]: port 7 enable backpressure ability bit[6]: port 6 enable backpressure ability bit[5]: port 5 enable backpressure ability bit[4]: port 4 enable backpressure ability bit[3]: port 3 enable backpressure ability bit[2]: port 2 enable backpressure ability bit[1]: port 1 enable backpressure ability bit[0]: port 0 enable backpressure ability	8'h00



5.10 TCP/UDP port priority registers

PHY	MII	ROM	R/W	Description	Default
30	14[15:8]	19[7:0]	R/W	LPP_AGING_EN TCP/UDP logical port priority aging enable 0: disable TCP/UDP logical port priority aging function 1: enable TCP/UDP logical port priority aging function When this function active, once receive a IP frame with TCP/UDP protocol and the logical port number is the pre-defined port number, the ingress port will treat as a port based high priority port for 300 seconds. After the internal timer expired, the ingress port will change back to previous behavior. bit[15]: port 7 logical port priority aging enable bit[14]: port 6 logical port priority aging enable bit[13]: port 5 logical port priority aging enable bit[12]: port 4 logical port priority aging enable bit[11]: port 3 logical port priority aging enable bit[10]: port 2 logical port priority aging enable bit[9]: port 1 logical port priority aging enable bit[8]: port 0 logical port priority aging enable	P(0)
30	14[7:6]			Reserved	
30	14[5:4]	10[5:4]	R/W	USERDEF_RANGE_EN User defined logic port range enable. bit[5]: user define range 1 register enable bit[4]: user define range 0 register enable	2'b11
30	14[3:0]	10[3:0]	R/W	PREDEF_PORT_EN Pre-defined logic port number enable. bit[3]: logic port set 3 enable, port 6000 bit[2]: logic port set 2 enable, port 3389 bit[1]: logic port set 1 enable, port 443 bit[0]: logic port set 0 enable, port 22	4'hF
30	15	12, 11	R/W	USERDEF_RANGE0_HIGH User defined logic port range 0 high limit	16'd23
30	16	14, 13	R/W	USERDEF_RANGE0_LOW User defined logic port range 0 low limit	16'd23
30	17	16.15	R/W	USERDEF_RANGE1_HIGH User defined logic port range 1 high limit	16'd 5800
30	18	18.17	R/W	USERDEF_RANGE1_LOW User defined logic port range 1 low limit	16'd 5800



5.11 CoS control registers – port 0

PHY	MII	ROM	R/W	Description	Default
31	0[10]	65[2]	R/W	Port 0 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port 0 are handled as high priority packets.	1'b0
	0[9]	65[1]	R/W	Port 0 set to be high priority port 1: enable, 0: disabled (default) Packets received from port 0 are handled as high priority packets.	1'b0

5.12 CoS control registers – port 1

PHY	MII	ROM	R/W	Description	Default
31	1[10]	67[2]	R/W	Port 1 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port 1 are handled as high priority packets.	1'b0
	1[9]	67[1]	R/W	Port 1 set to be high priority port 1: enable, 0: disabled (default) Packets received from port 1 are handled as high priority packets.	1'b0

5.13 CoS control registers – port 2

PHY	MII	ROM	R/W	Description	Default
31	2[10]	69[2]	R/W	Port 2 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port 2 are handled as high priority packets.	1'b0
	2[9]	69[1]	R/W	Port 2 set to be high priority port 1: enable, 0: disabled (default) Packets received from port 2 are handled as high priority packets.	1'b0

5.14 CoS control registers – port 3

PHY	MII	ROM	R/W	Description	Default
31	3[10]	71[2]	R/W	Port 3 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port 3 are handled as high priority packets.	1'b0
	3[9]	71[1]	R/W	Port 3 set to be high priority port 1: enable, 0: disabled (default) Packets received from port 3 are handled as high priority packets.	1'b0



5.15 CoS control registers – port 4

PHY	MII	ROM	R/W	Description	Default
CoS and port base VLAN register 4					
31	4[10]	73[2]	R/W	Port 4 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port 4 are handled as high priority packets.	1'b0
	4[9]	73[1]	R/W	Port 4 set to be high priority port 1: enable, 0: disabled (default) Packets received from port 4 are handled as high priority packets.	1'b0

5.16 CoS control registers – port 5

PHY	MII	ROM	R/W	Description	Default
31	5[10]	75[2]	R/W	Port 5 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port 5 are handled as high priority packets.	1'b0
	5[9]	75[1]	R/W	Port 5 set to be high priority port 1: enable, 0: disabled (default) Packets received from port 5 are handled as high priority packets.	1'b0

5.17 CoS control registers – port 6

PHY	MII	ROM	R/W	Description	Default
31	6[10]	77[2]	R/W	Port 6 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port 6 are handled as high priority packets.	1'b0
	6[9]	77[1]	R/W	Port 6 set to be high priority port 1: enable, 0: disabled (default) Packets received from port 6 are handled as high priority packets.	1'b0

5.18 CoS control registers – port 7

PHY	MII	ROM	R/W	Description	Default
31	7[10]	79[2]	R/W	Port 7 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port 7 are handled as high priority packets.	1'b0
	7[9]	79[1]	R/W	Port 7 set to be high priority port 1: enable, 0: disabled (default) Packets received from port 7 are handled as high priority packets.	1'b0



5.19 Switch control registers (IV)

PHY	MII	ROM	R/W	Description	Default
31	9[15:14]	83[7:6]	R/W	BF_STM_THR_SEL[1:0]. Broadcast storm threshold selection 00: 2 packets/10ms for 100Mbps port, or 2 packets/100ms for 10Mbps port, 01: 6 packets/10ms for 100Mbps port, or 6 packets/100ms for 10Mbps port, 10: 14 packets/10ms for 100Mbps port, or 14 packets/100ms for 10Mbps port, 11: 30 packets/10ms for 100Mbps port, or 30 packets/100ms for 10Mbps port	2'b00
	9[13:12]	83[5:4]	R/W	SHARE_FULL_THR_SEL[1:0]. Share buffer threshold selection 00: 160 units 01: 180 units 10: 140 units 11: 120 units	2'b00
	9[11:10]	83[3:2]	R/W	UNIT_DEFAULT_THR_SEL[1:0]. Output Queue minimum threshold selection 00: 40 units 01: 32 units 10: 48 units 11: 56 units	2'b00
	9[9:8]	83[1:0]	R/W	UNIT_LOW_THR_SEL	2'b00
	9[7:6]	82[7:6]	R/W	UNIT_HIGH_THR_SEL[1:0]. Output Queue Flow control ON threshold selection If share buffer is over share buffer full threshold, Output Queue Flow control ON threshold will be dynamic changed to 28. Others, 00: 50 units 01: 70 units 10: 90 units 11: 110 units	2'b00
	9[5]			Reserved	
	9[4]	82[4]	R/W	PREDROP_EN 1: Drop an incoming broadcast packet if any port is congested. 0: forward an incoming broadcast packet to un-congested ports instead of congested ports.	0
	9[3:2]	82[3:2]	R/W	PKT_LOW_THR_SEL[1:0]. Packet low water mark threshold selection 00: 40 units 01: 30 units 10: 20 units 11: 10 units	2'b00



PHY	MII	ROM	R/W	Description	Default
	9[1:0]	82[1:0]	R/W	PKT_HIGH_THR_SEL[1:0]. Packet high water mark threshold selection 00: 50 units 01: 40 units 10: 30 units 11: 20 units	2'b00



5.20 Switch control registers (V)

PHY	MII	ROM	R/W	Description	Default
31	30[15:8]	125	R/W	[15:14]: Reserved [13]: DIFFSERV_EN [12]: BF_FFFF_ONLY 1: broadcast DA=FFFFFFFF 0: broadcast DA=FFFFFFFF and multicast frame	8'h0d
				[11:8]: special_add_forward	
				bit 3 Reserved MAC address (0180C2000010-0180C20000FF) 1: forward (default), 0: discard.	
				bit 2 Reserved MAC address (0180C2000002- 0180C200000F) 1: forward (default), 0: discard. The default value is the inverted value of pin 78 FILTER_RSV_DA.	
				bit 1 Reserved MAC address (0180C2000001) 1: forward, 0: discard (default)	
				bit 0 Reserved MAC address (0180C2000000) 1: forward (default) 0: discard	
	30[7:0]			Reserved	



6 Crystal Specifications

Item	Parameter	Range
1	Nominal Frequency	25.000 MHz
2	Oscillation Mode	Fundamental Mode
3	Frequency Tolerance at 25	+/- 50 ppm
4	Temperature Characteristics	+/- 50 ppm
5	Operating Temperature Range	-10 ~ +70
6	Equivalent Series Resistance	40 ohm Max.
7	Drive Level	100 μ W
8	Load Capacitance	20 pF
9	Shunt Capacitance	7 pF Max
10	Insulation Resistance	Mega ohm Min./DC 100V
11	Aging Rate A Year	+/- 5 ppm/year



7 Electrical Characteristics

7.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	– 0.3V to 4.0V
Input Voltage	– 0.3V to 5.0V
Output Voltage	– 0.3V to 5.0V
Storage Temperature	– 65°C to 150°C
Ambient Operating Temperature (Ta) (IP178D LF)	0°C to 70°C
Ambient Operating Temperature (Ta) (IP178D LFI)	– 40 °C to 85°C

7.2 DC Characteristic

Operating Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	1.80	1.95	2.05	V	
Supply Voltage	VCC_O	3.135 2.25	3.3 2.5	3.465 2.75	V	VCC_O =3.3V VCC_O =2.5V
Power Consumption			1.35		W	100 Mbps full, VCC=1.95V

Input Clock

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency			25		MHz	
Frequency Tolerance		-50		+50	PPM	

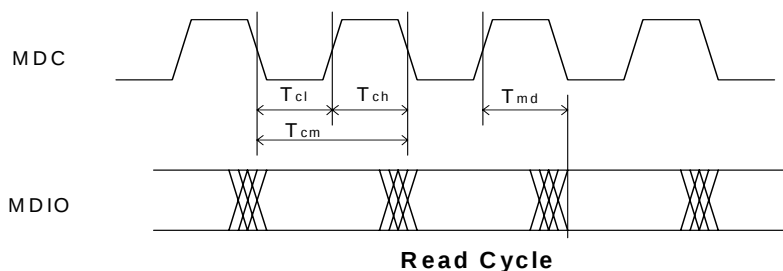
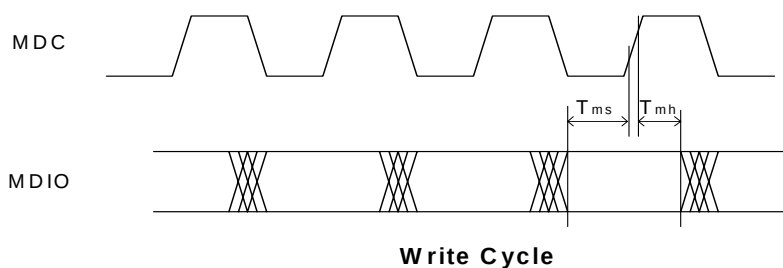
I/O Electrical Characteristics

Parameter	Sym	Min.	Max.	Unit	Conditions
Input Low Voltage -LED PAD direct mode -LED PAD bicolor mode -NOT LED PAD	VIL		0.39*VCC_O 0.36*VCC_O 0.4*VCC_O	V	
Input High Voltage -LED PAD direct mode -LED PAD bicolor mode -NOT LED PAD	VIH	0.58*VCC_O 0.58*VCC_O 0.6*VCC_O		V	
Output Low Voltage	VOL		0.4	V	IOH=4mA, VCC_O_x=3.3V
Output High Voltage	VOH	2.4		V	IOL=4mA, VCC_O_x=3.3V

7.3 AC Timing

7.3.1 Serial Management Interface Timing

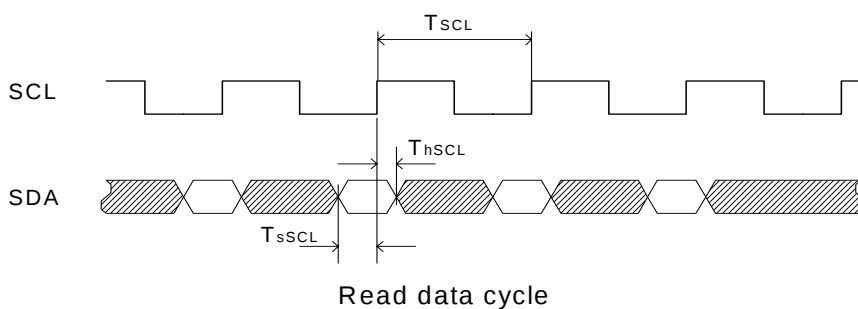
Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC High Time	40	-	-	ns
T_{cl}	MDC Low Time	40	-	-	ns
T_{cm}	MDC period	80	-	-	ns
T_{md}	MDIO output delay	-	-	15	ns
T_{mh}	MDIO setup time	10	-	-	ns
T_{ms}	MDIO hold time	10	-	-	ns



7.3.2 EEPROM Timing

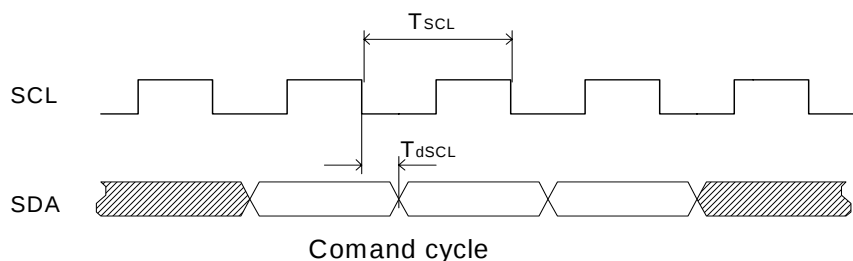
7.3.2.1 Data read cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	20480	-	ns
T_{sSCL}	SDA to SCL setup time	2	-	-	ns
T_{hSCL}	SDA to SCL hold time	0.5	-	-	ns



7.3.2.2 Command cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	20480	-	ns
T_{dSCL}	SCL falling edge to SDA	-	-	5200	ns



7.4 Thermal Data

Theta Ja	Theta Jc	Conditions	Units
30.7~32.5	11.6~12.4	2 Layer PCB	°C/W
25.0~26.6	11.1~11.7	4 Layer PCB	°C/W

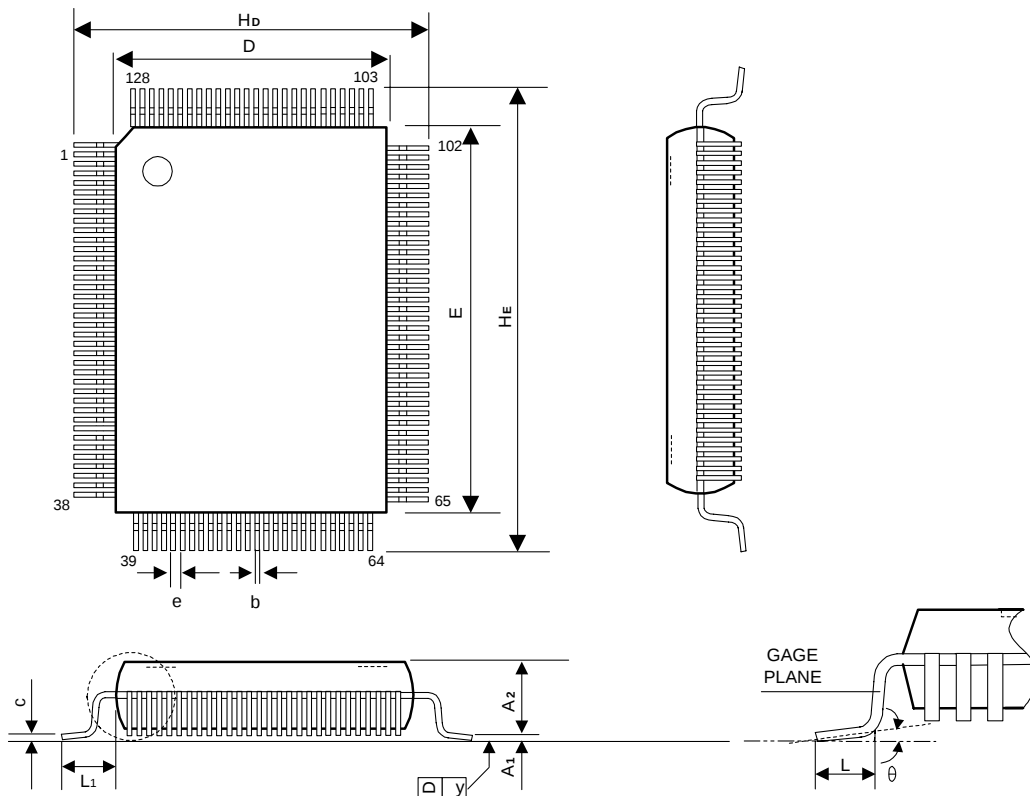


8 Order Information

Part No.	Package	Notice
IP178D LF	128-PIN PQFP	
IP178D LFI	128-PIN PQFP	-40°C to 85°C

9 Package Detail

128 PQFP Outline Dimensions



Symbol	Dimensions In Inches			Dimensions In mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A1	0.010	0.014	0.018	0.25	0.35	0.45
A2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.09	0.15	0.20
HD	0.669	0.677	0.685	17.00	17.20	17.40
D	0.547	0.551	0.555	13.90	14.00	14.10
HE	0.906	0.913	0.921	23.00	23.20	23.40
E	0.783	0.787	0.791	19.90	20.00	20.10
e	-	0.020	-	-	0.50	-
L	0.025	0.035	0.041	0.65	0.88	1.03
L1	-	0.063	-	-	1.60	-
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Note:

1. Dimension D & E do not include mold protrusion.
2. Dimension B does not include dambar protrusion. Total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.