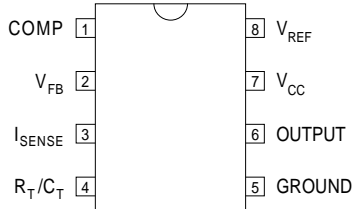
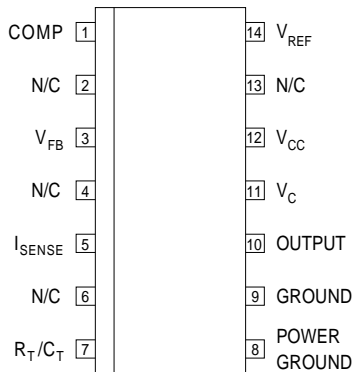


**TOP VIEW**



**J Package – 8 Pin Ceramic DIP**  
**N Package – 8 Pin Plastic DIP**  
**D-8 Package – 8 Pin Plastic (150) SOIC**

**TOP VIEW**



**D-14 Package – 14 Pin Plastic (150) SOIC**

**CURRENT MODE  
REGULATING  
PULSE WIDTH  
MODULATORS**

**FEATURES**

- Guaranteed  $\pm 1\%$  reference voltage tolerance
- Accurate oscillator discharge current
- Guaranteed  $\pm 10\%$  frequency tolerance
- Low start-up current ( $< 500 \mu A$ )
- Under voltage lockout with hysteresis
- Output state completely defined for all supply and input conditions
- Interchangeable with IP and UC1842/3 series for improved operation
- 500kHz Oscillator operation

**Order Information**

Part Number	J-Pack 8 Pin	N-Pack 8 Pin	D-8 8 Pin	D-14 14 Pin	Temp. Range	Note:
IP1842A	✓				-55 to +125°C	To order, add the package identifier to the part number.
IP2842A	✓	✓	✓	✓	-25 to +85°C	
IP3842A	✓	✓	✓	✓	0 to +70°C	
IP1843A	✓				-55 to +125°C	eg. IP1842AD-14 IP3843AJ
IP2843A	✓	✓	✓	✓	-25 to +85°C	
IP3843A	✓	✓	✓	✓	0 to +70°C	

**ABSOLUTE MAXIMUM RATINGS** ( $T_{case} = 25^\circ C$  unless otherwise stated)

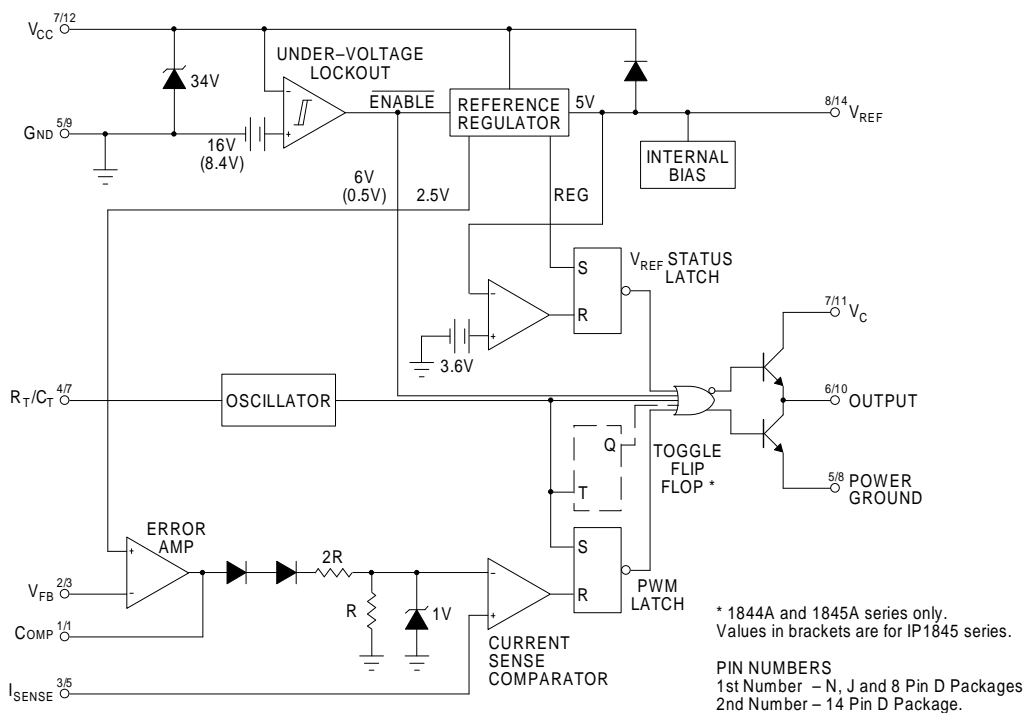
$V_{CC}$	Supply Voltage	(low impedance source) ( $I_{CC} < 30mA$ )		+30V Self limiting
$I_O$	Output Current			$\pm 1A$
	Output Energy	(capacitive load)		5 $\mu J$
	Analog Inputs	(pins 2 and 3)		-0.3V to $+V_{CC}$
	Error Amp Output Sink Current			10mA
$P_D$	Power Dissipation	$T_{amb} = 25^\circ C$	J, N Packages	1W
	Derate @ $T_{amb} > 50^\circ C$			10mW/ $^\circ C$
$P_D$	Power Dissipation	$T_{case} = 25^\circ C$	D Package	725mW
	Derate @ $T_{amb} > 50^\circ C$			7.25mW/ $^\circ C$
$P_D$	Power Dissipation	$T_{case} = 25^\circ C$	J, N Packages	2W
	Derate @ $T_{case} > 25^\circ C$			16mW/ $^\circ C$
$T_{STG}$	Storage Temperature Range			-65 to 150°C
$T_L$	Lead Temperature	(soldering, 10 seconds)		+300°C

**DESCRIPTION**

The IP1842A/IP1843A series of switching regulator control circuits contain all the functions necessary to implement off-line, current mode switching regulators, using a minimum number of external parts. Functions included are voltage reference, error amplifier, current sense comparator, oscillator, totem-pole output driver and under-voltage lockout circuitry.

Although pin compatible with the standard IP1842/3 parts these devices offer improved performance in several areas. They also offer tighter specification and improved performance over the IP and UC1842/3 series, whilst retaining complete compatibility.

**BLOCK DIAGRAM**



**RECOMMENDED OPERATING CONDITIONS**

$V_{CC}$	Supply Voltage <sup>1</sup>	$\leq 30V$
$I_O$	Output Current	0 to $\pm 200mA$
	Analog Inputs (pins 2 and 3)	-0.3V to 3V
	Error Amp Output Sink Current	0 to 2mA
	Operating Ambient Temperature Range	IP1842A , IP1843A IP2842A , IP2843A IP3842A , IP3843A
		-55 to 125°C -25 to 85°C 0 to 70°C

**Notes:**

1. Lower limit set by under voltage lockout specification.

**ELECTRICAL CHARACTERISTICS** (Over Full Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions <sup>1</sup>	IP1842A , IP1843A IP2842A , IP2843A			IP3842A IP3843A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>REFERENCE SECTION</b>								
Output Voltage	$I_O = 1\text{mA}$ $T_J = 25^\circ\text{C}$	4.95	5.00	5.05	4.90	5.00	5.10	V
Input Regulation	$V_{CC} = 12\text{V to } 25\text{V}$		6	20		6	20	mV
Output Regulation	$I_O = 1\text{mA to } 20\text{mA}$		6	25		6	25	
Temperature Stability			0.2	0.4		0.2	0.4	$\frac{\text{mV}}{^\circ\text{C}}$
Total Output Variation	Line, Load, Temp	4.90		5.10	4.82		5.18	V
Output Noise Voltage	$f = 10\text{Hz to } 10\text{kHz}$ $T_J = 25^\circ\text{C}$		50			50		$\mu\text{V}$
Long Term Stability	$T_J = 125^\circ\text{C @ } 1000\text{Hrs}$		5	25		5	25	mV
Output Short Circuit Current	$V_{REF} = 0$	30	80	160	30	80	160	mA
<b>OSCILLATOR SECTION</b>								
Frequency	$T_J = 25^\circ\text{C}$	47	52	57	47	52	57	kHz
Voltage Stability	$V_{CC} = 12\text{V to } 25\text{V}$		0.2	1		0.2	1	%
Temperature Stability	$\Delta T_A = \text{Min to Max}$		5			5		%
Amplitude	$V_{PIN4}$ Peak to Peak		1.7			1.7		V
Discharge Current	$T_J = 25^\circ\text{C}$	7.8	8.3	8.8	7.8	8.3	8.8	mA
	$\Delta T_A = \text{Min to Max}$	7		9	7		9	
<b>ERROR AMP SECTION</b>								
Input Voltage	$V_{PIN1} = 2.5\text{V}$	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	$\mu\text{A}$
Open Loop Voltage Gain	$V_O = 2\text{V to } 4\text{V}$	65	90		65	90		dB
Unity Gain Bandwidth		0.7	1		0.7	1		MHz
Supply Voltage Rejection	$V_{CC} = 12\text{V to } 25\text{V}$	60	70		60	70		dB
Output Sink Current	$V_{PIN2} = 2.7\text{V}$ $V_{PIN1} = 1.1\text{V}$	2	6		2	6		mA
Output Source Current	$V_{PIN2} = 2.3\text{V}$ $V_{PIN1} = 5\text{V}$	-0.5	-0.8		-0.5	-0.8		
$V_{OUT}$ High	$V_{PIN2} = 2.3\text{V}$ $R_L = 15\text{k}\Omega$	4.6	6		4.6	6		V
$V_{OUT}$ Low	$V_{PIN2} = 2.7\text{V}$ $R_L = 15\text{k}\Omega$		0.7	1.1		0.7	1.1	

**NOTES**

1. Test Conditions unless otherwise stated:

$V_{CC} = 15\text{V}^*$  ,  $R_T = 10\text{k}\Omega$  ,  $C_T = 3.3\text{nF}$  ,  $f = 52\text{kHz}$ .

\*Adjust  $V_{CC}$  above start threshold before setting at required level.

All specifications apply over the full operating temperature range unless otherwise stated.  
(See Ordering Information for further details).

**ELECTRICAL CHARACTERISTICS** (Over Full Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions <sup>1</sup>	IP1842A , IP1843A IP2842A , IP2843A			IP3842A IP3843A			Units		
		Min.	Typ.	Max.	Min.	Typ.	Max.			
<b>CURRENT SENSE SECTION</b>										
Gain	See Notes 2,3	2.85	3	3.15	2.85	3	3.15	V/V		
Maximum Input Signal	V <sub>PIN1</sub> = 5V (Note 2)	0.9	1	1.1	0.9	1	1.1	V		
Supply Voltage Rejection	V <sub>C</sub> = 12V to 25V	60	70		60	70		dB		
Input Bias Current			-2	-10		-2	-10	μA		
Delay to Output			150	300		150	300	ns		
<b>OUTPUT SECTION</b>										
Output Low Level	I <sub>SINK</sub> = 20mA		0.1	0.4		0.1	0.4	V		
	I <sub>SINK</sub> = 200mA		1.5	2.2		1.5	2.2			
Output High Level	I <sub>SOURCE</sub> = 20mA	13	13.5		13	13.5		V		
	I <sub>SOURCE</sub> = 200mA	12	13.5		12	13.5				
Rise Time	C <sub>L</sub> = 1nF		50	150		50	150	ns		
Fall Time	C <sub>L</sub> = 1nF		50	150		50	150			
UVLO Saturation	V <sub>CC</sub> = 6V I <sub>L</sub> = 1mA		0.7	1.1		0.7	1.1	V		
<b>UNDER-VOLTAGE LOCKOUT SECTION</b>										
Upper Threshold (V <sub>CC</sub> )	IP1842A Series	15	16	17	14.5	16	17.5	V		
	IP1843A Series	7.8	8.4	9	7.8	8.4	9			
Lower Threshold (V <sub>CC</sub> )	IP1842A Series	9	10	11	8.5	10	11.5	V		
	IP1843A Series	7	7.6	8.2	7	7.6	8.2			
<b>TOTAL STANDBY CURRENT</b>										
Start-up Current			0.3	0.5		0.3	0.5	mA		
Operating Supply Current	V <sub>PIN2</sub> = 0V	IP1842A Series		11	15		11	15	mA	
	V <sub>PIN3</sub> = 0V		IP1843A Series		14	17		14		17
V <sub>CC</sub> Zener Voltage	I <sub>CC</sub> = 25mA		30	34	40		30	34	40	V
<b>PWM SECTION</b>										
Maximum Duty Cycle			95	97	100		95	97	100	%
Minimum Duty Cycle					0				0	

**NOTES**

1. Test Conditions unless otherwise stated:

V<sub>CC</sub> = 15V\*, R<sub>T</sub> = 10kΩ, C<sub>T</sub> = 3.3nF, f = 52kHz.

\*Adjust V<sub>CC</sub> above start threshold before setting at required level.

2. Parameter measured at trip point of latch with

V<sub>PIN2</sub> = 0V

3. Gain defined as:

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}}$$

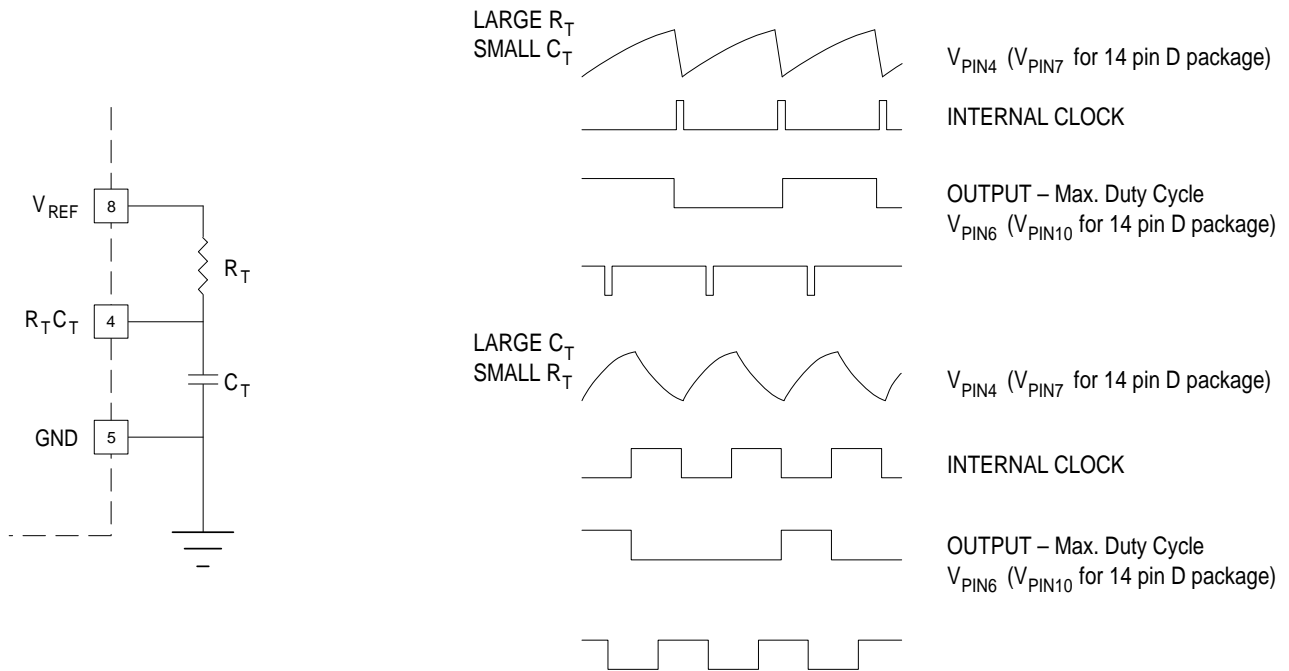
$$0 \leq V_{PIN3} \leq 0.8$$

All specifications apply over the full operating temperature range unless otherwise stated.

(See Ordering Information for further details).

**APPLICATIONS INFORMATION**

**Oscillator Waveforms and Maximum Duty Cycle**



Oscillator timing capacitor  $C_T$  is charged by  $V_{REF}$  through  $R_T$  and discharged by an internal current source. During the discharge time, the internal clock signal blanks the output to the low state. Selection of  $R_T$  and  $C_T$  therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulae:

$$t_c \approx 0.55 R_T C_T$$

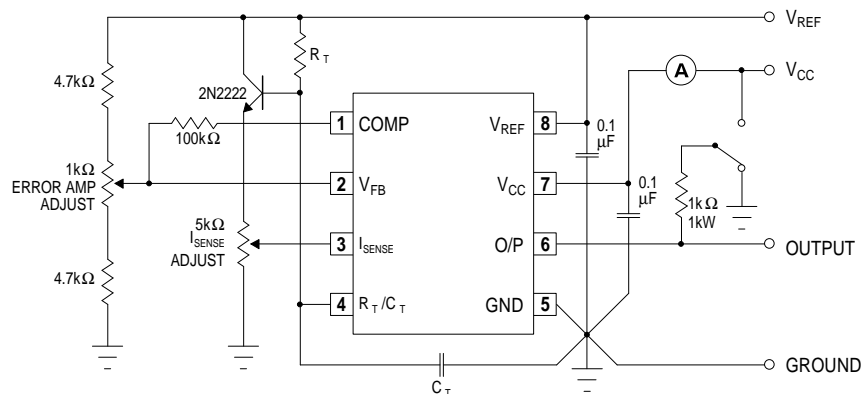
$$t_d \approx R_T C_T \ln \left( \frac{.0063 R_T - 2.3}{.0063 - 4} \right)$$

$$\text{Resultant frequency } f = \frac{1}{(t_c + t_d)}$$

For  $R_T > 5k\Omega$ ,

$$\text{Resultant frequency } f \approx \frac{1.8}{(R_T C_T)}$$

**Open-Loop Laboratory Test Fixture**



High peak current associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

**TYPICAL PERFORMANCE CHARACTERISTICS**

