

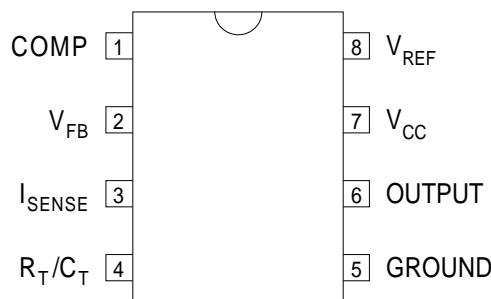


**SEME
LAB**

IP3842N-200.01

CURRENT MODE REGULATING PULSE WIDTH MODULATORS

TOP VIEW



FEATURES

- Guaranteed $\pm 10\%$ frequency tolerance
- Low start-up current ($< 200 \mu A$)
- Under voltage lockout with hysteresis
- Output state completely defined for all supply and input conditions
- 500kHz operation

N Package – 8 Pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

V _{CC}	Supply Voltage	(low impedance source) (I _{CC} < 30mA)	+30V Self limiting
I _O	Output Current		$\pm 1A$
	Output Energy	(capacitive load)	5μJ
	Analog Inputs	(pins 2 and 3)	-0.3V to +V _{CC}
	Error Amp Output Sink Current		10mA
P _D	Power Dissipation Derate @ T _{amb} > 50°C	T _{amb} = 25°C	1W 10mW/°C
P _D	Power Dissipation Derate @ T _{case} > 25°C	T _{case} = 25°C	2W 24mW/°C
T _{STG}	Storage Temperature Range		-65 to 150°C
T _L	Lead Temperature	(soldering, 10 seconds)	+300°C



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ELECTRICAL CHARACTERISTICS (Over Full Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
REFERENCE SECTION					
Output Voltage	$I_O = 1\text{mA}$ $T_J = 25^\circ\text{C}$	4.90	5.00	5.10	V
Input Regulation	$V_{CC} = 12\text{V}$ to 25V	6	20		mV
Output Regulation	$I_O = 1\text{mA}$ to 20mA	6	25		
Temperature Stability		0.2	0.4		mV/ $^\circ\text{C}$
Total Output Variation	Line, Load, Temp	4.82	5.18		V
Output Noise Voltage	$f = 10\text{Hz}$ to 10kHz $T_J = 25^\circ\text{C}$	50			μV
Long Term Stability	$T_J = 125^\circ\text{C}$ @ 1000Hrs	5	25		mV
Output Short Circuit Current	$V_{REF} = 0$	30	80	160	mA
OSCILLATOR SECTION					
Frequency	$T_J = 25^\circ\text{C}$	47	52	57	kHz
Voltage stability	$V_{CC} = 12\text{V}$ to 25V	0.2	1		%
Temperature Stability	ΔT_A = Min to Max	5			%
Amplitude	V_{PIN4} Peak to Peak	1.7			V
Discharge Current	$T_J = 25^\circ\text{C}$	6.7	10.8		mA
	ΔT_A = Min to Max	8			%
ERROR AMP SECTION					
Input Voltage	$V_{PIN1} = 2.5\text{V}$	2.42	2.50	2.58	V
Input Bias Current		-0.3	-2		μA
Open Loop Voltage Gain	$V_O = 2\text{V}$ to 4V	65	90		dB
Unity Gain Bandwidth		0.7	1		MHz
Supply Voltage Rejection	$V_{CC} = 12\text{V}$ to 25V	60	70		dB
Output Sink Current	$V_{PIN2} = 2.7\text{V}$ $V_{PIN1} = 1.1\text{V}$	2	6		mA
Output Source Current	$V_{PIN2} = 2.3\text{V}$ $V_{PIN1} = 4.6\text{V}$	-0.5	-0.8		
V_{OUT} High	$V_{PIN2} = 2.3\text{V}$ $R_L = 15\text{k}\Omega$	4.6	4.8		V
V_{OUT} Low	$V_{PIN2} = 2.7\text{V}$ $R_L = 15\text{k}\Omega$	0.7	1.1		

NOTES

1. Test Conditions unless otherwise stated:

$V_{CC} = 15\text{V}^*$, $R_T = 10\text{k}\Omega$, $C_T = 3.3\text{nF}$, $f = 52\text{kHz}$.

*Adjust V_{CC} above start threshold before setting at required level.

All specifications apply over the full operating temperature range unless otherwise stated. (See Ordering Information for further details).



**SEME
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ELECTRICAL CHARACTERISTICS (Over Full Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
CURRENT SENSE SECTION					
Gain	See Notes 2,3	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN1} = 4.6V$ (Note 2)	0.9	1	1.1	V
Supply Voltage Rejection	$V_C = 12V$ to $25V$	60	70		dB
Input Bias Current			-2	-10	μA
Delay to Output		200	400		ns
OUTPUT SECTION					
Output Low Level	$I_{SINK} = 20mA$		0.1	0.4	V
	$I_{SINK} = 200mA$		1.5	2.2	
Output High Level	$I_{SOURCE} = 20mA$		13	13.5	V
	$I_{SOURCE} = 200mA$		12	13.5	
Rise Time	$C_L = 1nF$ $T_J = 25^\circ C$		50	150	ns
Fall Time	$C_L = 1nF$ $T_J = 25^\circ C$		50	150	
UVLO Saturation	$V_{CC} = 6V$ $I_L = 1mA$		0.7	1.1	V
UNDER-VOLTAGE LOCKOUT SECTION					
Upper Threshold (V_{CC})	1842 Series	14.5	16	17.5	V
Lower Threshold (V_{CC})	1842 Series	8.5	10	11.5	
TOTAL STANDBY CURRENT					
Start-up Current		0.16	0.2		mA
Operating Supply Current	$V_{PIN2} = 0V$ $V_{PIN3} = 0V$ 1842 Series	11	15		
V_{CC} Zener Voltage	$I_{CC} = 25mA$	30	34	40	V

NOTES

1. Test Conditions unless otherwise stated:

$V_{CC} = 15V^*$, $R_T = 10k\Omega$, $C_T = 3.3nF$, $f = 52kHz$.

*Adjust V_{CC} above start threshold before setting at required level.

All specifications apply over the full operating temperature range unless otherwise stated.

(See Ordering Information for further details).

2. Parameter measured at trip point of latch with

$V_{PIN2} = 0V$

3. Gain defined as:

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}}$$

$0 \leq V_{PIN3} \leq 0.8$