IP4369CX4

ESD protection for high-speed interfaces

Rev. 1 — 1 October 2012 Product data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as High-Definition Multimedia Interface (HDMI), DisplayPort, USB, external Serial Advanced Technology Attachment (eSATA) and Low Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The device includes high-level ESD protection diodes structure for high-speed signal lines in a 4-channel 0.4 mm pitch single Wafer-Level Chip-Scale Package (WLCSP). These features make the device ideal for use in applications requiring component miniaturization such as mobile phone handsets and other portable electronic devices.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of 0.8 pF (typical). These diodes provide protection to downstream components from ESD voltages up to ±8 kV contact according to IEC 61000-4-2, level 4.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- System ESD protection for USB 2.0, USB On-The-Go (USB OTG), Ethernet and Digital Visual Interface (DVI)
- All signal lines with integrated rail-to-rail clamping diodes structure for downstream ESD protection of ±8 kV according to IEC 61000-4-2, level 4
- 2 × 2 solder ball WLCSP with 0.4 mm pitch and height < 500 μm
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Line capacitance of only 0.8 pF for each channel

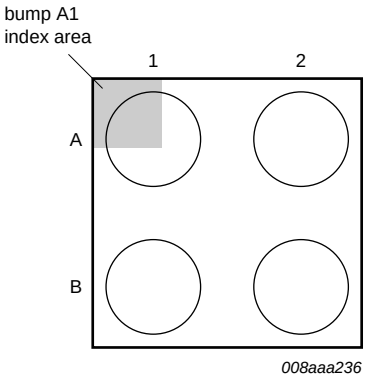
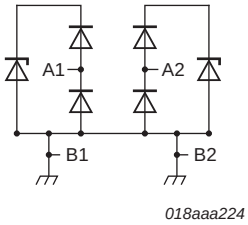
1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- Portable devices
- Mobile handsets
- Wireless data systems
- Digital cameras

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
A1 and A2	ESD protection		
B1 and B2	ground		

transparent top view,
solder balls facing down

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4369CX4	WLCSP4	wafer level chip-size package; 4 bumps (2 × 2)	IP4369CX4

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			–0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; contact discharge	[1]	-	±8	kV
T_{stg}	storage temperature			–55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	$t_p \leq 10$ s		-	+260	°C
T_{amb}	ambient temperature			–30	+85	°C

[1] Pins A1 and A2 to ground (B1 and B2).

5. Characteristics

Table 4. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{line}	line capacitance	per pin; pins A1 and A2 to GDN; V_{bias} = 0 V; f = 1 MHz	[1]	-	0.8	1	pF
$C_{(I/O-I/O)}$	input/output to input/output capacitance	GND not connected; V_{bias} = 0 V; f = 1 MHz	[1]	-	0.4	-	pF
I_{RM}	reverse leakage current	V_{bias} = 3 V		-	-	100	nA
V_{BR}	breakdown voltage	I_{test} = 1 mA		6	-	10	V
V_F	forward voltage			-	–0.7	-	V
R_{dyn}	dynamic resistance	TLP	[2]				
		positive transient		-	0.24	-	Ω
		negative transient		-	0.21	-	Ω
		surge	[3]				
		positive transient		-	0.21	-	Ω
		negative transient		-	0.16	-	Ω
V_{CL}	clamping voltage	I_{CL} = 4 A	[3]	-	4	-	V
		I_{CL} = –5 A	[3]	-	–3	-	V

[1] This parameter is guaranteed by design.

[2] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 80 ns.

[3] According to IEC 61000-4-5 (8/20 μs).

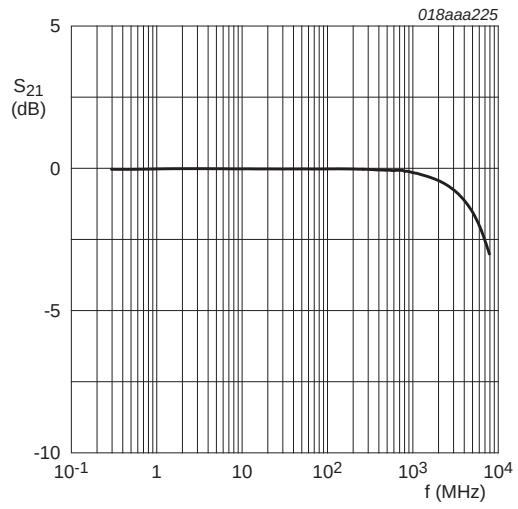


Fig 1. Mixed-mode differential insertion loss; typical values

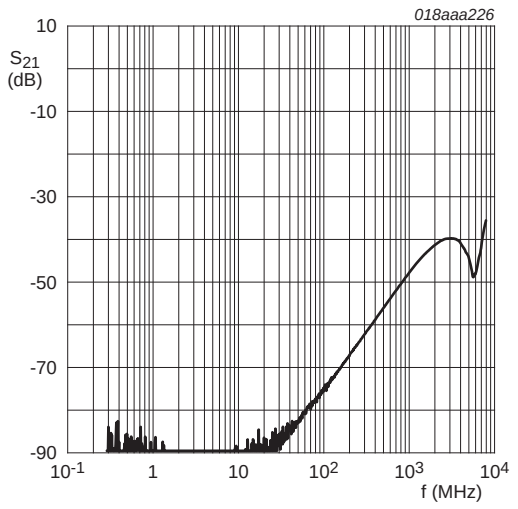
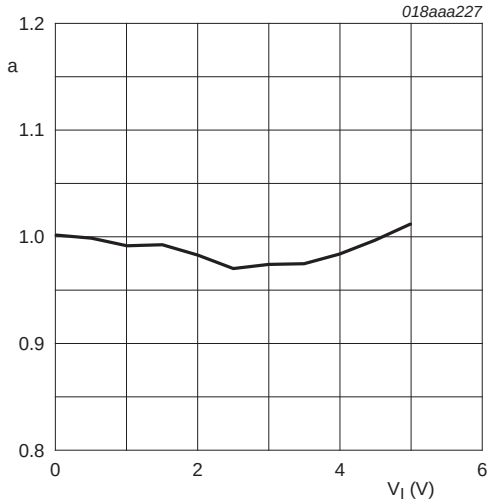
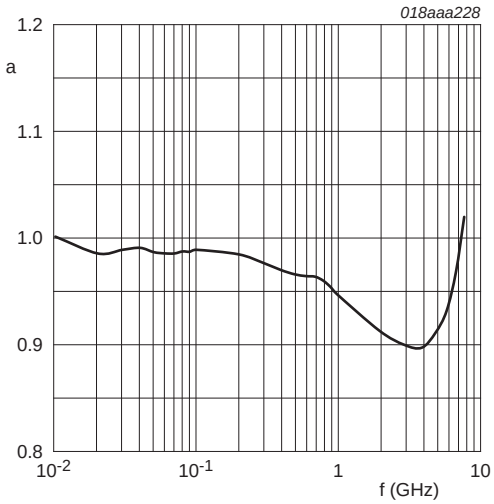


Fig 2. Mixed-mode differential crosstalk, typical values



$$a = \frac{C_{line}}{C_{line(V_{bias} = 0V)}}$$

Fig 3. Relative capacitance as a function of input voltage; typical values



$$a = \frac{C_{line}}{C_{line(f = 10MHz)}}$$

Fig 4. Relative capacitance as a function of frequency; typical values

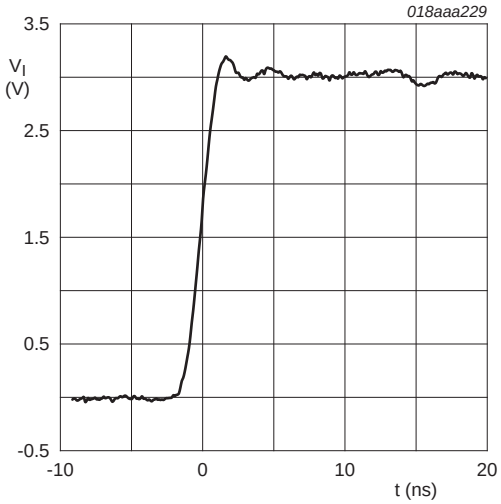


Fig 5. Input voltage for crosstalk measurements; channel 1; typical values

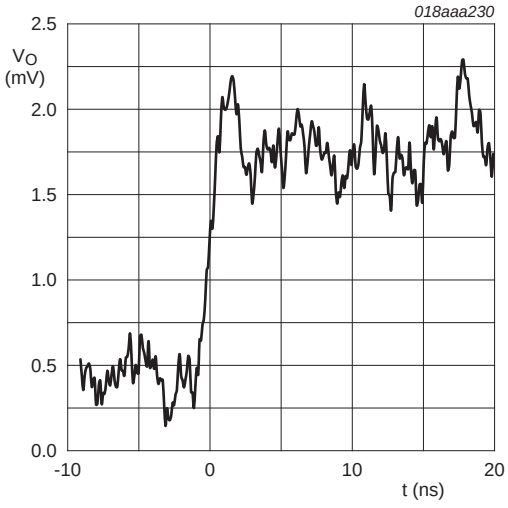
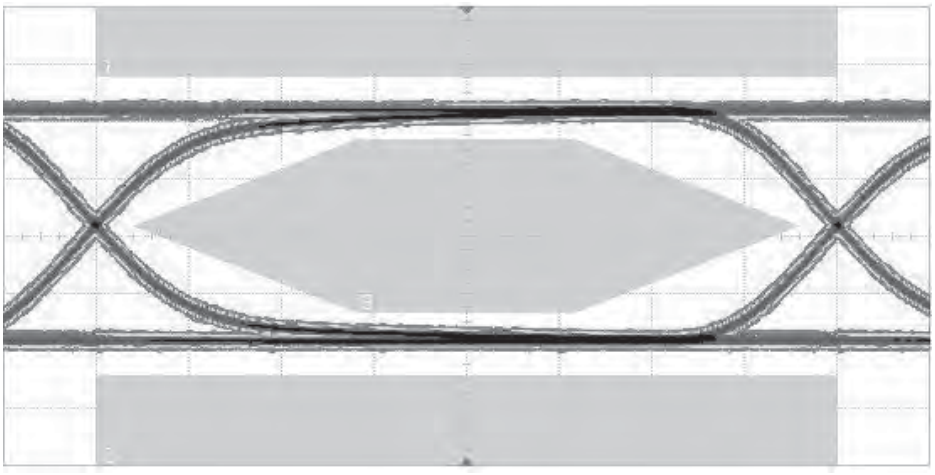


Fig 6. Output voltage for crosstalk measurements; channel 2; typical values

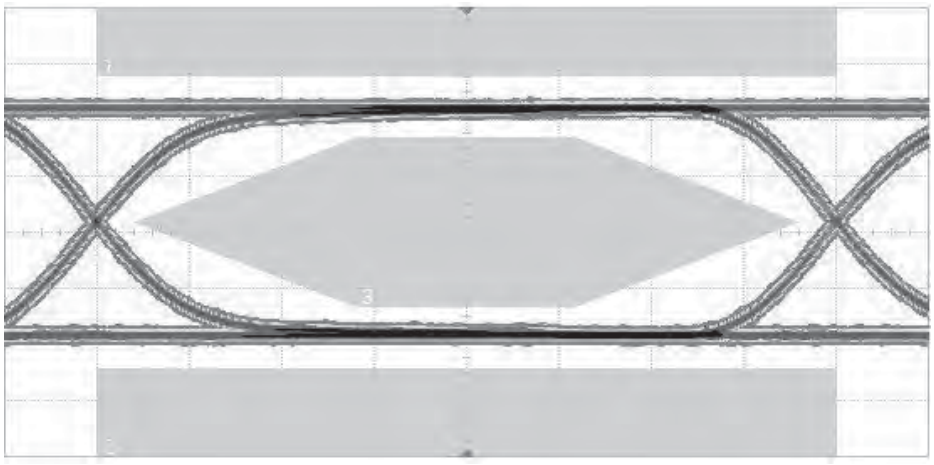
Figure 5 and 6 show time-domain crosstalk from channel 1 to channel 2. Generator impedance on channel 1 is 50 Ω, probe impedance on channel 2 is 1 MΩ.



018aaa231

Data rate: 480 Mbit/s (USB 2.0 High-speed)
Vertical scale = 200 mV/div
Horizontal scale = 260 ps/div

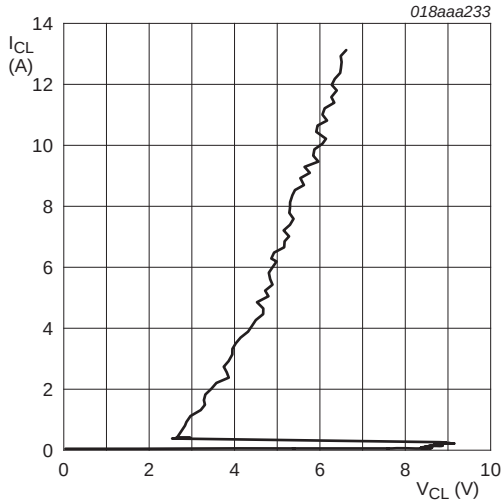
Fig 7. USB 2.0 eye diagram with IP4369CX4



018aaa232

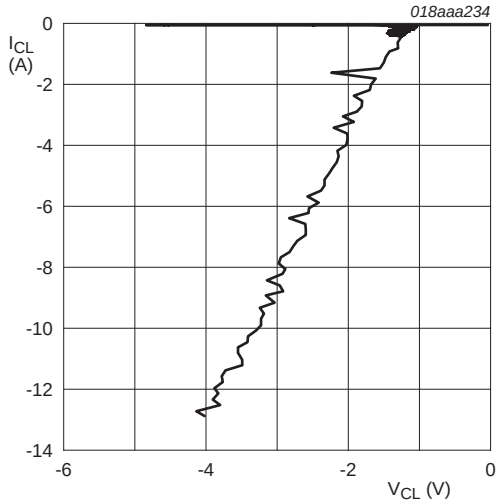
Data rate: 480 Mbit/s (USB 2.0 High-speed)
Vertical scale = 200 mV/div
Horizontal scale = 260 ps/div

Fig 8. USB 2.0 eye diagram without IP4369CX4



t_p = 100 ns; Transmission Line Pulse (TLP)

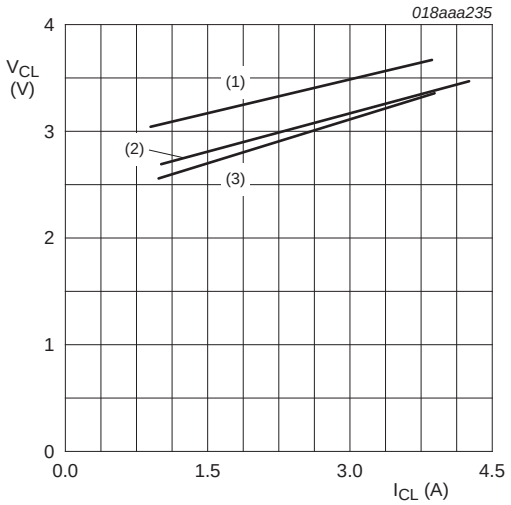
Fig 9. Dynamic resistance with positive clamping



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 10. Dynamic resistance with negative clamping

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).



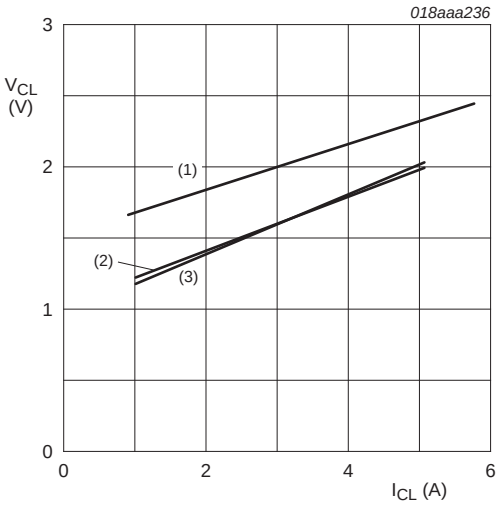
IEC 61000-4-5

(1) T_{amb} = 25 °C; y = 0.21x + 2.86

(2) T_{amb} = 75 °C

(3) T_{amb} = 125 °C

Fig 11. Surge pulse response test; positive transient, typical values



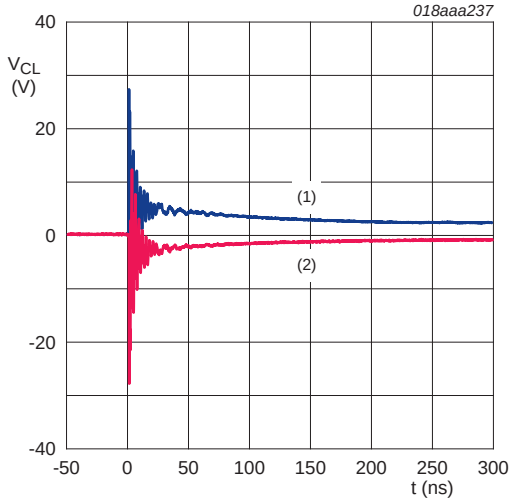
IEC 61000-4-5

(1) T_{amb} = 25 °C; y = 0.16x + 1.52

(2) T_{amb} = 75 °C

(3) T_{amb} = 125 °C

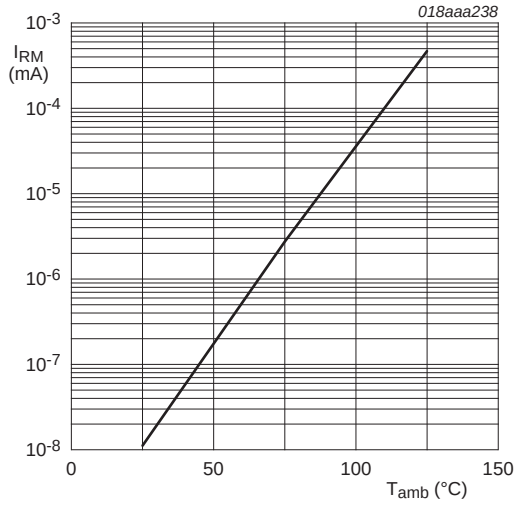
Fig 12. Surge pulse response test; negative transient, typical values



(1) +8 kV

(2) −8 kV

Fig 13. ESD pulse transient response; IEC 61000-4-2; contact discharge; typical values



V_{bias} = 3 V

Fig 14. Reverse leakage current as a function of ambient temperature; typical values

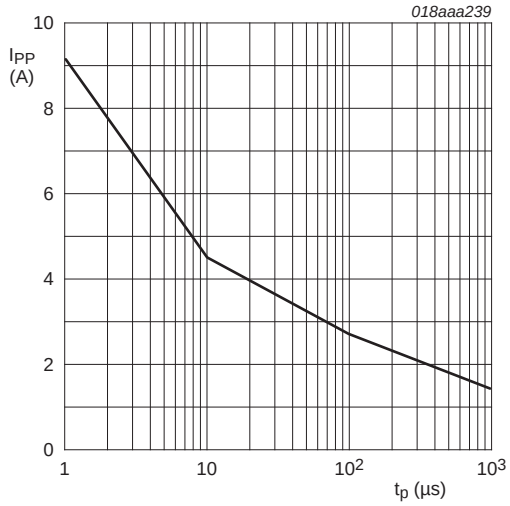


Fig 15. Peak pulse current as a function of pulse duration; rectangular pulses; typical values

6. Package outline

WLCSP4: wafer level chip-size package; 4 bumps (2 x 2)

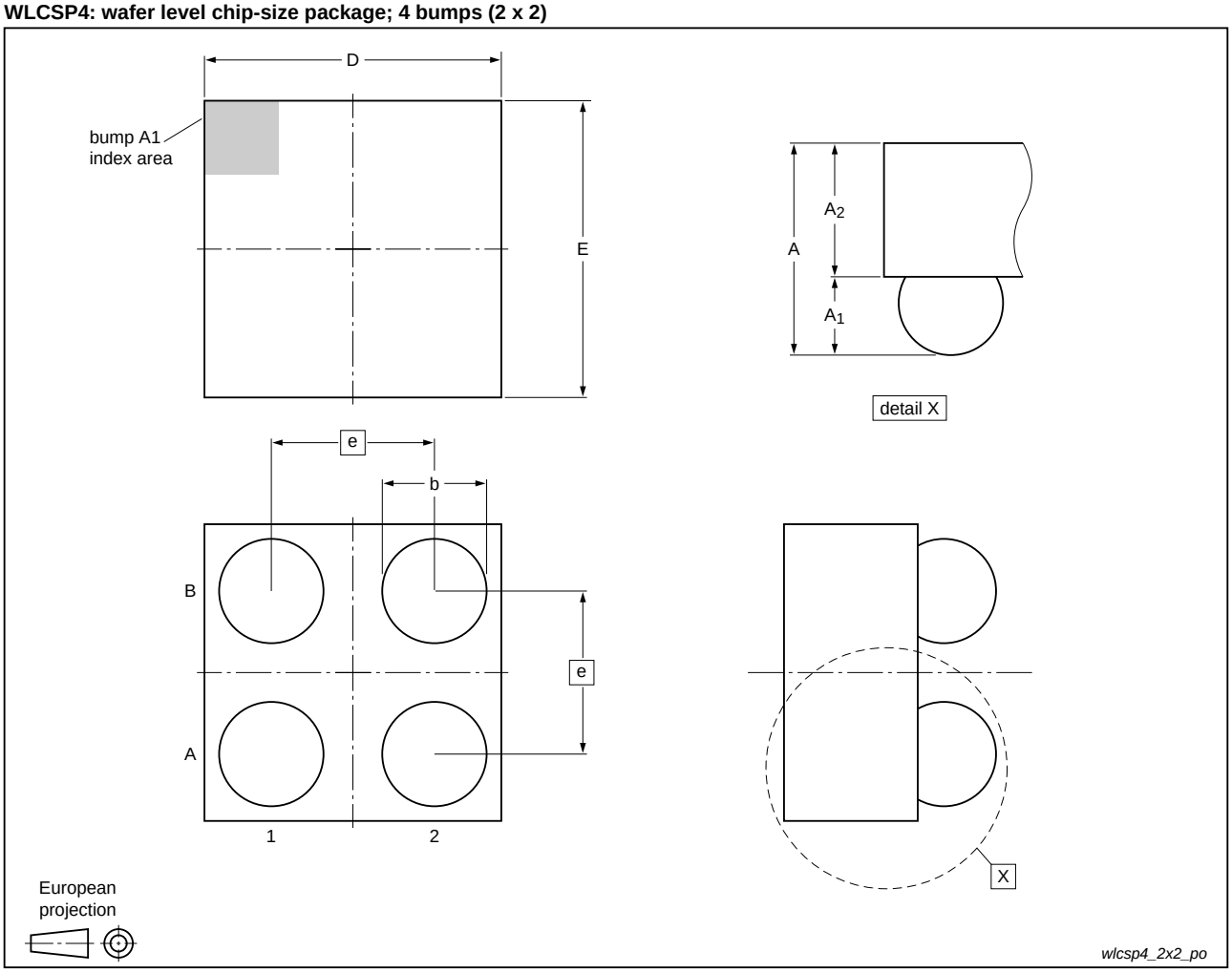


Fig 16. Package outline IP4369CX4 (WLCSP4)

Table 5. Package outline dimensions of IP4369CX4 (WLCSP4)

Symbol	Min	Typ	Max	Unit
A	0.44	0.47	0.50	mm
A_1	0.18	0.20	0.22	mm
A_2	0.26	0.27	0.28	mm
b	0.21	0.26	0.31	mm
D	0.71	0.76	0.81	mm
E	0.71	0.76	0.81	mm
e	0.35	0.40	0.45	mm

7. Design and assembly recommendations

7.1 PCB design guidelines

For optimum performance, use a Non-Solder Mask Defined (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. Refer to Table 6 for the recommended Printed-Circuit Board (PCB) design parameters.

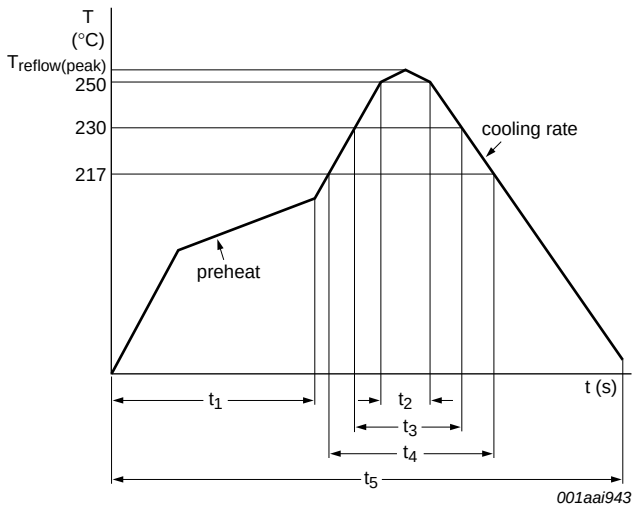
Table 6. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	250 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	325 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

7.2 PCB assembly guidelines for Pb-free soldering

Table 7. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	290 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %) Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 17



The device is capable of withstanding at least three reflows of this profile.

Fig 17. Pb-free solder reflow profile

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		pre-heat	2.5	-	4.0	°C/s

8. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4369CX4 v.1	20121001	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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