

**HDMI™**  
HIGH-DEFINITION MULTIMEDIA INTERFACE



# IP4776CZ38

Fully integrated HDMI interface with level shifter, ESD and backdrive protection

Rev. 01 — 14 July 2006

Product data sheet

## 1. General description

The IP4776CZ38 is designed for HDMI host-interface protection. The IP4776CZ38 includes level shifting for the DDC channels and backdrive protection for HDMI as well as high-level ESD protection diodes for the TMDS signal lines.

The level shifting function is required when the receiver operates at a supply voltage lower than the external devices to protect the I/Os against over voltages. The IP4776CZ38 contains four N-channel MOSFETs to provide this level shifting function.

Furthermore, all TMDS intra-pairs are protected by a special diode configuration offering an ultra low line capacitance of 0.7 pF only. These diodes provide protection to downstream components from ESD voltages up to  $\pm 8$  kV contact according to the IEC 61000-4-2, level 4 standard.

## 2. Features

- Pb-free and RoHS compliant
- Integrated high-level ESD protection, level shifting and backdrive protection
- All TMDS lines with integrated rail-to-rail clamping diodes with downstream ESD protection of  $\pm 8$  kV according to IEC 61000-4-2, level 4 standard
- Matched 0.5 mm trace spacing
- Bidirectional level shifting N-channel FETs provided for DDC clock and data channels
- TMDS lines with  $\leq 0.05$  pF matching of capacitance between the TMDS pairs
- Ultra low line capacitance of 0.7 pF per channel
- HDMI 1.3 compliant
- Backdrive protection
- 38-pin TSSOP lead-free package

## 3. Applications

- The IP4776CZ38 is designed for HDMI receiver and transmitter port protection, level shifting and backdrive protection e.g.:
  - ◆ TV
  - ◆ Graphics card
  - ◆ Set-top box
  - ◆ DVD
  - ◆ Digital media adapter
  - ◆ Game console

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## 4. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
IP4776CZ38	TSSOP38	plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm	SOT510-1

## 5. Functional diagram

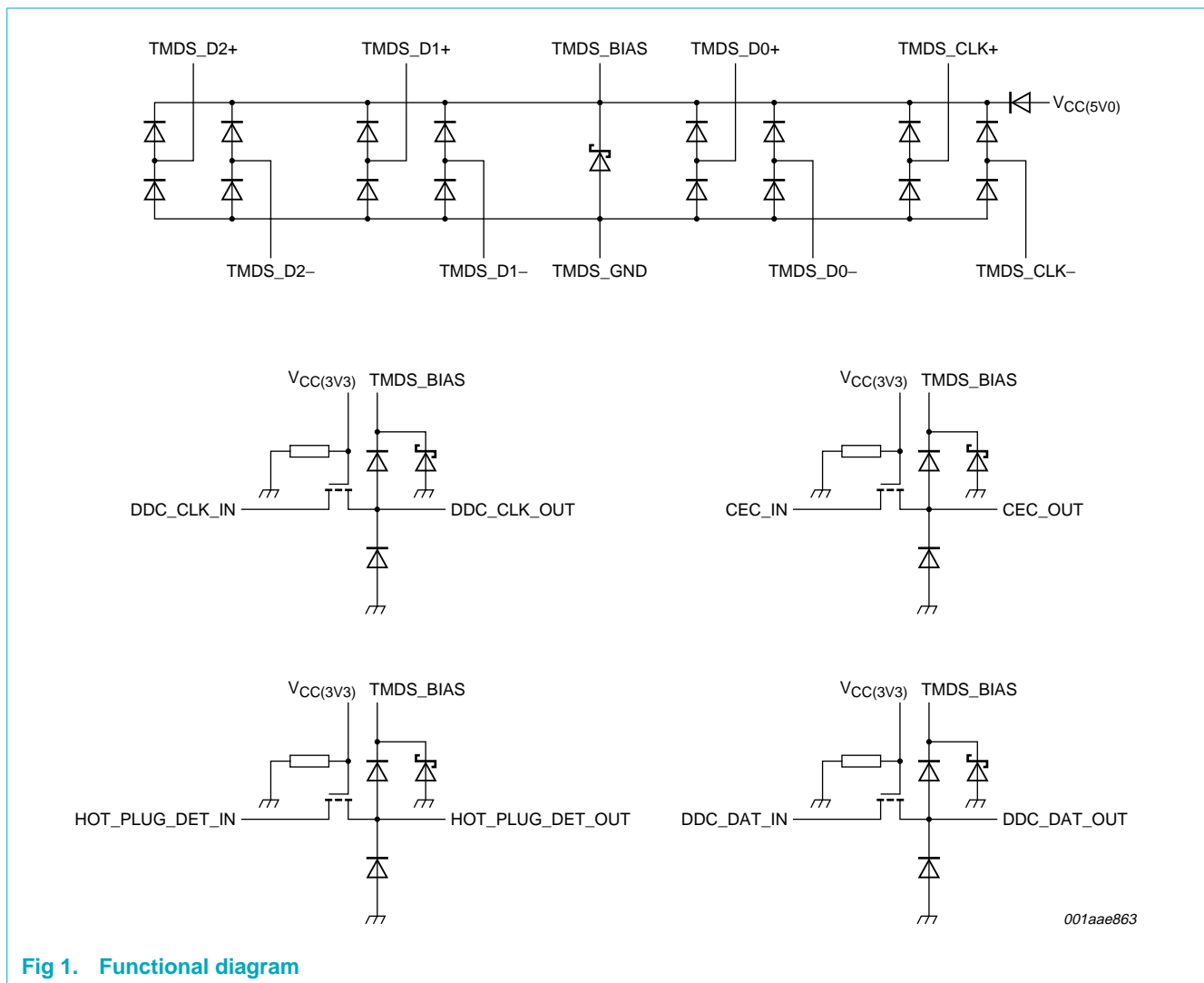
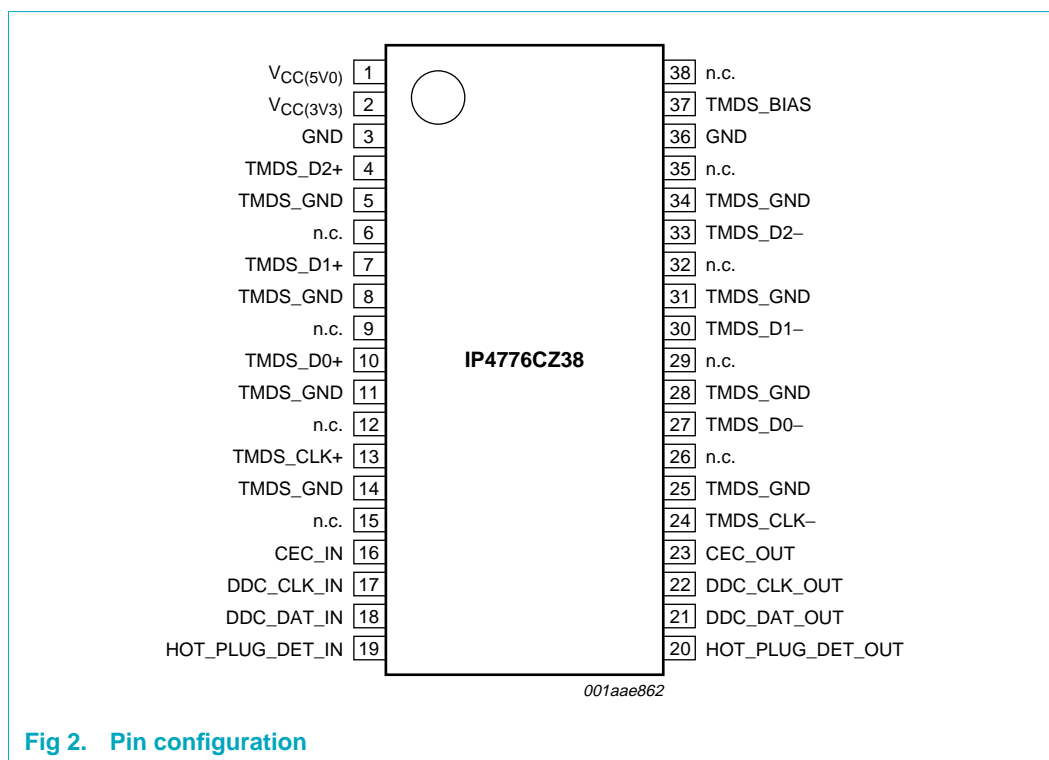


Fig 1. Functional diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
V <sub>CC</sub> (5V0)	1	supply voltage
V <sub>CC</sub> (3V3)	2	bias supply voltage for the level shifters
GND	3	ground reference <sup>[1]</sup>
TMDS_D2+	4	D2+ TMDS ESD protection <sup>[2]</sup>
TMDS_GND	5	ground reference <sup>[1]</sup>
n.c.	6	not connected <sup>[2]</sup>
TMDS_D1+	7	D1+ TMDS ESD protection <sup>[2]</sup>
TMDS_GND	8	ground reference <sup>[1]</sup>
n.c.	9	not connected <sup>[2]</sup>
TMDS_D0+	10	D0+ TMDS ESD protection <sup>[2]</sup>
TMDS_GND	11	ground reference <sup>[1]</sup>
n.c.	12	not connected <sup>[2]</sup>
TMDS_CLK+	13	CLK+ TMDS ESD protection <sup>[2]</sup>
TMDS_GND	14	ground reference <sup>[1]</sup>
n.c.	15	not connected <sup>[2]</sup>

Table 2. Pin description ...continued

Symbol	Pin	Description
CEC_IN	16	CEC input <sup>[3]</sup>
DDC_CLK_IN	17	DDC clock input <sup>[3]</sup>
DDC_DAT_IN	18	DDC data input <sup>[3]</sup>
HOT_PLUG_DET_IN	19	hot plug detection input <sup>[3]</sup>
HOT_PLUG_DET_OUT	20	hot plug detection output <sup>[4]</sup>
DDC_DAT_OUT	21	DDC data output <sup>[4]</sup>
DDC_CLK_OUT	22	DDC clock output <sup>[4]</sup>
CEC_OUT	23	CEC output <sup>[4]</sup>
TMDS_CLK-	24	CLK- TMDS ESD protection <sup>[2]</sup>
TMDS_GND	25	ground reference <sup>[1]</sup>
n.c.	26	not connected <sup>[2]</sup>
TMDS_D0-	27	D0- TMDS ESD protection <sup>[2]</sup>
TMDS_GND	28	ground reference <sup>[1]</sup>
n.c.	29	not connected <sup>[2]</sup>
TMDS_D1-	30	D1- TMDS ESD protection <sup>[2]</sup>
TMDS_GND	31	ground reference <sup>[1]</sup>
n.c.	32	not connected <sup>[2]</sup>
TMDS_D2-	33	D2- TMDS ESD protection <sup>[2]</sup>
TMDS_GND	34	ground reference <sup>[1]</sup>
n.c.	35	not connected <sup>[2]</sup>
GND	36	ground reference <sup>[1]</sup>
TMDS_BIAS	37	bias for TMDS ESD protection and bias for level shifter output ESD protection. This pin must be connected to a 0.1 $\mu$ F capacitor.
n.c.	38	not connected

[1] Pins GND and TMDS\_GND are internally connected.

[2] This pin always has to be connected to the pin on the opposite location of the IC via a PCB track to guarantee correct functionality; see [Figure 3](#), [Figure 4](#) and [Figure 5](#).

[3]  $V_{CC(3V3)}$  referenced logic level in.

[4]  $V_{CC(5V0)}$  referenced logic level out.

## 7. Limiting values

**Table 3. Limiting values**
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{CC}$	supply voltage		GND – 0.5	5.5	V	
$V_I$	input voltage	at input pins	GND – 0.5	5.5	V	
$V_{ESD}$	electrostatic discharge voltage	signal pins; IEC 61000-4-2, level 4	[1]			
		contact	[2]	–8	+8	kV
		air discharge	[2]	–15	+15	kV
		all other pins; MIL-STD-883 Method 3015 (human body model)				
		contact		–2	+2	kV
		air discharge		–2	+2	kV
$T_{stg}$	storage temperature		–55	+125	°C	

[1] Signal pins:

TMDS\_D2+, TMDS\_D2–, TMDS\_D1+, TMDS\_D1–, TMDS\_D0+, TMDS\_D0–,  
 TMDS\_CLK+, TMDS\_CLK–,  
 CEC\_OUT,  
 DDC\_DAT\_OUT,  
 DDC\_CLK\_OUT,  
 HOT\_PLUG\_DET\_OUT.

[2] This measurement is performed with an 0.1  $\mu$ F external capacitor on pin TMDS\_BIAS.

## 8. Recommended operating conditions

**Table 4. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb}$	ambient temperature		–40	-	+85	°C

## 9. Characteristics

**Table 5. Characteristics**
 *$T_{amb} = 25\text{ °C}$ ; unless otherwise specified.*

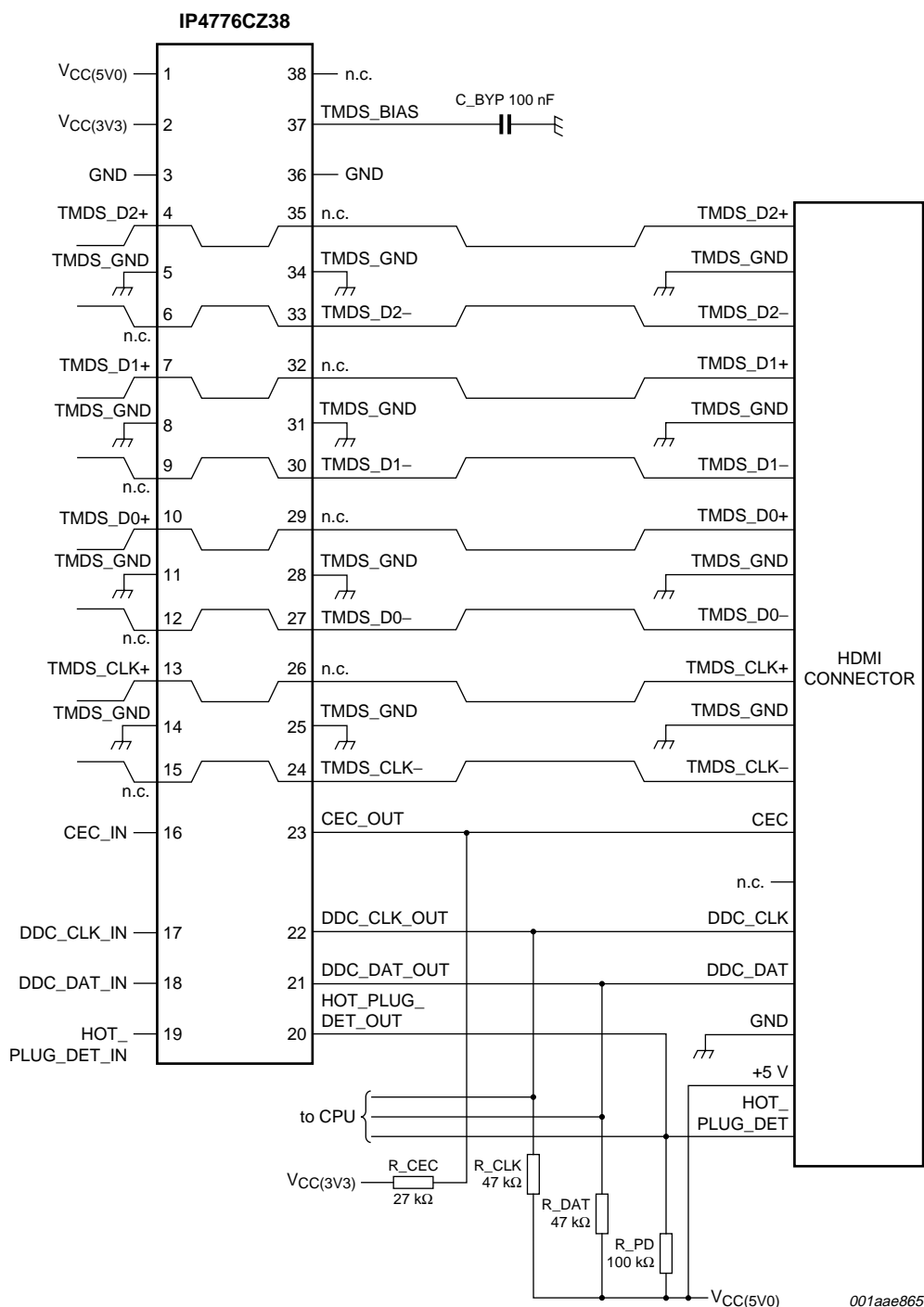
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CC(5V0)}$	supply current (5.0 V)	$V_{CC(5V0)} = 5.0\text{ V}$	100	110	130	$\mu$ A
$I_{CC(3V3)}$	supply current (3.3 V)	$V_{CC(3V3)} = 3.3\text{ V}$	-	1	5	$\mu$ A
$I_{bck(out-VCC5V0)}$	back current from output / TMDS pins to $V_{CC(5V0)}$	signal pins; powered down; $V_{CC(5V0)} < V_{O(ch)}$	[1]	-	0.1	$\mu$ A
$V_{BRzd}$	Zener diode breakdown voltage	$I = 1\text{ mA}$	6	-	9	V
$I_{L(r)}$	reverse leakage current	per TMDS channel; $V_I = 3.0\text{ V}$	-	-	1	$\mu$ A
$V_F$	forward voltage		-	0.7	-	V
$C_{ch(TMDS)}$	TMDS channel capacitance	$V_{CC(5V0)} = 5\text{ V}$ ; $f = 1\text{ MHz}$ ; $V_{bias} = 2.5\text{ V}$	[2]	-	0.7	pF

**Table 5. Characteristics ...continued**  
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta C_{ch(TMDS)}$	TMDS channel capacitance difference	$V_{CC(5V0)} = 5\text{ V}$ ; $f = 1\text{ MHz}$ ; $V_{bias} = 2.5\text{ V}$	[2] -	0.05	-	pF
$C_{ch(mutual)}$	mutual channel capacitance	between signal pin and pin n.c.; $V_{CC(5V0)} = 0\text{ V}$ ; $f = 1\text{ MHz}$ ; $V_{bias} = 2.5\text{ V}$	[2] -	0.07	-	pF
$C_{l(ch-GND)(levsh)}$	level shifting input capacitance from channel to ground	$V_{CC(5V0)} = 0\text{ V}$ ; $f = 1\text{ MHz}$ ; $V_{bias} = 2.5\text{ V}$	[2] -	4	6	pF
$R_{dyn}$	dynamic resistance	$I = 1\text{ A}$ ; IEC 61000-4-5/9				
		positive transient	-	2.4	-	$\Omega$
		negative transient	-	1.3	-	$\Omega$
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	$V_{ESD} = 8\text{ kV}$	[3] -	8	-	V
$\Delta V_{on}$	on-state voltage drop	$V_{CC(3V3)} = 2.5\text{ V}$ ; $V_S = \text{GND}$ ; $I_{DS} = 3\text{ mA}$	[4] -	85	140	mV

- [1] Signal pins:  
 TMDS\_D2+, TMDS\_D2-, TMDS\_D1+, TMDS\_D1-, TMDS\_D0+, TMDS\_D0-,  
 TMDS\_CLK+, TMDS\_CLK-,  
 CEC\_OUT,  
 DDC\_DAT\_OUT,  
 DDC\_CLK\_OUT,  
 HOT\_PLUG\_DET\_OUT.
- [2] This parameter is guaranteed by design.
- [3] This measurement is performed with an 0.1  $\mu\text{F}$  external capacitor on pin TMDS\_BIAS.
- [4] For level shifting N-FET.

## 10. Application information

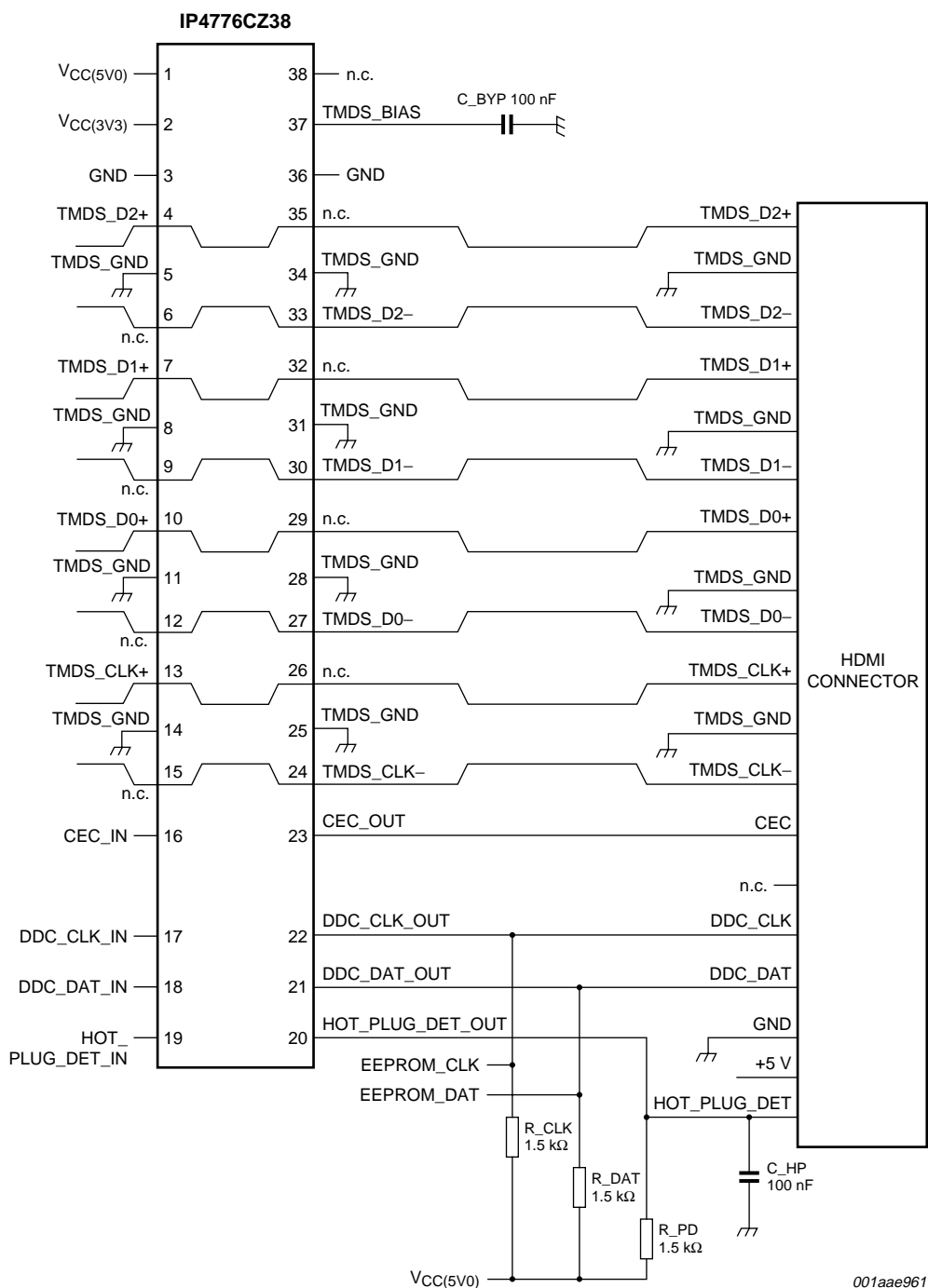


Use tapered tracks to connect adjacent TMDS+ and TMDS- pins with the opposite n.c. pins; see [Figure 5](#).

Use tapered tracks to connect adjacent TMDS+ and TMDS- pins with the HDMI connector; see [Figure 5](#).

Use tapered tracks to connect adjacent TMDS+ and TMDS- pins with the HDMI transmitter; see [Figure 5](#).

**Fig 3. HDMI transmitter application layout diagram**



Use tapered tracks to connect adjacent TMDS+ and TMDS- pins with the opposite n.c. pins; see [Figure 5](#).

Use tapered tracks to connect adjacent TMDS+ and TMDS- pins with the HDMI connector; see [Figure 5](#).

Use tapered tracks to connect adjacent TMDS+ and TMDS- pins with the HDMI receiver; see [Figure 5](#).

**Fig 4. HDMI receiver application layout diagram**



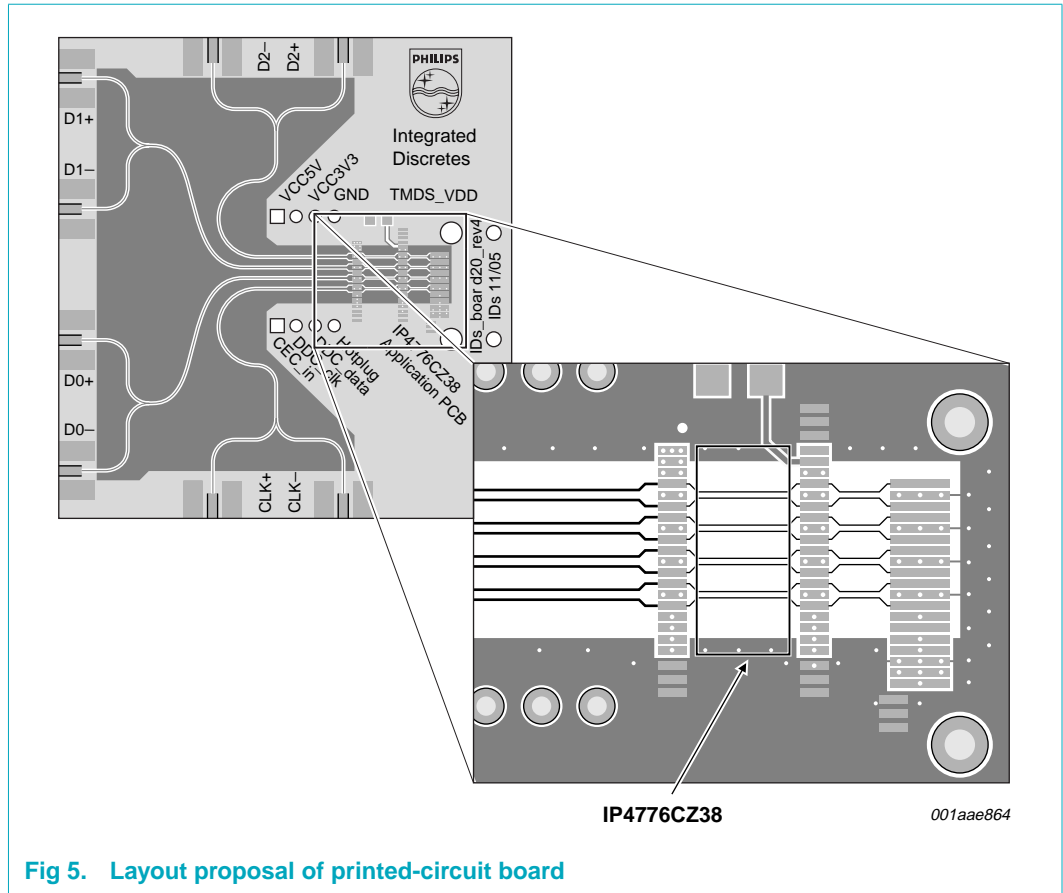


Fig 5. Layout proposal of printed-circuit board

11. Package outline

TSSOP38: plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm

SOT510-1

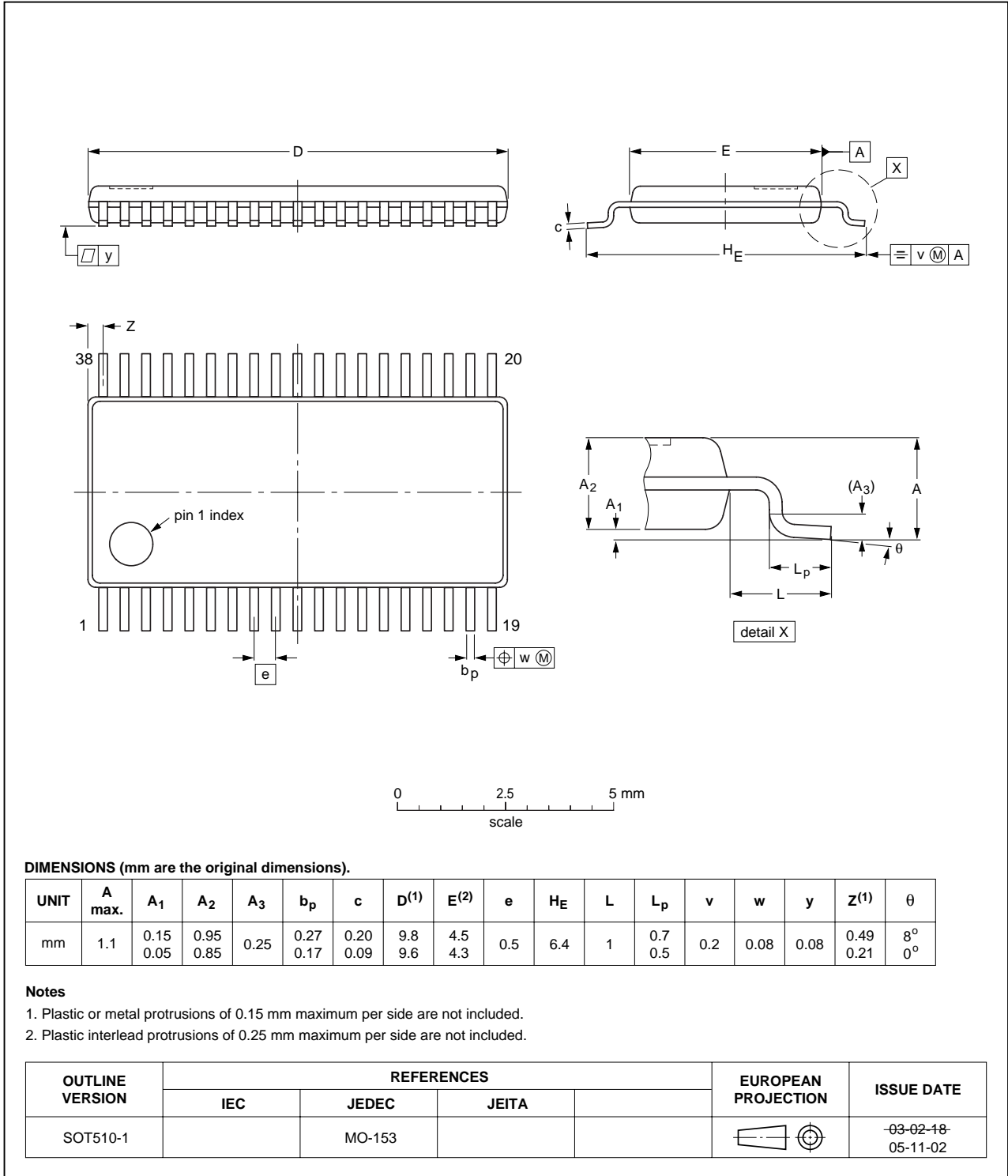


Fig 6. Package outline SOT510-1 (TSSOP38)

## 12. Abbreviations

**Table 6. Abbreviations**

Acronym	Description
CEC	Consumer Electronics Control
DDC	Data Display Channel
DVD	Digital Video Disk
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HDM	High-Definition Multimedia
HDMI	High-Definition Multimedia Interface
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
RoHS	Restriction of the use of certain Hazardous Substances
TMDS	Transition Minimized Differential Signaling

## 13. Revision history

**Table 7. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4776CZ38_1	20060714	Product data sheet	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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## Notes

## Notes

## Notes

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