

# MOSFET

## 500V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.



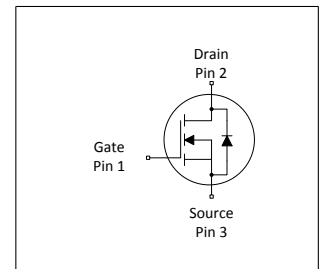
### Features

- Extremely low losses due to very low FOM  $R_{DS(on)} \cdot Q_g$  and  $E_{oss}$
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

### Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor lighting.

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	550	V
$R_{DS(on),max}$	0.65	$\Omega$
$I_D$	9	A
$Q_{g,typ}$	15	nC
$I_{D,pulse}$	19	A
$E_{oss} @ 400V$	1.69	$\mu J$

Type / Ordering Code	Package	Marking	Related Links
IPA50R650CE	PG-TO 220 FullPAK	5R650CE	see Appendix A

## Table of Contents

Description .....	1
Maximum ratings .....	3
Thermal characteristics .....	3
Electrical characteristics .....	4
Electrical characteristics diagrams .....	6
Test Circuits .....	10
Package Outlines .....	11
Appendix A .....	12
Revision History .....	13
Trademarks .....	13
Disclaimer .....	13

## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	9 5.7	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	19	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	102	mJ	$I_D=2.3\text{A}$ ; $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	$E_{AR}$	-	-	0.15	mJ	$I_D=2.3\text{A}$ ; $V_{DD} = 50\text{V}$
Avalanche current, repetitive	$I_{AR}$	-	-	2.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0\dots 400\text{V}$
Gate source voltage	$V_{GS}$	-20 -30	-	20 30	V	static; AC ( $f > 1\text{ Hz}$ )
Power dissipation (Full PAK)	$P_{tot}$	-	-	27.2	W	$T_C=25^\circ\text{C}$
Operating and storage temperature	$T_j, T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	$I_S$	-	-	4.0	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	19.0	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	15	V/ns	$V_{DS} = 0\dots 400\text{V}$ , $I_{SD} \leq I_S$ , $T_j=25^\circ\text{C}$
Maximum diode commutation speed <sup>3)</sup>	di/dt	-	-	500	A/ $\mu\text{s}$	$V_{DS} = 0\dots 400\text{V}$ , $I_{SD} \leq I_S$ , $T_j=25^\circ\text{C}$
Insulation withstand voltage for TO-220 FullPAK	$V_{ISO}$	-	-	2500	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

## 2 Thermal characteristics

**Table 3 Thermal characteristics TO220 Full PAK**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	4.6	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	80	$^\circ\text{C/W}$	leaded
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	$^\circ\text{C}$	1.6mm (0.063 in.) from case for 10s

<sup>1)</sup> Limited by  $T_{j,max} < 150^\circ\text{C}$ , Maximum Duty Cycle  $D = 0.5$ , TO220 equivalent

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup>  $V_{DClink}=400\text{V}$ ;  $V_{DS,peak} < V_{(BR)DSS}$ ; identical low side and high side switch with identical  $R_G$

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	$V_{DS}=V_{GS}, I_D=0.15mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=500V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=500V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.59	0.65	$\Omega$	$V_{GS}=13V, I_D=1.8A, T_j=25^\circ C$ $V_{GS}=13V, I_D=1.8A, T_j=150^\circ C$
Gate resistance	$R_G$	-	3	-	$\Omega$	$f=1\text{ MHz, open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	342	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Output capacitance	$C_{oss}$	-	26	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	21	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	80	-	pF	$I_D=constant, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	6	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3\Omega$
Rise time	$t_r$	-	5	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3\Omega$
Turn-off delay time	$t_{d(off)}$	-	27	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3\Omega$
Fall time	$t_f$	-	13	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3\Omega$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	1.8	-	nC	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$
Gate to drain charge	$Q_{gd}$	-	8.1	-	nC	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$
Gate charge total	$Q_g$	-	15	-	nC	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$

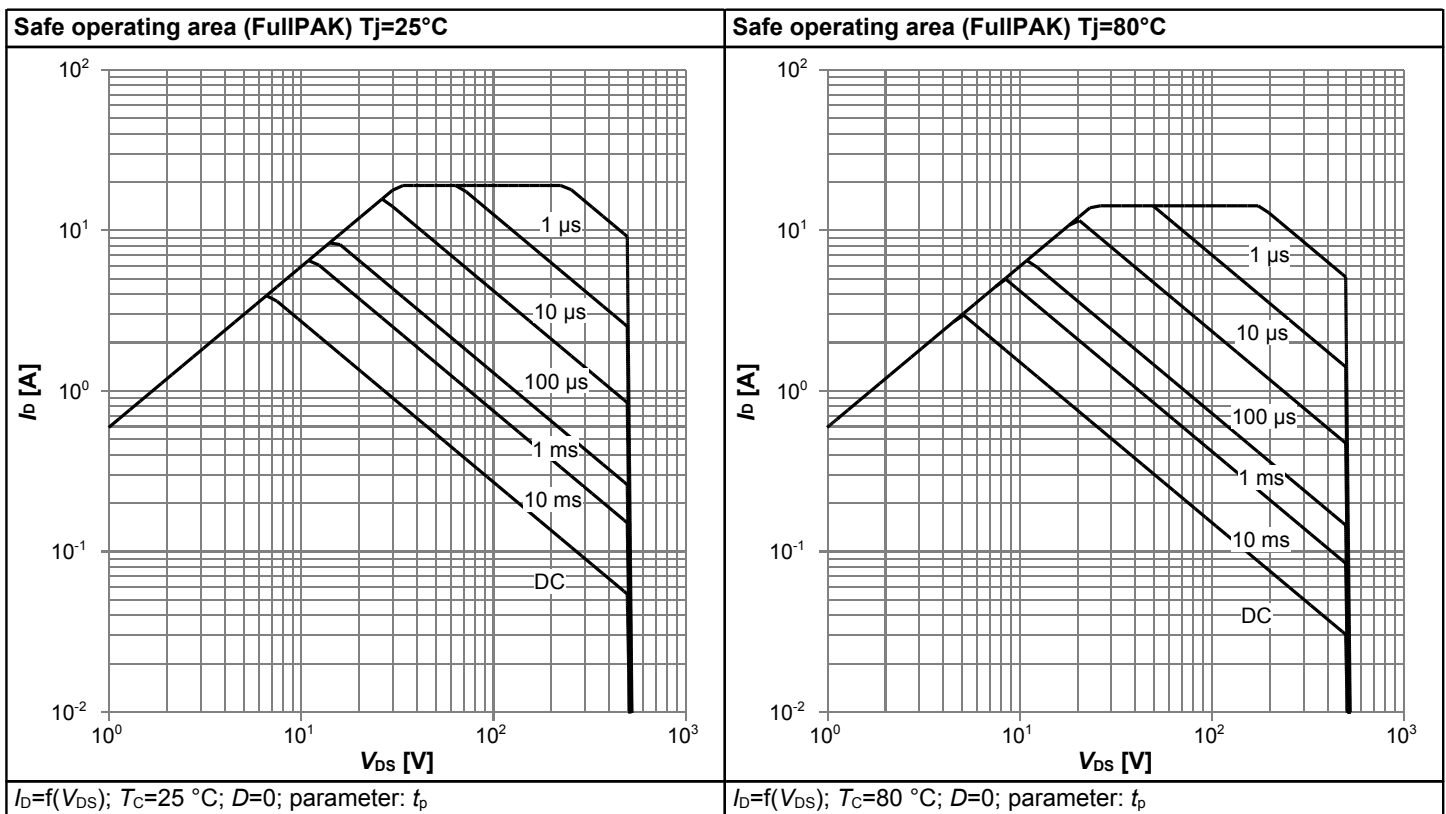
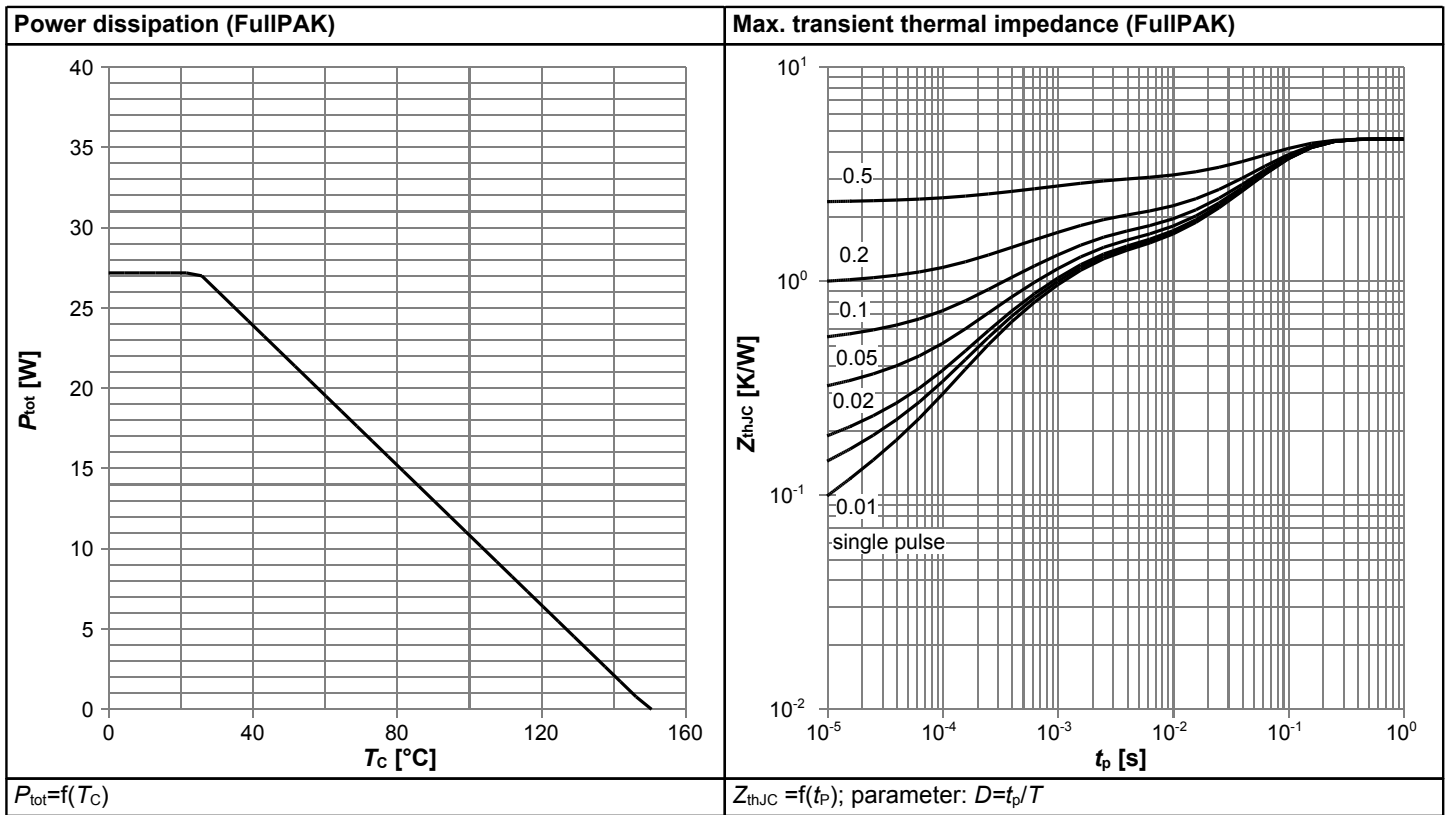
<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

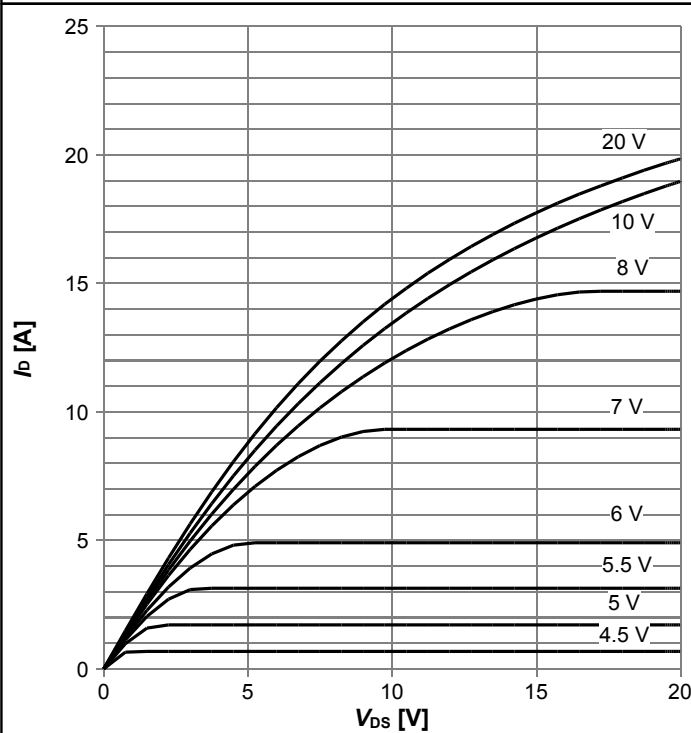
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.84	-	V	$V_{GS}=0V, I_F=2.3A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	162	-	ns	$V_R=400V, I_F=2.3A, di_F/dt=100A/\mu s$
Reverse recovery charge	$Q_{rr}$	-	1	-	$\mu C$	$V_R=400V, I_F=2.3A, di_F/dt=100A/\mu s$
Peak reverse recovery current	$I_{rrm}$	-	11.1	-	A	$V_R=400V, I_F=2.3A, di_F/dt=100A/\mu s$

### 4 Electrical characteristics diagrams

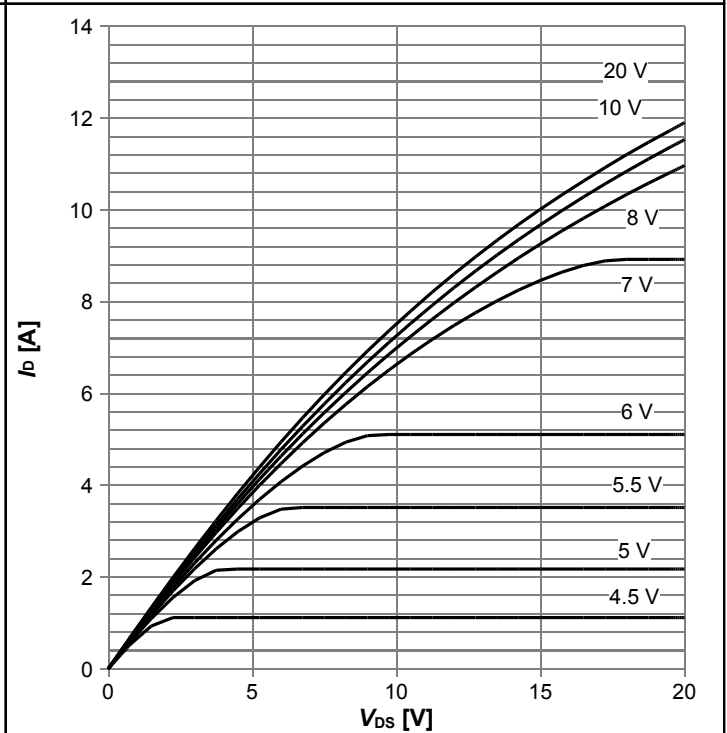


Typ. output characteristics  $T_j=25^\circ\text{C}$



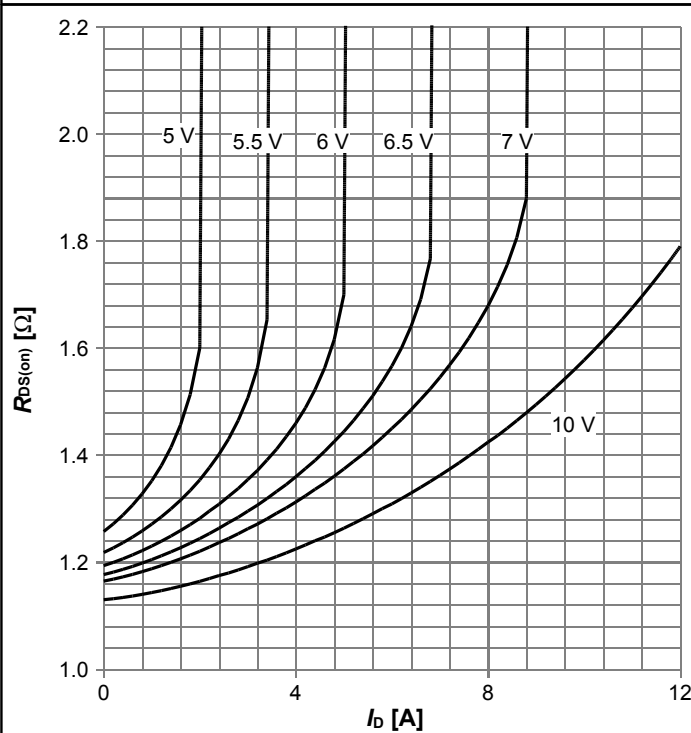
$I_D=f(V_{DS})$ ;  $T_j=25^\circ\text{C}$ ; parameter:  $V_{GS}$

Typ. output characteristics  $T_j=125^\circ\text{C}$



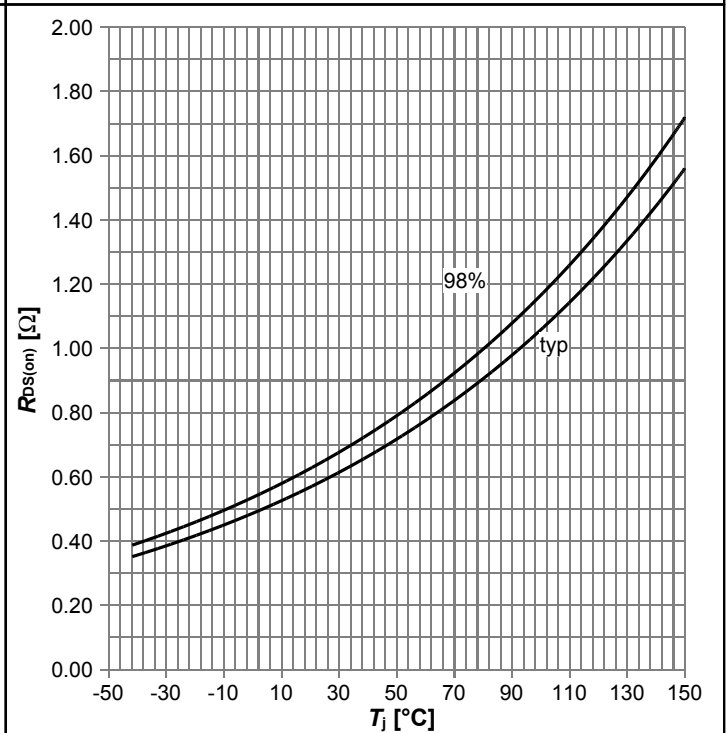
$I_D=f(V_{DS})$ ;  $T_j=125^\circ\text{C}$ ; parameter:  $V_{GS}$

Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D)$ ;  $T_j=125^\circ\text{C}$ ; parameter:  $V_{GS}$

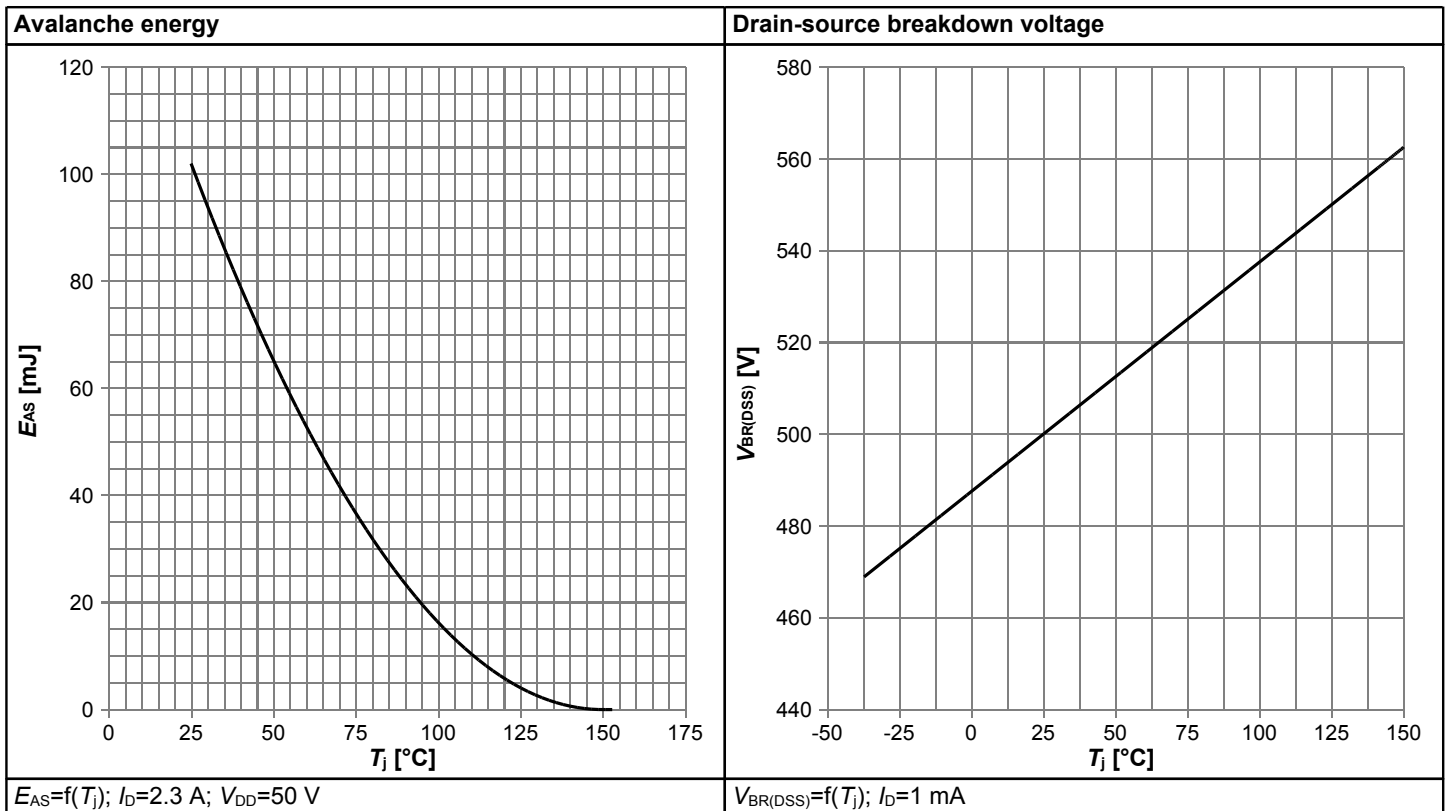
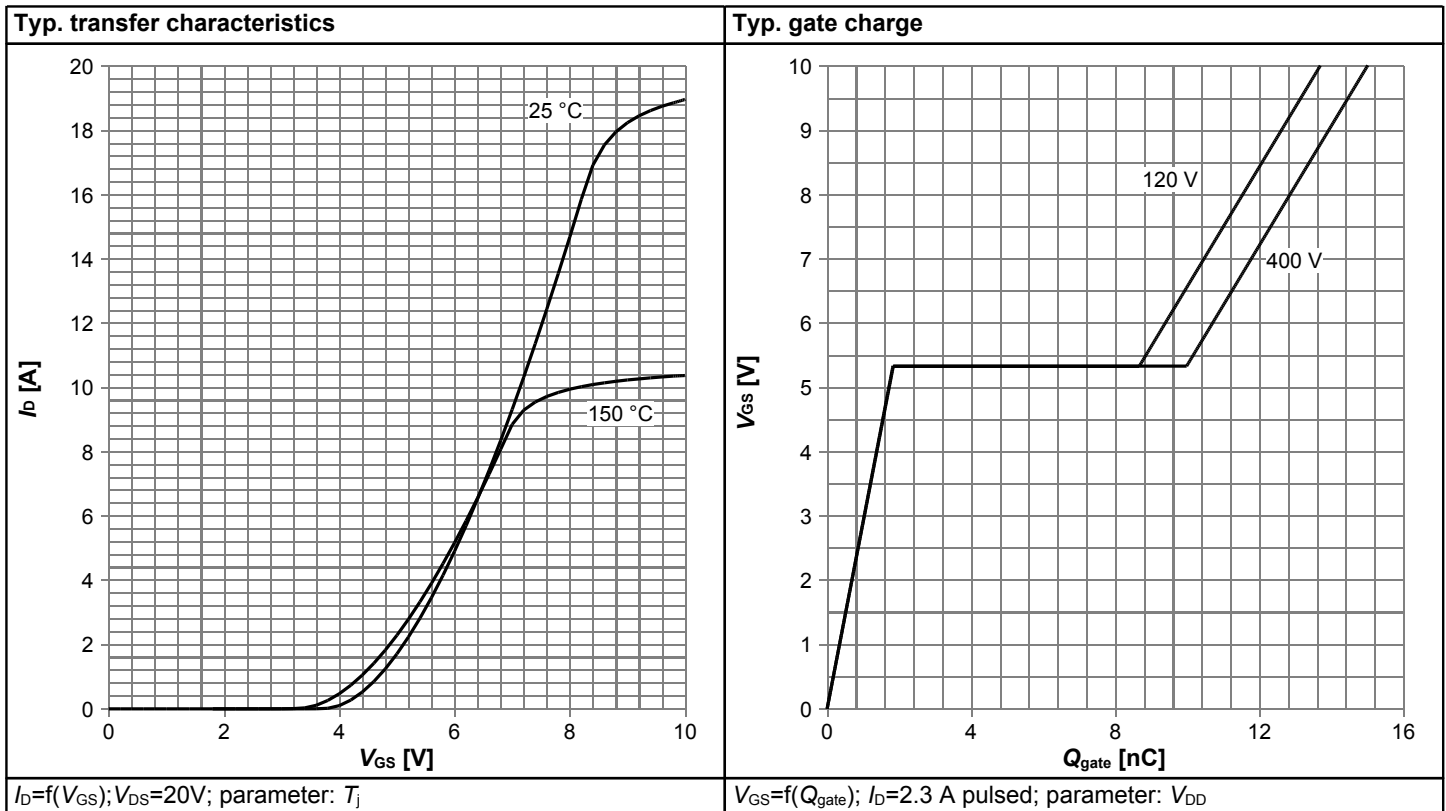
Drain-source on-state resistance



$R_{DS(on)}=f(T_j)$ ;  $I_D=1.8\text{ A}$ ;  $V_{GS}=13\text{ V}$

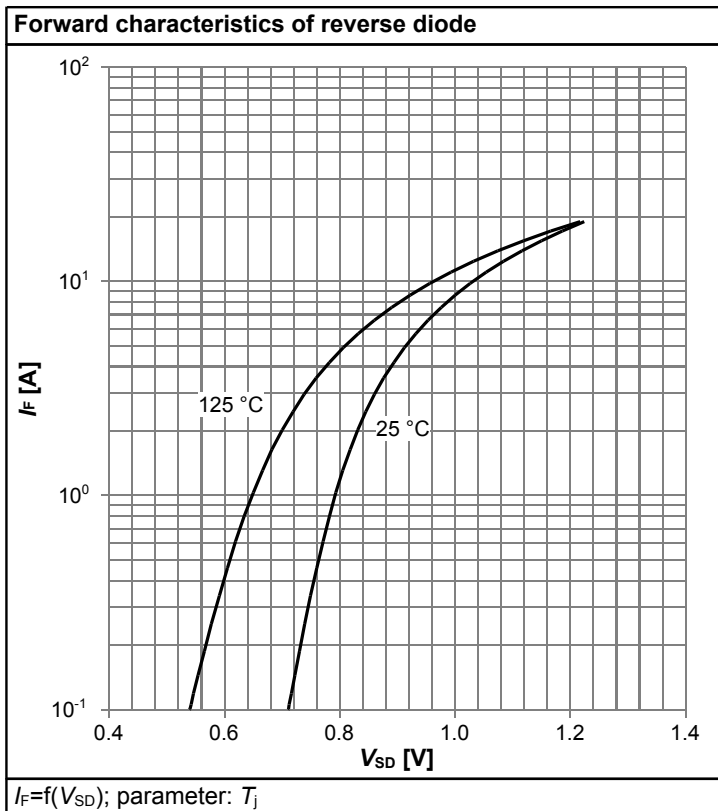
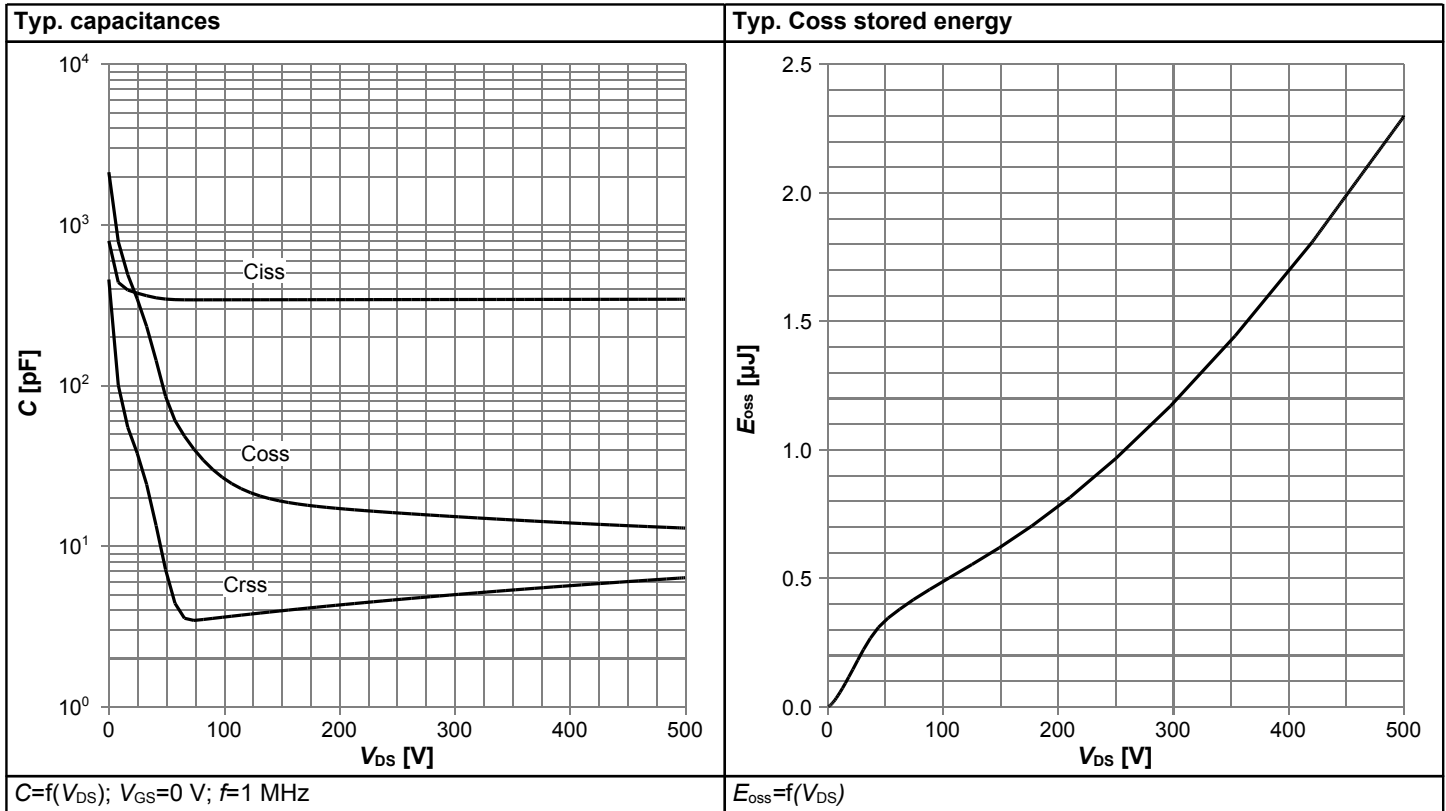
# 500V CoolMOS™ CE Power Transistor

## IPA50R650CE





**500V CoolMOS™ CE Power Transistor**  
**IPA50R650CE**



## 5 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform

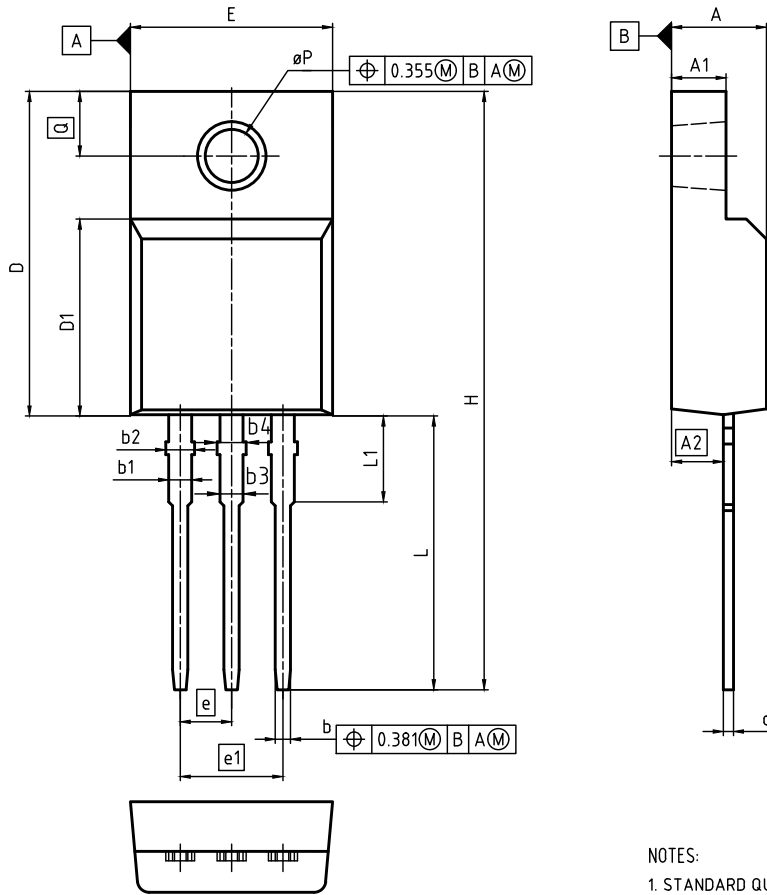
**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform

## 6 Package Outlines



**NOTES:**

1. STANDARD QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281 NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.80	0.092	0.110
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	1.20	1.50	0.047	0.059
b3	0.65	1.38	0.026	0.054
b4	1.20	1.50	0.047	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
$\phi P$	3.00	3.38	0.118	0.133
Q	3.15	3.50	0.124	0.138

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**Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches**

## **7 Appendix A**

### **Table 11 Related Links**

- **IFX CoolMOS Webpage:** [www.infineon.com](http://www.infineon.com)
- **IFX Design tools:** [www.infineon.com](http://www.infineon.com)

## Revision History

IPA50R650CE

**Revision: 2016-07-12, Rev. 2.3**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2012-08-24	Release of final version
2.1	2014-06-12	Release of final datasheet
2.2	2016-06-13	Updated ID ratings, package marking code & package drawing
2.3	2016-07-12	Changed marking information in page 1

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