OptiMOS®2 Power-Transistor

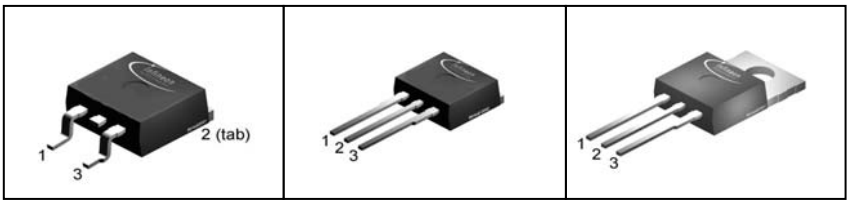
Features

- Ideal for high-frequency dc/dc converters
- Qualified according to JEDEC[1] for target applications
- N-channel - Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 175 °C operating temperature
- dv/dt rated

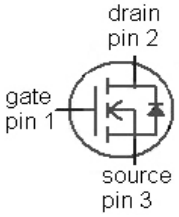
Product Summary

V_{DS}	25	V
$R_{DS(on),max}$ (SMD version)	3.9	mΩ
I_D	80	A

P-TO263-3-2 P-TO262-3-1 P-TO220-3-1



Type	Package	Ordering Code	Marking
IPB04N03LA	P-TO263-3-2	Q67042-S4181	04N03LA
IPI04N03LA	P-TO262-3-1	Q67042-S4183	04N03LA
IPP04N03LA	P-TO220-3-1	Q67042-S4182	04N03LA



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2]	80	A
		T_C=100 °C	80	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C[3]	385	
Avalanche energy, single pulse	E_{AS}	I_D=77 A, R_{GS}=25 Ω	290	mJ
Reverse diode dv/dt	dv/dt	I_D=80 A, V_{DS}=20 V, di/dt=200 A/µs, $T_{j,max}$=175 °C	6	kV/µs
Gate source voltage[4]	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	107	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1] J-STD20 and JESD22

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.4	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[5)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=60 µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=25 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=25 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=55 A	-	5.4	6.7	mΩ
		V_{GS}=4.5 V, I_D=55 A, SMD version	-	5.1	6.4	
		V_{GS}=10 V, I_D=55 A	-	3.5	4.2	
		V_{GS}=10 V, I_D=55 A, SMD version	-	3.2	3.9	
Gate resistance	R_G		-	1.1	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=55 A	43	85	-	S

[2)] Current is limited by bondwire; with an R_{thJC}=1.4 K/W the chip is able to carry 125 A.

[3)] See figure 3

[4)] $T_{j,max}$=150 °C and duty cycle D<0.25 for V_{GS}<-5 V

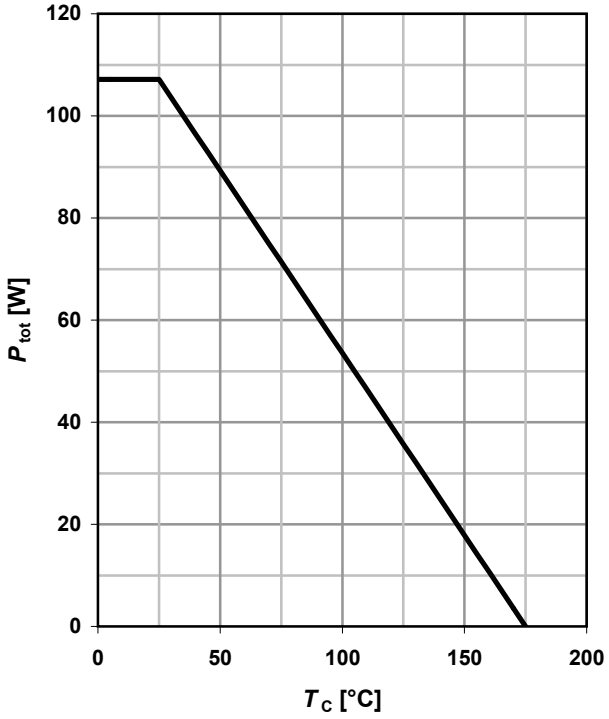
[5)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	2915	3877	pF
Output capacitance	C_{oss}		-	1236	1643	
Reverse transfer capacitance	C_{rss}		-	175	263	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=20 A, R_G=2.7 Ω	-	13	19	ns
Rise time	t_r		-	4.5	7.0	
Turn-off delay time	$t_{d(off)}$		-	38	57	
Fall time	t_f		-	5.4	8.1	
Gate Charge Characteristics[6)]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=40 A, V_{GS}=0 to 5 V	-	10	13	nC
Gate charge at threshold	$Q_{g(th)}$		-	4.6	6.2	
Gate to drain charge	Q_{gd}		-	7.2	11	
Switching charge	Q_{sw}		-	12	17	
Gate charge total	Q_g		-	24	32	
Gate plateau voltage	$V_{plateau}$		-	3.3	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 5 V	-	20	27	nC
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	27	35	
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	80	A
Diode pulse current	$I_{S,pulse}$		-	-	385	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=80 A, T_j=25 °C	-	0.96	1.2	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	-	15	nC

[6)] See figure 16 for gate charge parameter definition

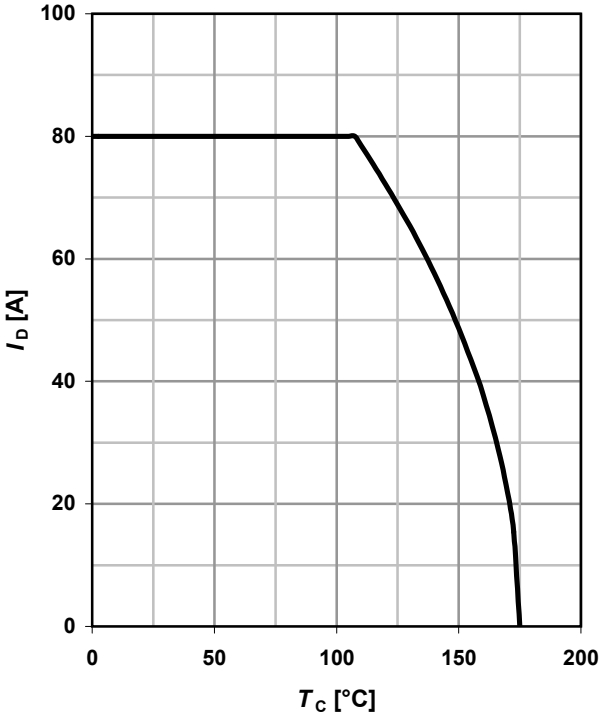
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

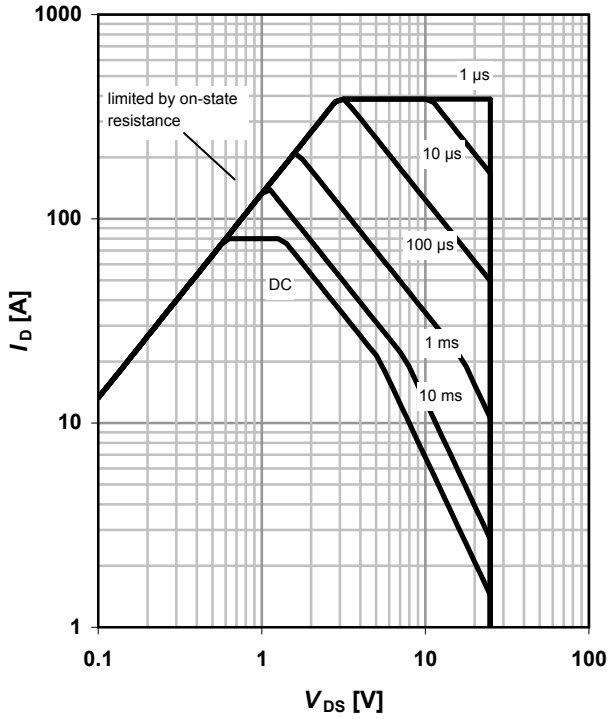
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operation area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

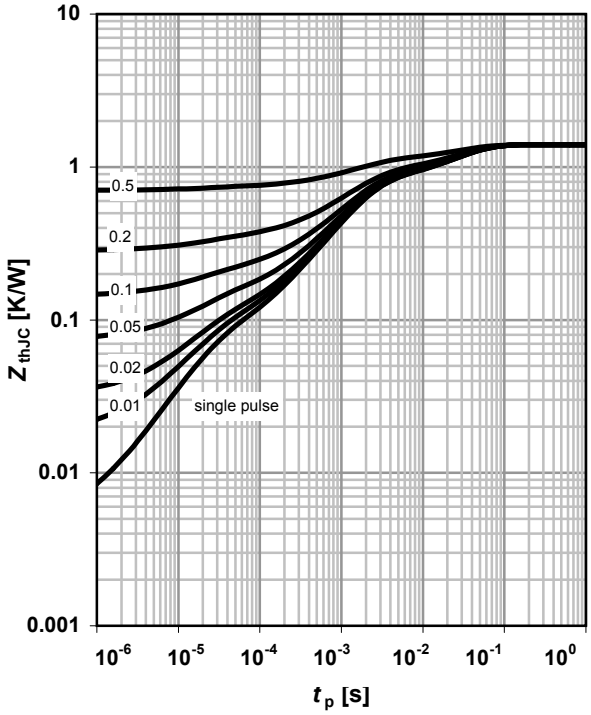
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

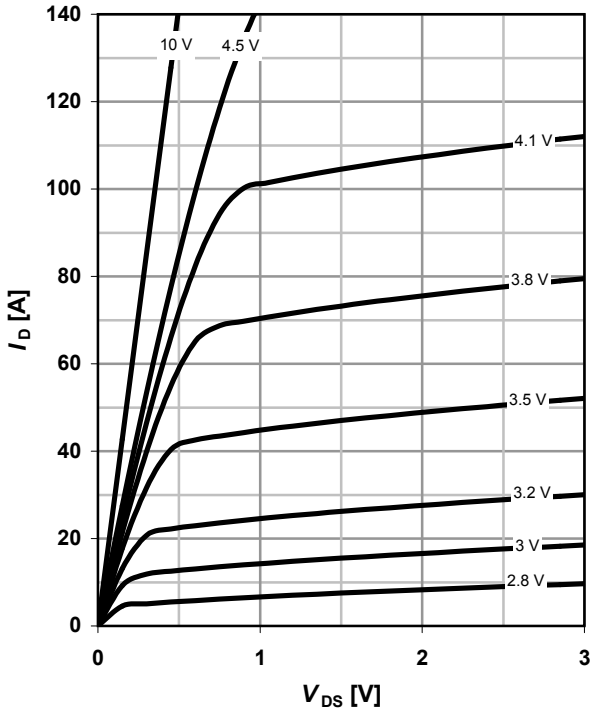
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

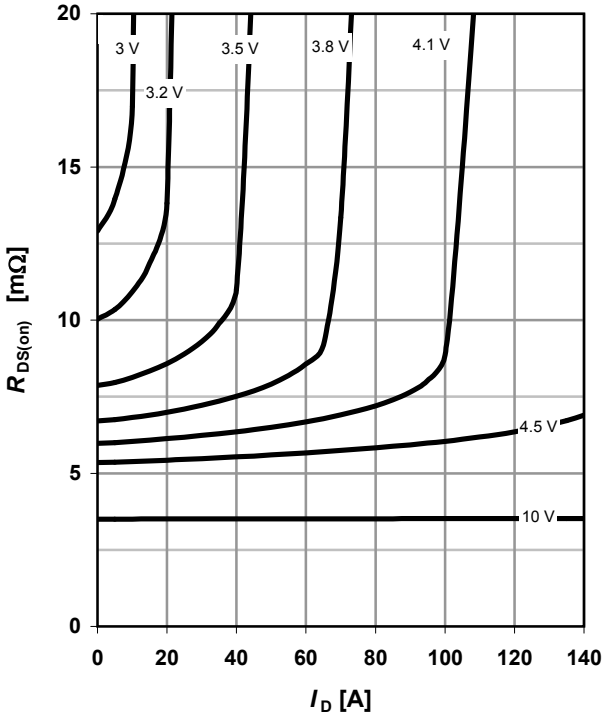
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

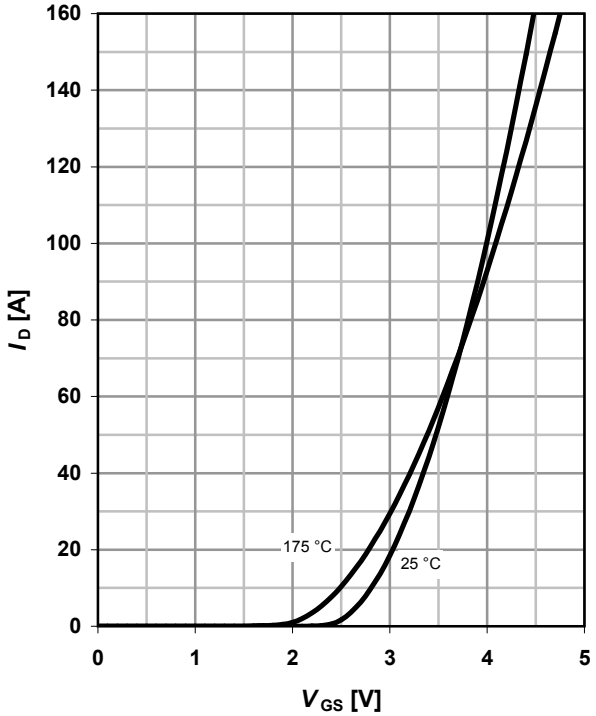
parameter: V_{GS}



7 Typ. transfer characteristics

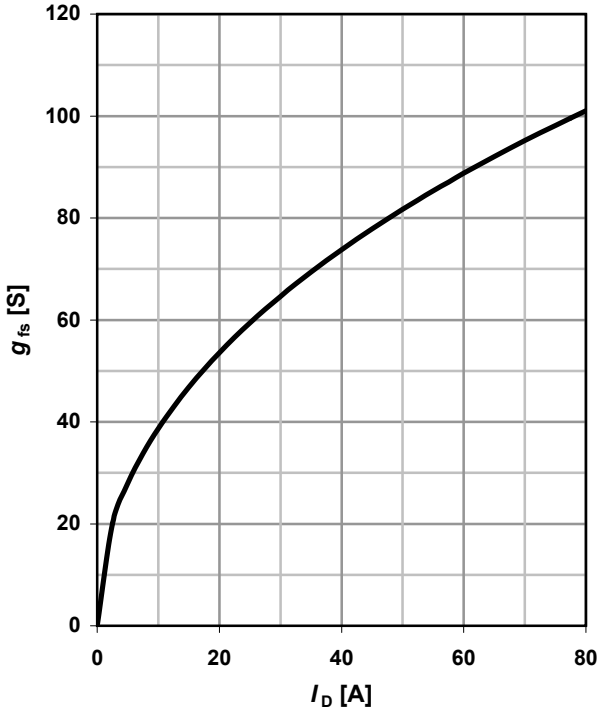
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



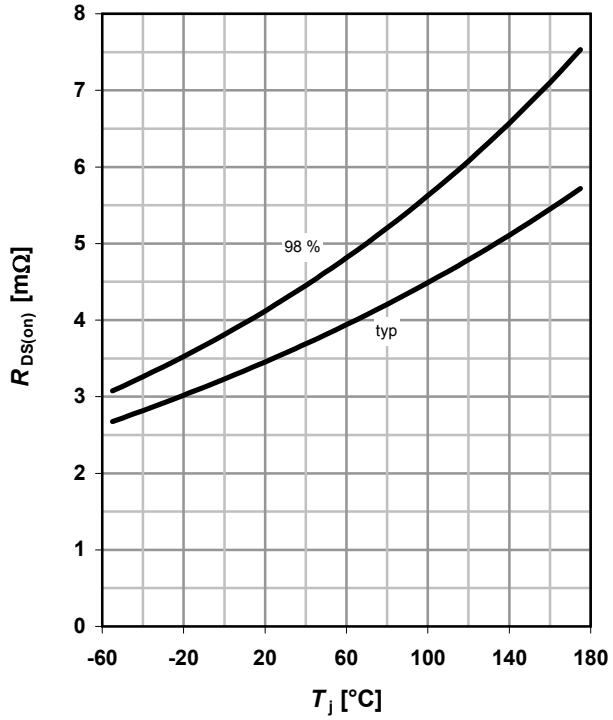
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

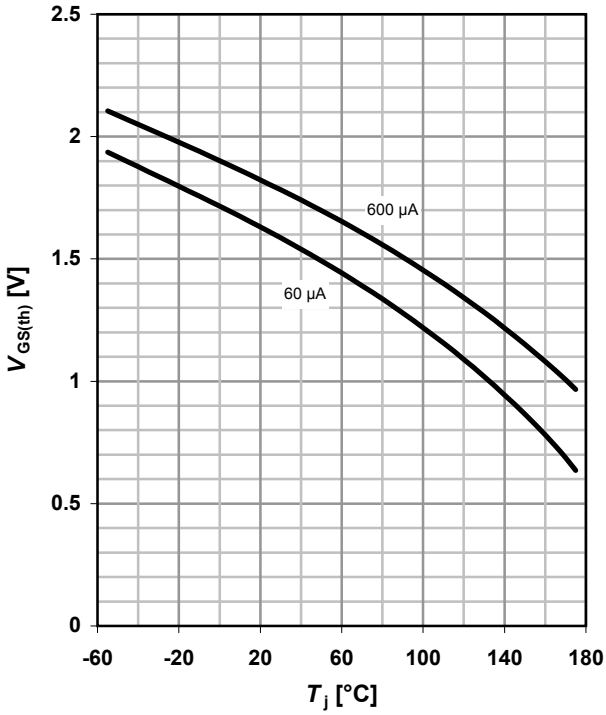
$R_{DS(on)}=f(T_j)$; $I_D=55$ A; $V_{GS}=10$ V



10 Typ. gate threshold voltage

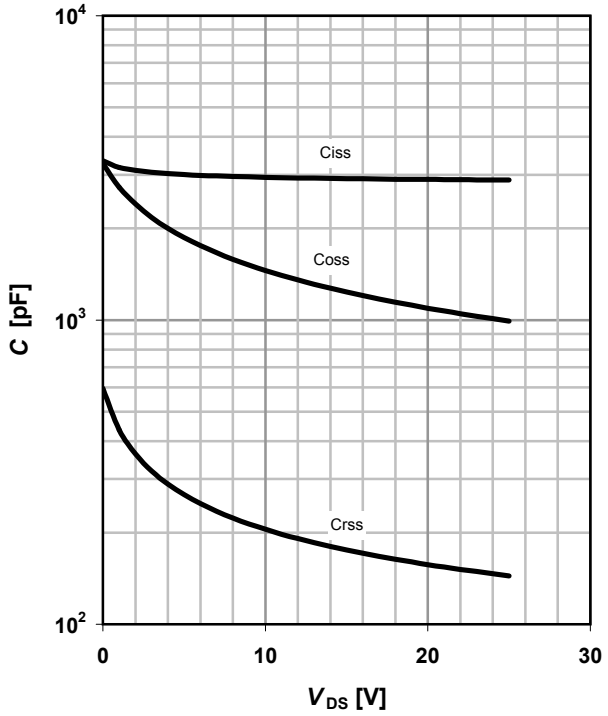
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

parameter: I_D



11 Typ. capacitances

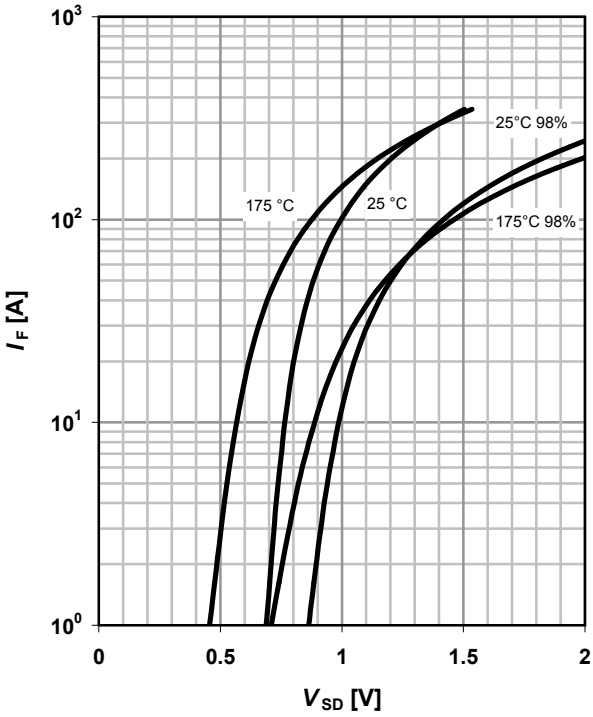
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

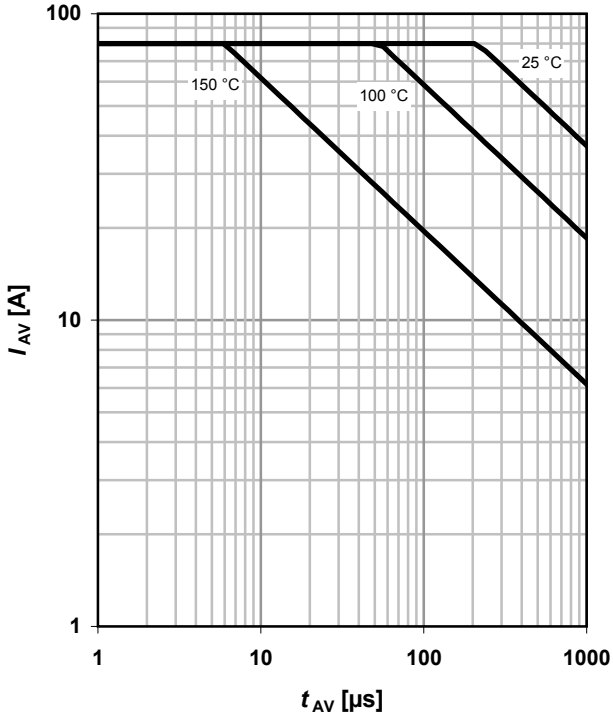
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

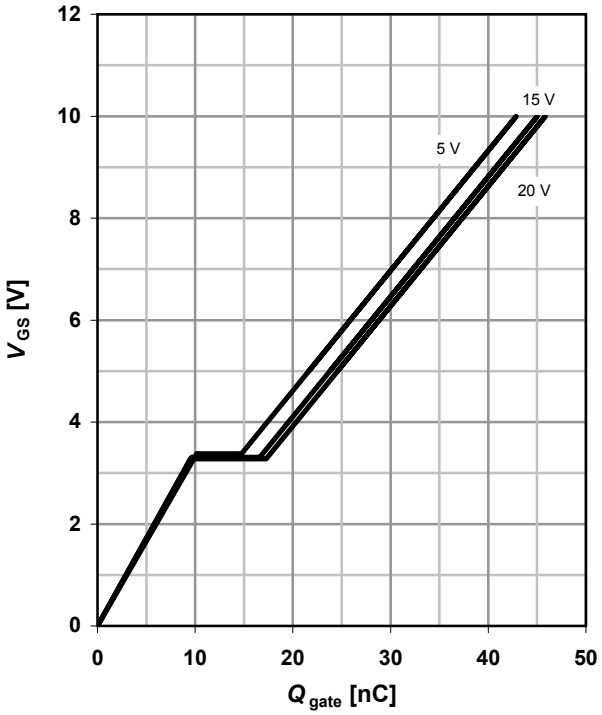
parameter: $T_{j(start)}$



14 Typ. gate charge

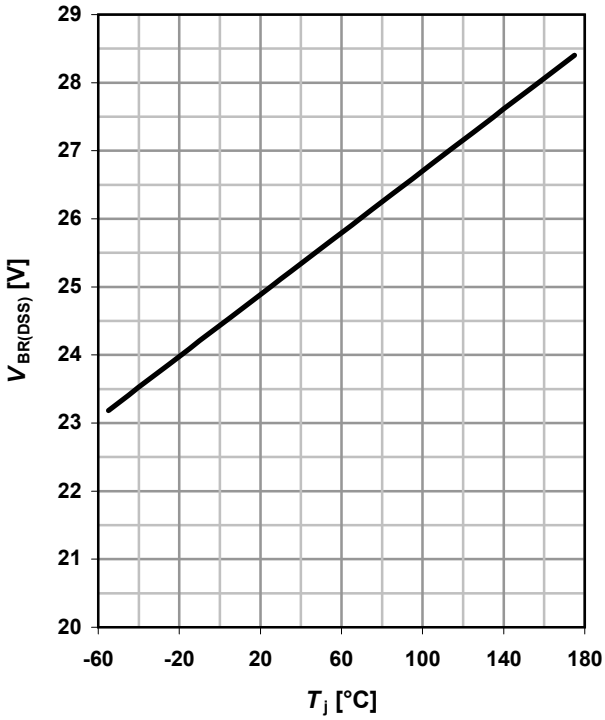
V_{GS}=f(Q_{gate}); I_D=40 A pulsed

parameter: V_{DD}

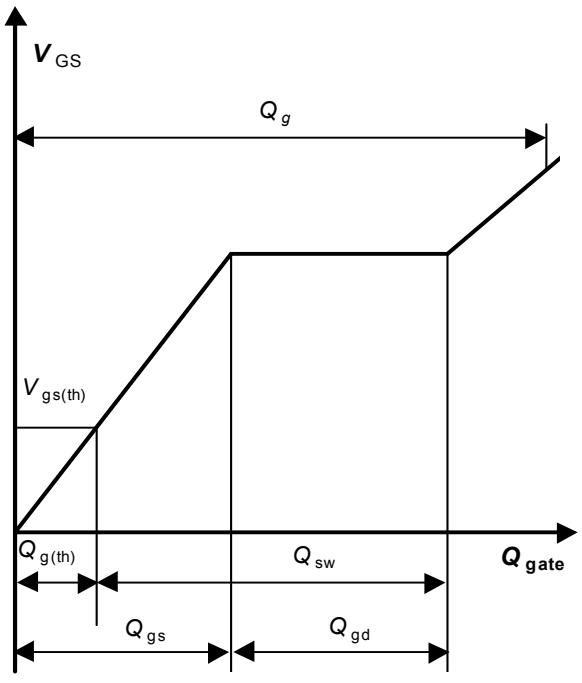


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

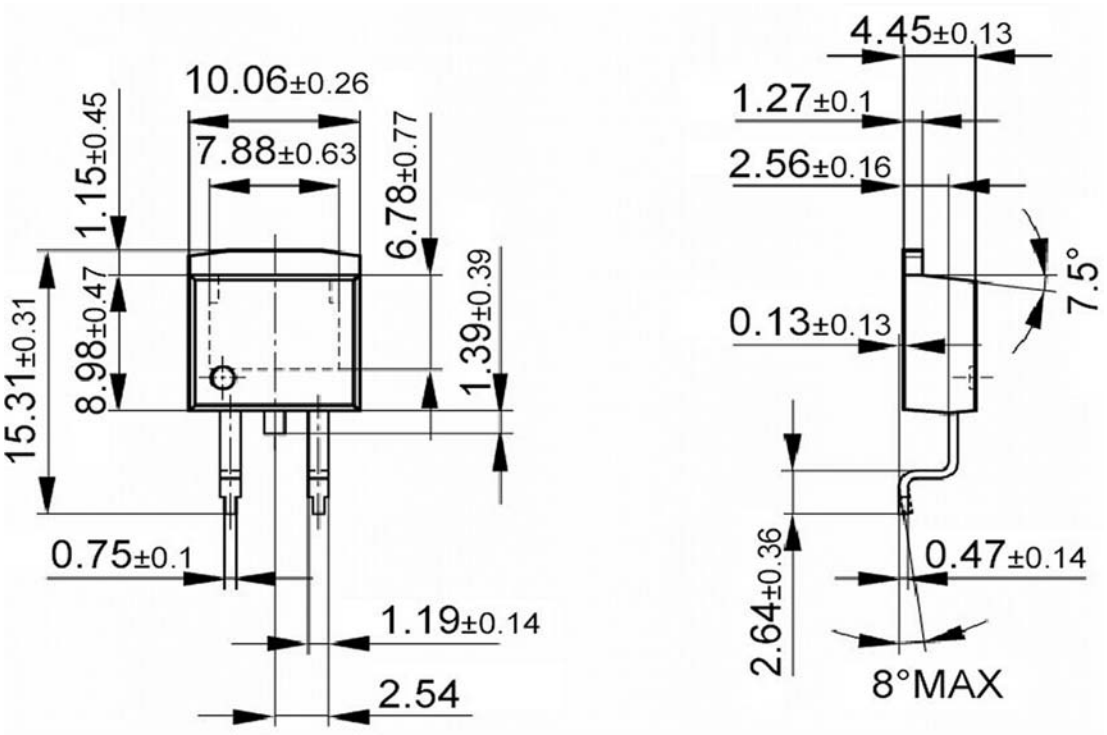


16 Gate charge waveforms

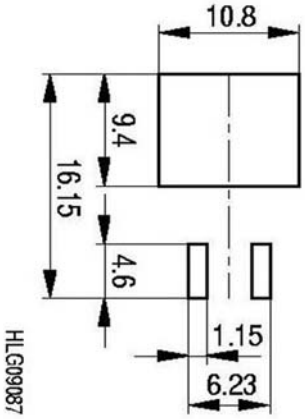


Package Outline

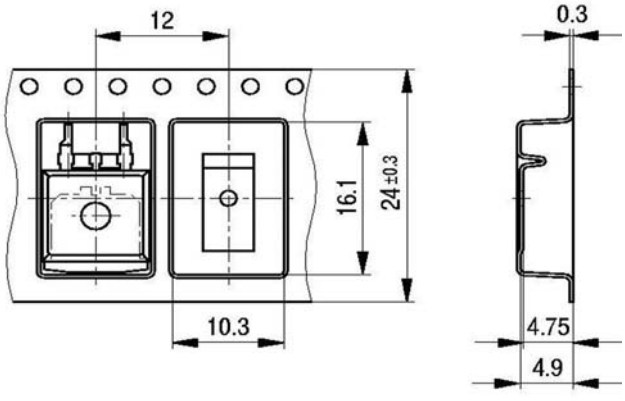
P-TO263-3-2: Outline



Footprint

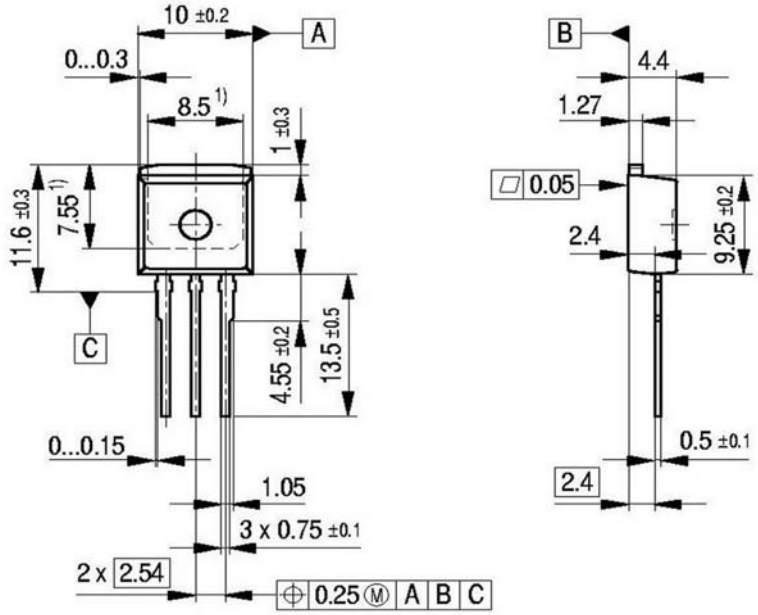


Packaging



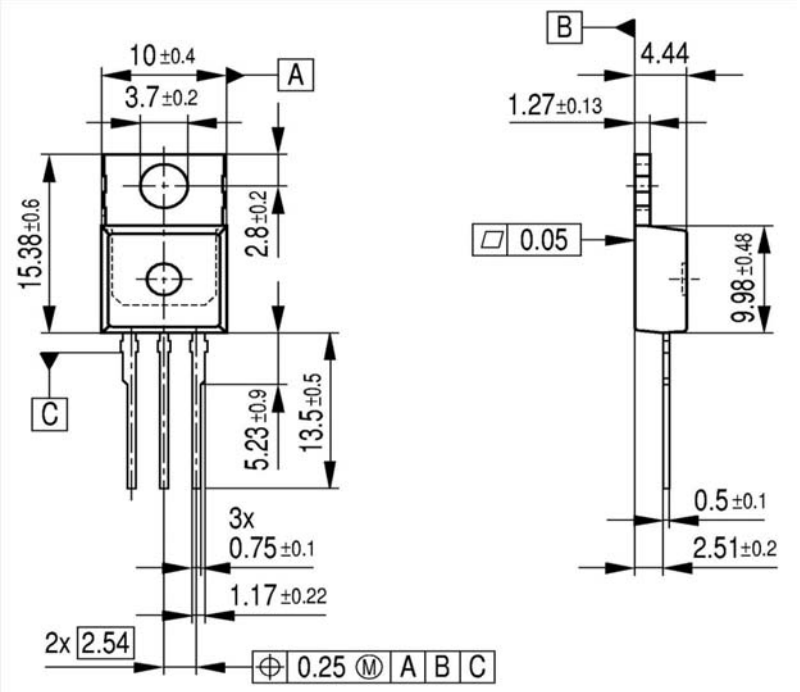
Dimensions in mm

P-TO262-3-1: Outline



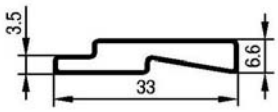
1) Typical
Metal surface min. X = 7.25, Y = 6.9
All metal surfaces tin plated, except area of cut.

P-TO220-3-1: Outline



All metal surfaces tin plated, except area of cut.
Metal surface min. x=7.25, y=12.3

Packaging



Dimensions in mm

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