

OptiMOS[®] -P2 Power-Transistor



Product Summary

V_{DS}	-40	V
$R_{DS(on),max}$	2.4	mΩ
I_D	-180	A

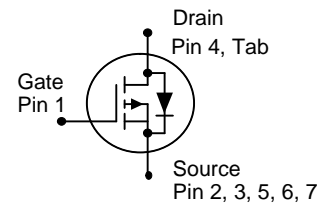
Features

- P-channel - Logic Level - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested
- Intended for reverse battery protection

PG-TO263-7-3



Type	Package	Marking
IPB180P04P4L-02	PG-TO263-7-3	4QP04L02



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$, $V_{GS}=-10\text{V}^{(1)}$	-180	A
		$T_C=100\text{ °C}$, $V_{GS}=-10\text{V}^{(2)}$	-140	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	-720	
Avalanche energy, single pulse	E_{AS}	$I_D= -90\text{A}$	84	mJ
Avalanche current, single pulse	I_{AS}	-	-180	A
Gate source voltage	V_{GS}	-	$\pm 16^{(3)}$	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	150	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	1	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ⁴⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D = -1mA$	-40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-410\mu A$	-1.2	-1.7	-2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-32V, V_{GS}=0V, T_j=25\text{ °C}$	-	-0.1	-1	μA
		$V_{DS}=-32V, V_{GS}=0V, T_j=125\text{ °C}^{2)}$	-	-20	-200	
Gate-source leakage current	I_{GSS}	$V_{GS}=-16V, V_{DS}=0V$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-100A$	-	2.6	3.9	m Ω
		$V_{GS}=-10V, I_D=-100A$	-	1.8	2.4	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=-25V,$ $f=1MHz$	-	14400	18700	pF
Output capacitance	C_{oss}		-	4570	5900	
Reverse transfer capacitance	C_{rss}		-	180	360	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-20V,$ $V_{GS}=-10V, I_D=-180A,$ $R_G=3.5\Omega$	-	32	-	ns
Rise time	t_r		-	28	-	
Turn-off delay time	$t_{d(off)}$		-	146	-	
Fall time	t_f		-	119	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=-32V,$ $I_D=-180A,$ $V_{GS}=0 \text{ to } -10V$	-	50	65	nC
Gate to drain charge	Q_{gd}		-	38	76	
Gate charge total	Q_g		-	220	286	
Gate plateau voltage	$V_{plateau}$		-	-3.5	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	-180	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	-720	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=-100A,$ $T_j=25^\circ C$	-	-1.0	-1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=-20V, I_F=-50A,$ $di_F/dt=-100A/\mu s$	-	71	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	101	-	nC

¹⁾ Current is limited by bondwire; with an $R_{thJC} = 1K/W$ the chip is able to carry 200A at 25°C.

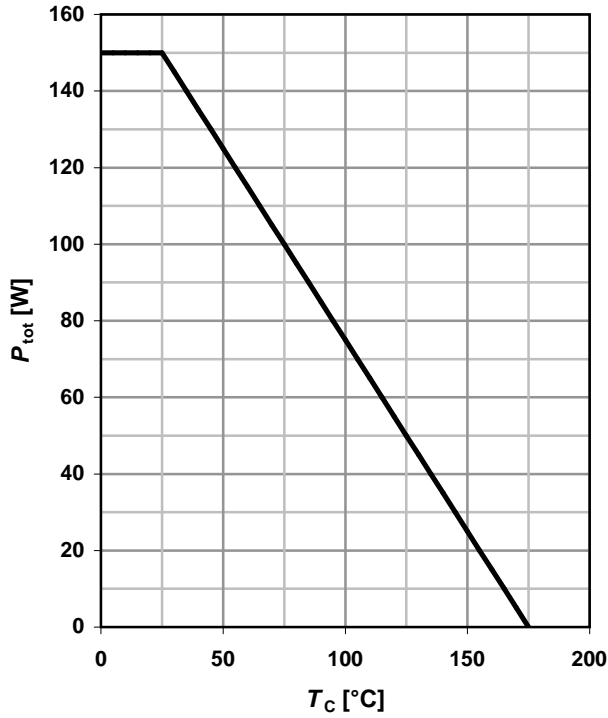
²⁾ Specified by design. Not subject to production test.

³⁾ $V_{GS}=+5V/-16V$ according AEC; $V_{GS}=+16V$ for max 168h at $T_j=175^\circ C$

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

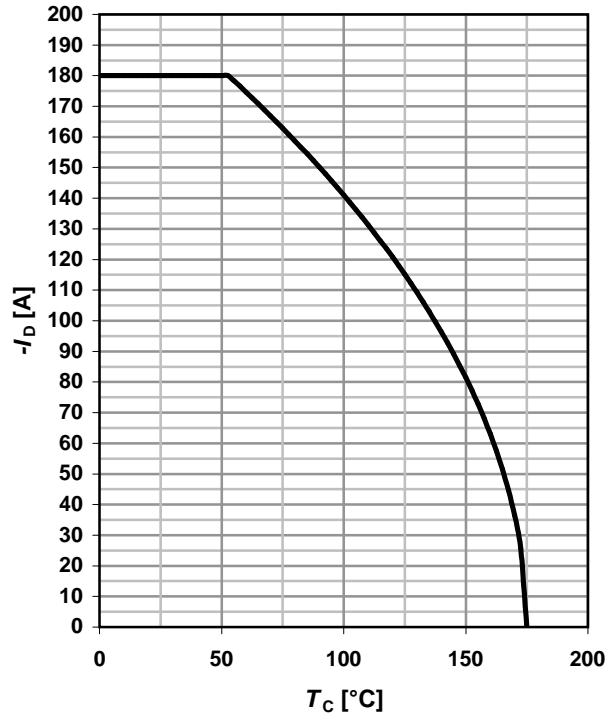
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \leq -6V$



2 Drain current

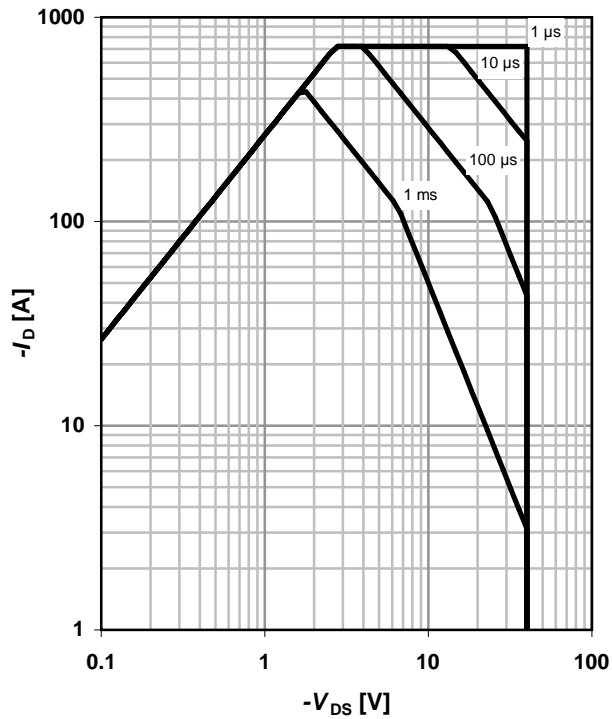
$I_D = f(T_C); V_{GS} \leq -6V$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

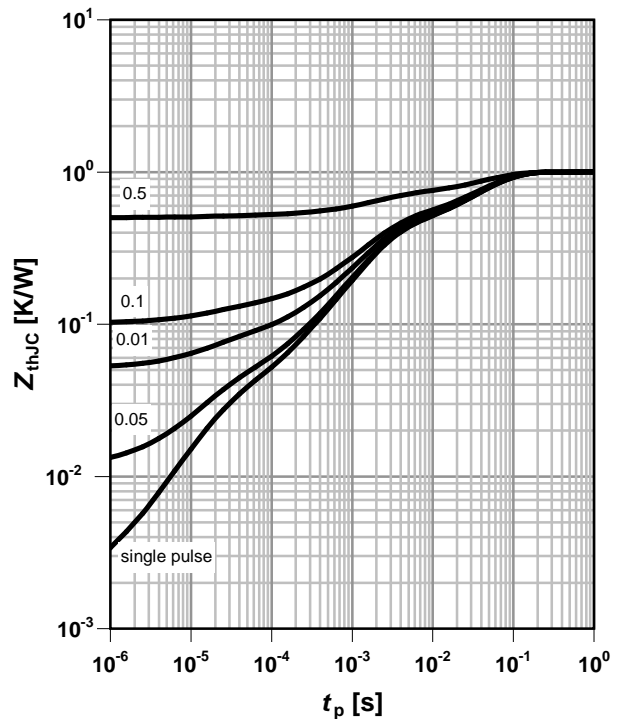
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

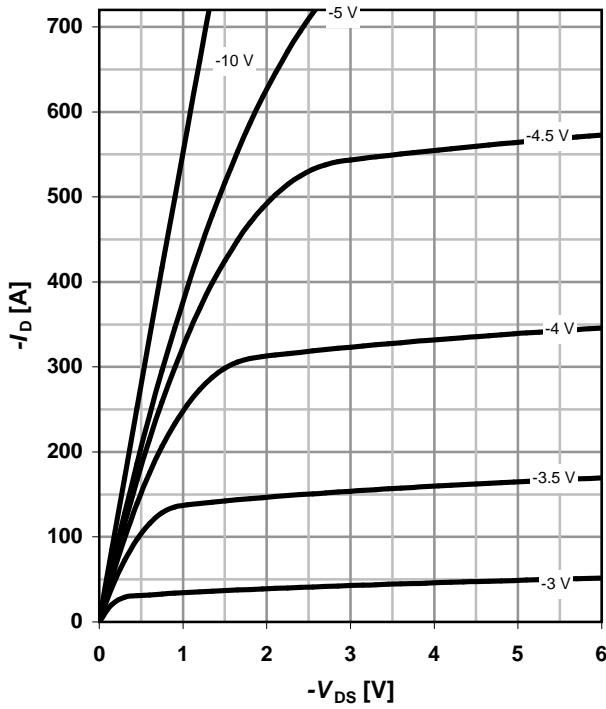
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

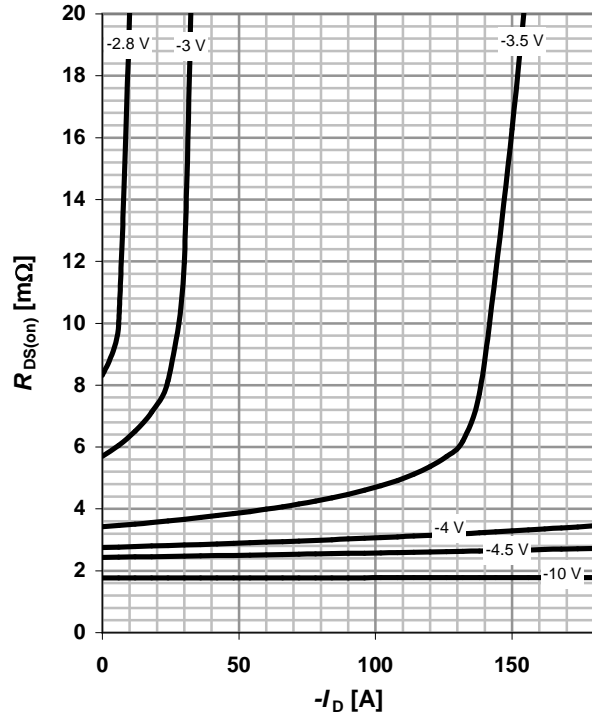
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

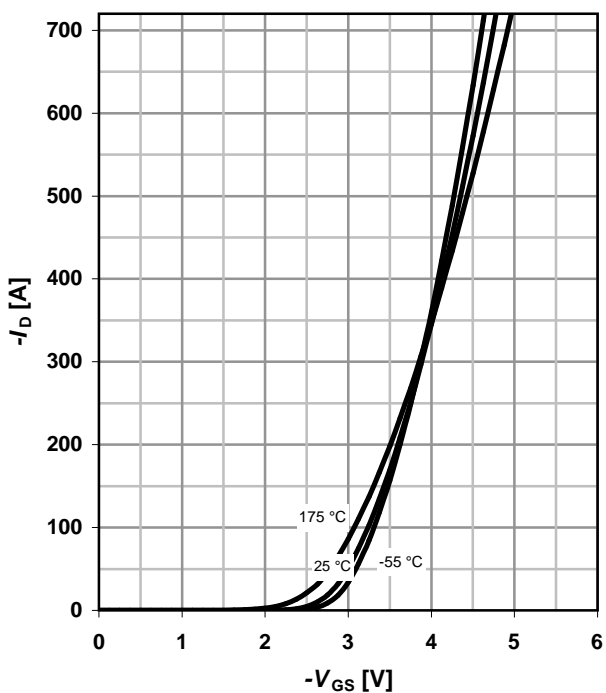
parameter: V_{GS}



7 Typ. transfer characteristics

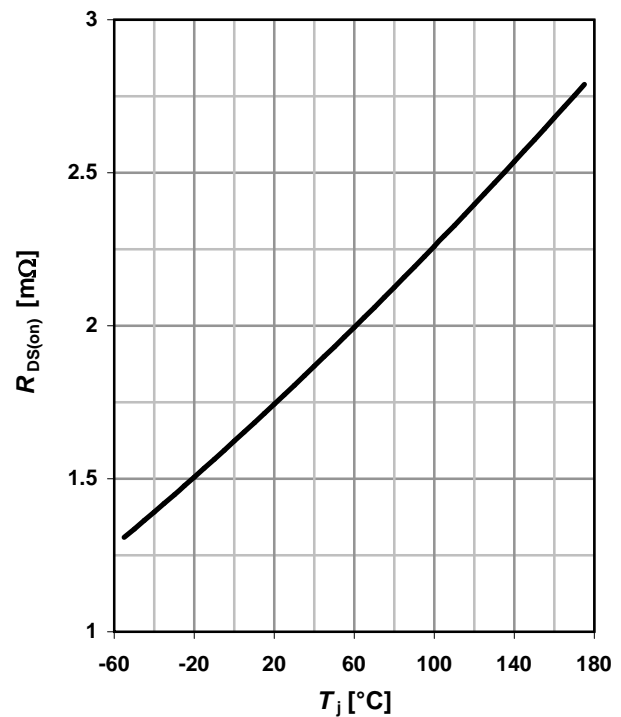
$I_D = f(V_{GS}); V_{DS} = -6\text{V}$

parameter: T_j



8 Typ. drain-source on-state resistance

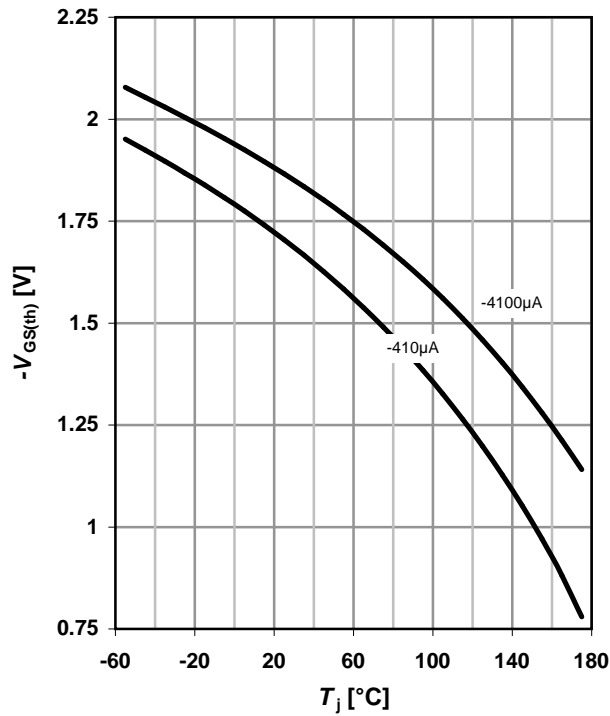
$R_{DS(on)} = f(T_j); I_D = -100\text{A}; V_{GS} = -10\text{V}$



9 Typ. gate threshold voltage

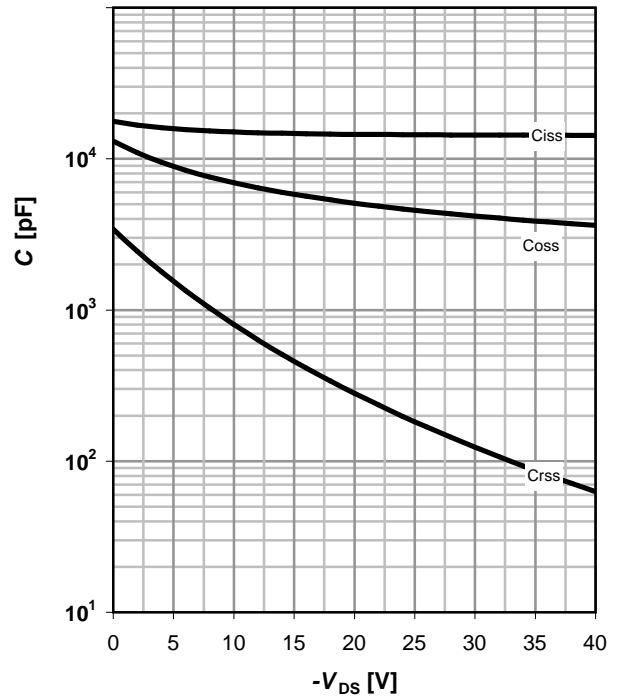
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

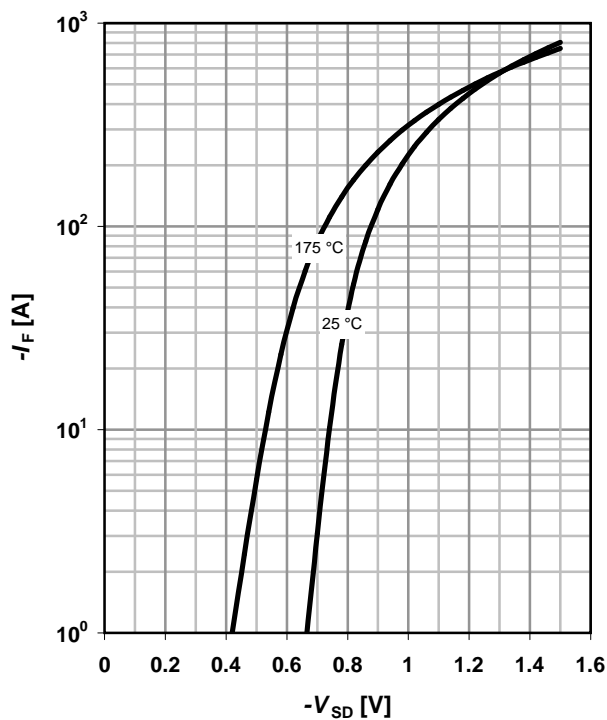
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

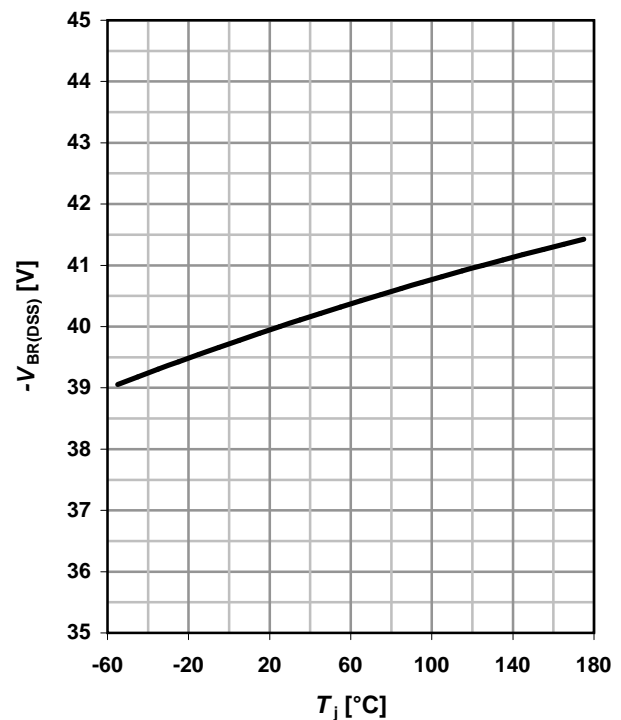
$I_F = f(V_{SD})$

parameter: T_j



12 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j); I_D = -1mA$

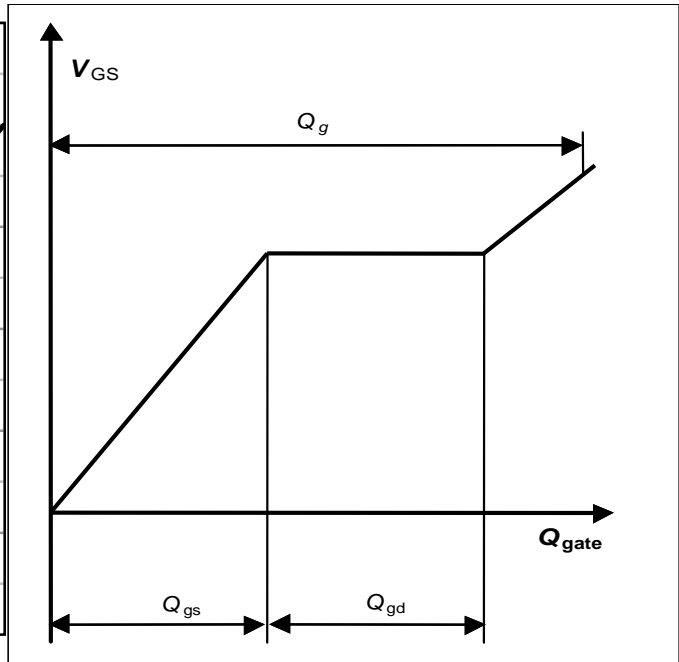
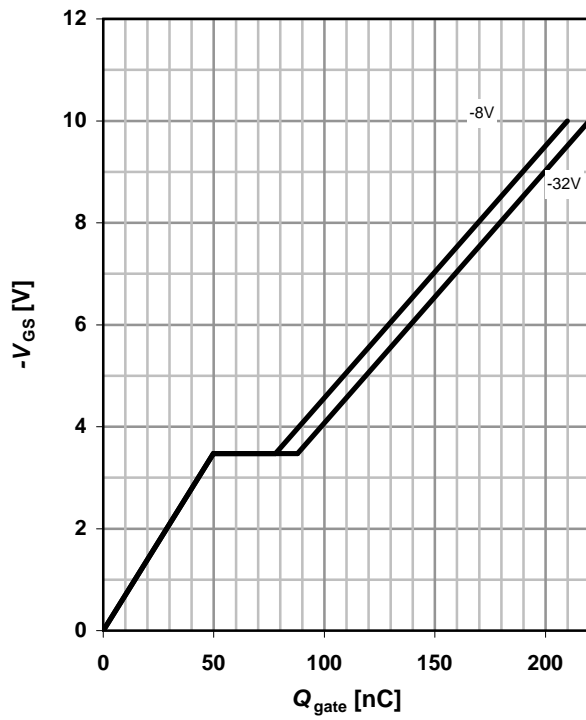


13 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = -180A$ pulsed

parameter: V_{DD}

14 Gate charge waveforms



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Revision History

Version	Date	Changes
1.1	02.09.2009	$R_{DS(on)}$ @4.5V: I_D changed to 135A
1.1	02.09.2009	$V_{GS(th)}$: I_D changed to 410uA
1.2	07.10.2009	$R_{DS(on)}$ @4.5V: I_D changed to 80A
1.2	07.10.2009	$R_{DS(on)}$ @10V: I_D changed to 80A
1.2	07.10.2009	V_{SD} : I_D changed to 80A
1.3	27.04.2011	Final Data Sheet