

OptiMOS®-P2 Power-Transistor

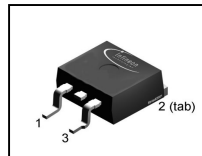
Features

- P-channel - Logic Level - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- 100% Avalanche tested

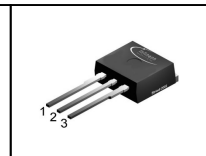
Product Summary

V_{DS}	-40	V
$R_{DS(on)}$ (SMD Version)	6.4	mΩ
I_D	-80	A

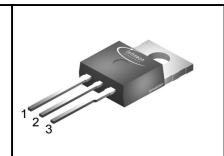
PG-TO263-3-2



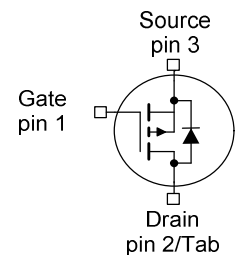
PG-TO262-3-1



PG-TO220-3-1



Type	Package	Marking
IPB80P04P4L-06	PG-TO263-3-2	4P04L06
IPI80P04P4L-06	PG-TO262-3-1	4P04L06
IPP80P04P4L-06	PG-TO220-3-1	4P04L06


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=-10\text{V}$	-80	A
		$T_C=100\text{ °C}$, $V_{GS}=-10\text{V}^{2)}$	-68	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	-320	
Avalanche energy, single pulse	E_{AS}	$I_D=-40\text{A}$	31	mJ
Avalanche current, single pulse	I_{AS}	-	-80	A
Gate source voltage	V_{GS}	-	$\pm 16^{3)}$	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	88	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}		-	-	1.7	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ⁴⁾	-	-	40	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-1mA$	-40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-150\mu A$	-1.2	-1.7	-2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-32V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-0.05	-1	μA
		$V_{DS}=-32V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-20	-200	
Gate-source leakage current	I_{GSS}	$V_{GS}=-16V, V_{DS}=0V$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-50A$	-	8.2	10.8	m Ω
		$V_{GS}=-4.5V, I_D=-50A, \text{SMD version}$	-	7.9	10.5	
		$V_{GS}=-10V, I_D=-80A$	-	5.8	6.7	
		$V_{GS}=-10V, I_D=-80A, \text{SMD version}$	-	5.5	6.4	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=-25V,$ $f=1MHz$	-	5060	6580	pF
Output capacitance	C_{oss}		-	1520	2280	
Reverse transfer capacitance	C_{rss}		-	60	120	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-20V,$ $V_{GS}=-10V, I_D=-80A,$ $R_G=3.5\Omega$	-	17	-	ns
Rise time	t_r		-	12	-	
Turn-off delay time	$t_{d(off)}$		-	61	-	
Fall time	t_f		-	44	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=-32V,$ $I_D=-80A,$ $V_{GS}=0$ to $-10V$	-	19	25	nC
Gate to drain charge	Q_{gd}		-	13	26	
Gate charge total	Q_g		-	80	104	
Gate plateau voltage	$V_{plateau}$		-	3.6	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	-80	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	-320	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=-80A,$ $T_J=25^\circ C$	-	-1	-1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=-20V, I_F=-50A,$ $di_F/dt=-100A/\mu s$	-	56	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	64	-	nC

¹⁾ Current is limited by bondwire; with an $R_{thJC} = 1.7K/W$ the chip is able to carry -96A at 25°C.

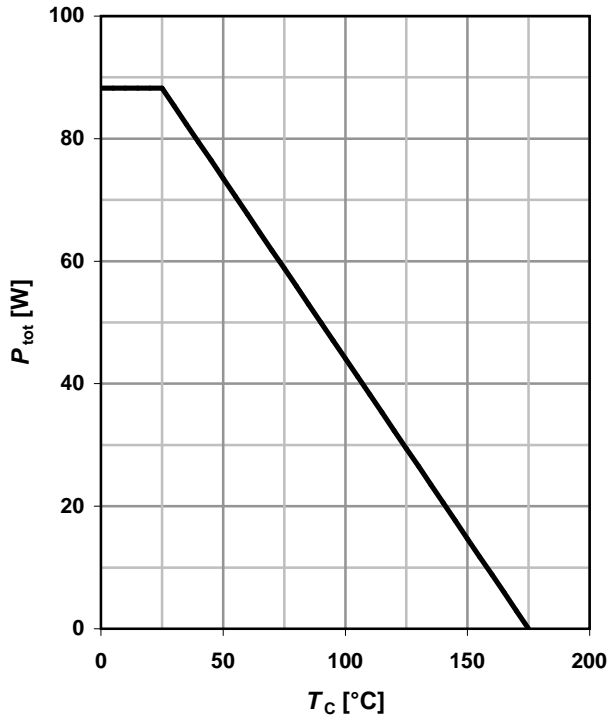
²⁾ Defined by design. Not subject to production test.

³⁾ $V_{GS}=+5V/-16V$ according AEC; $V_{GS}=+16V$ for max 168h at $T_J=175^\circ C$

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

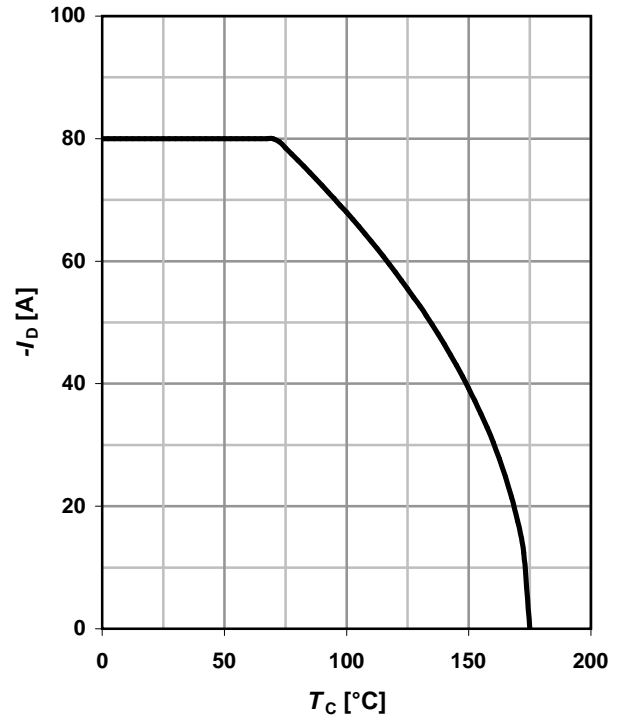
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \leq -6V$



2 Drain current

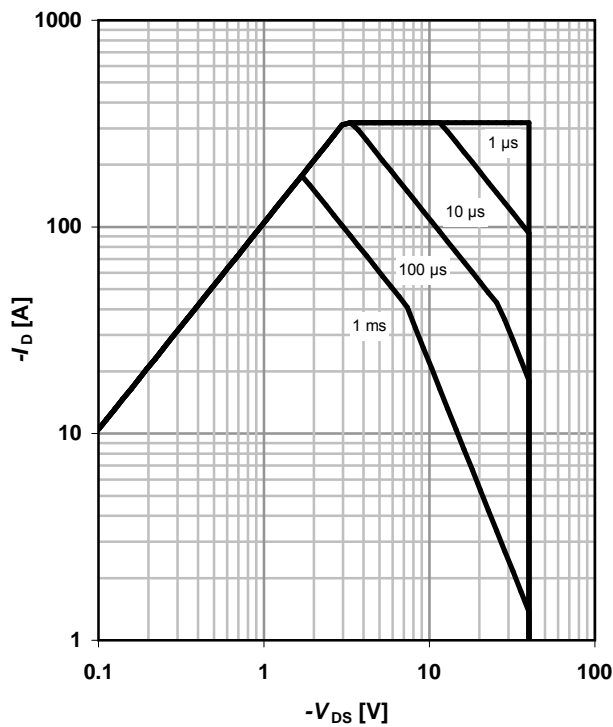
$I_D = f(T_C); V_{GS} \leq -6V; SMD$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25^\circ C; D = 0; SMD$

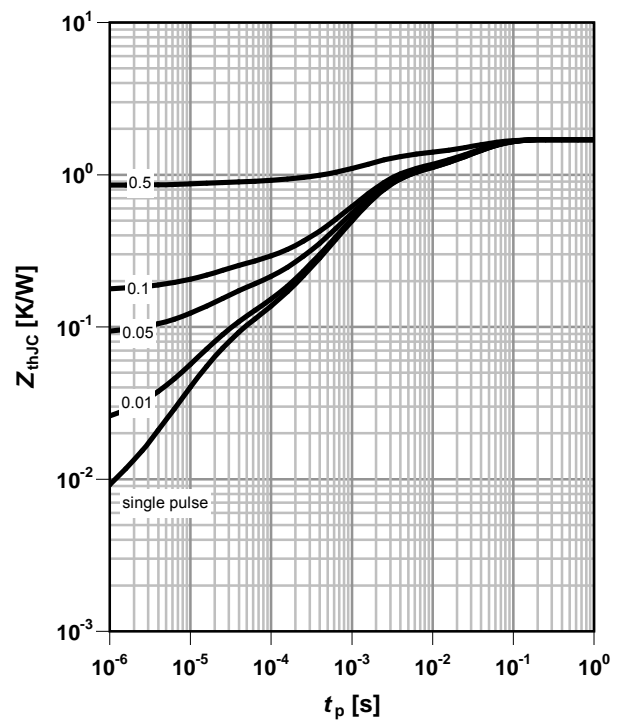
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

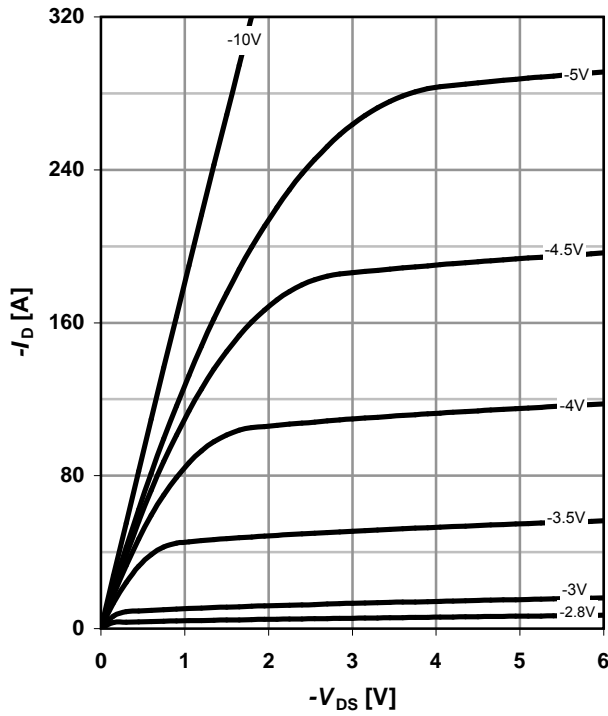
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}; \text{SMD}$

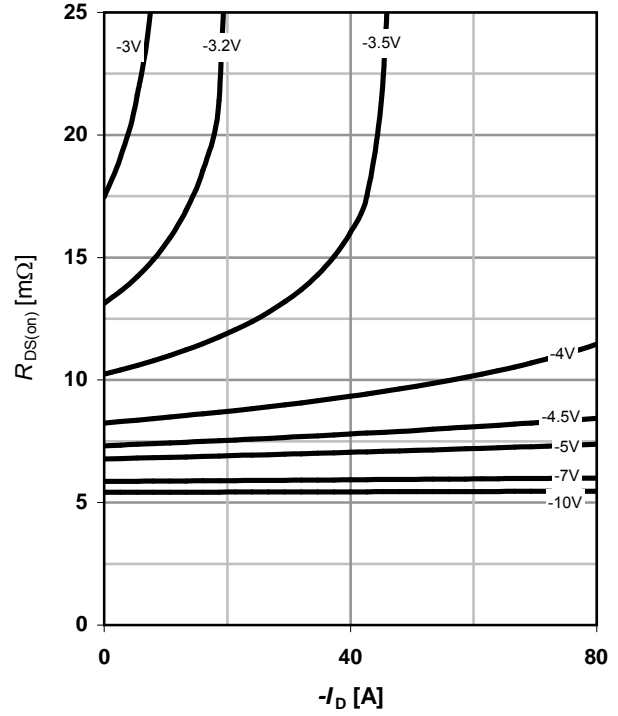
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}; \text{SMD}$

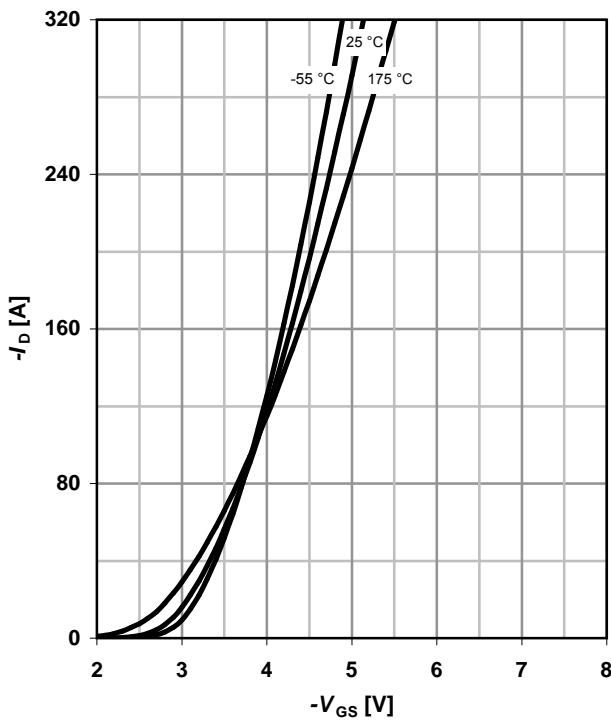
parameter: V_{GS}



7 Typ. transfer characteristics

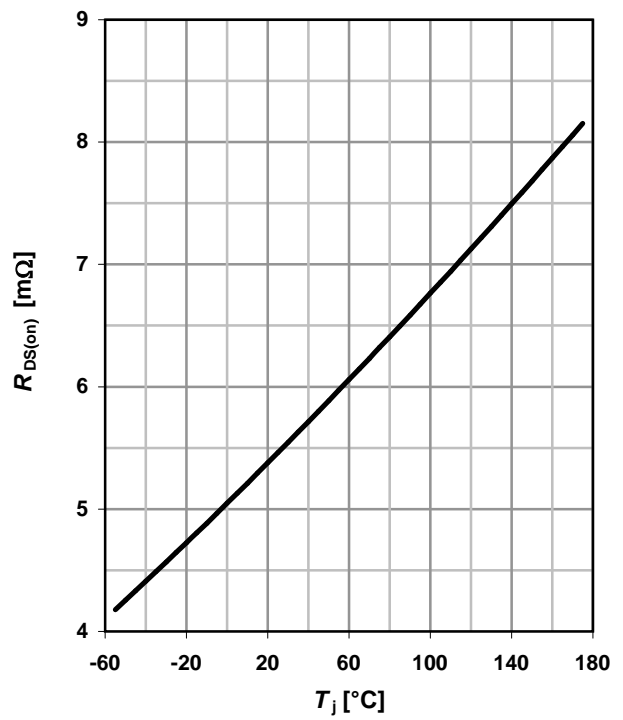
$I_D = f(V_{GS}); V_{DS} = -6\text{V}$

parameter: T_j



8 Typ. drain-source on-state resistance

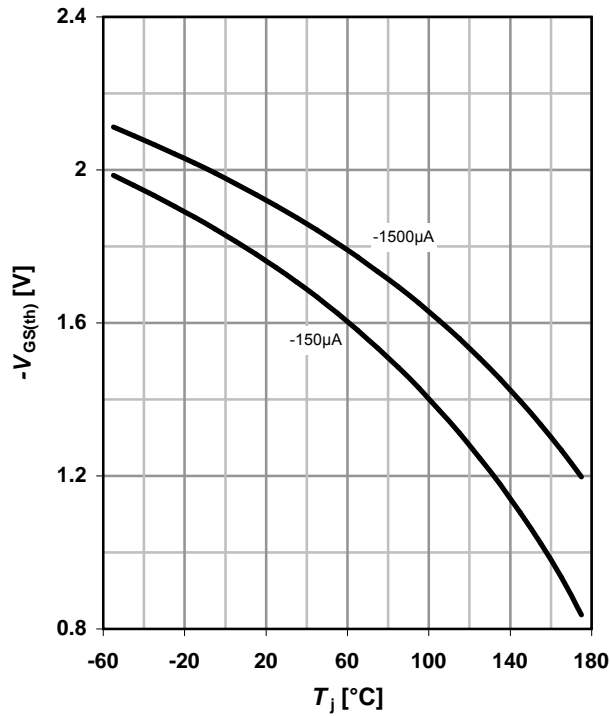
$R_{DS(on)} = f(T_j); I_D = -80\text{ A}; V_{GS} = -10\text{ V}; \text{SMD}$



9 Typ. gate threshold voltage

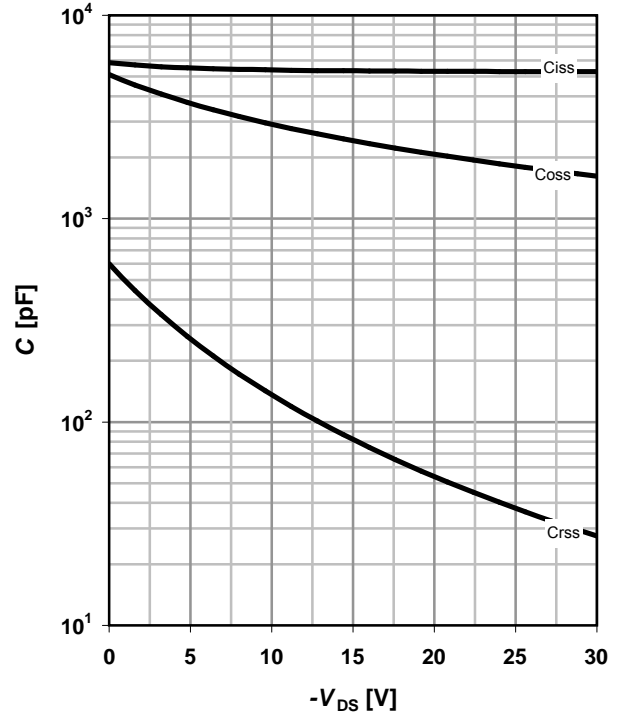
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

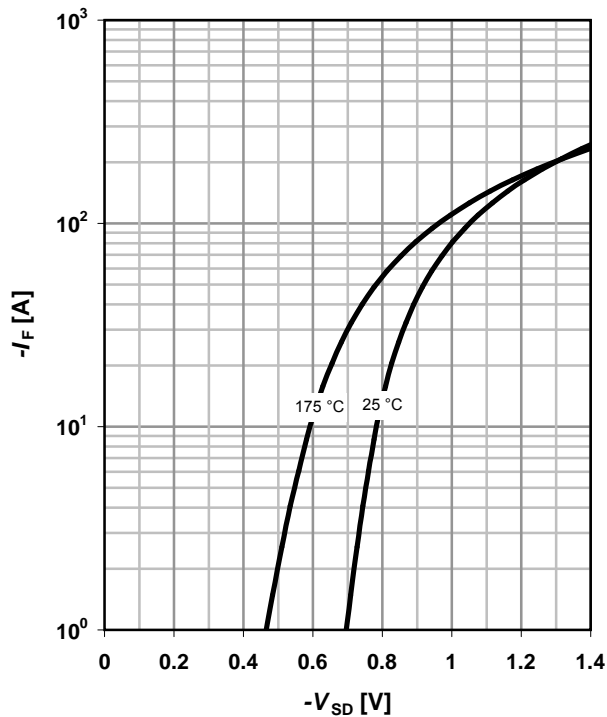
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

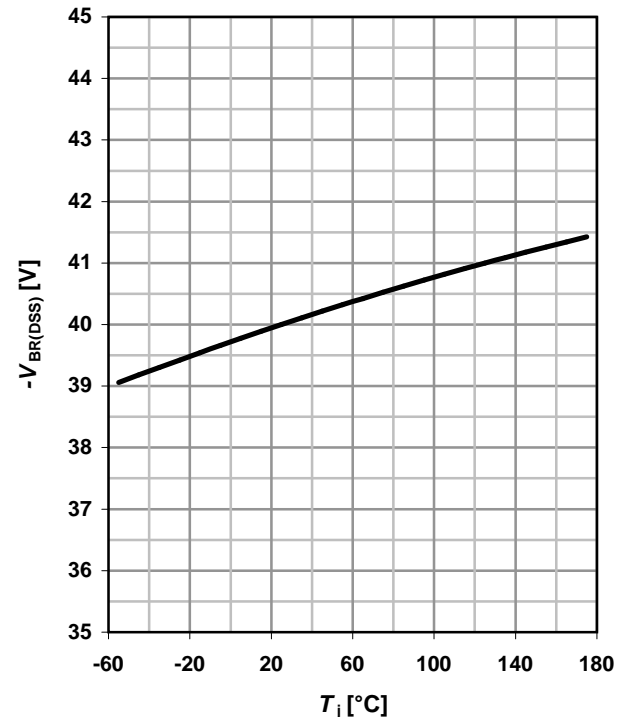
$I_F = f(V_{SD})$

parameter: T_j



12 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j); I_D = -1 mA$

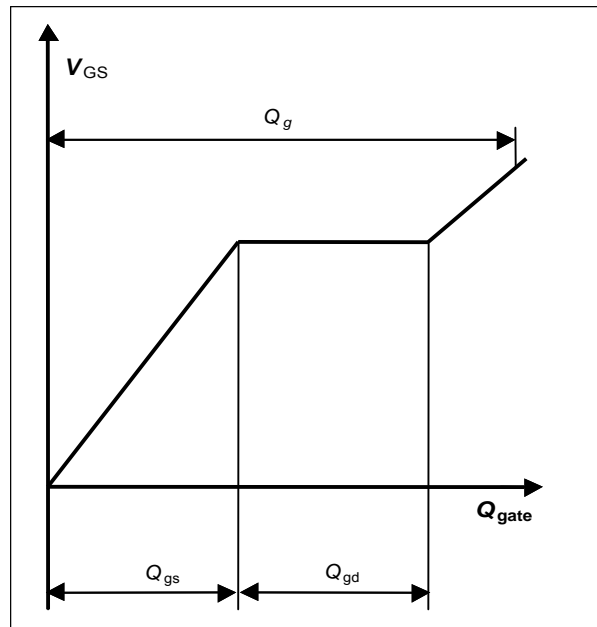
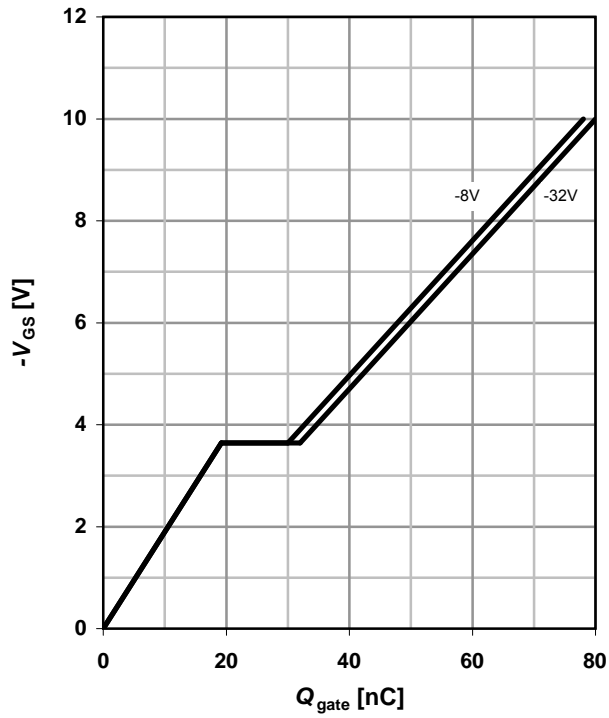


13 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = -80 \text{ A pulsed}$

parameter: V_{DD}

14 Gate charge waveforms



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Revision History

Version	Date	Changes
0.1	08.03.2010	Initial Target Data Sheet
1.0	03.02.2011	Final Data Sheet