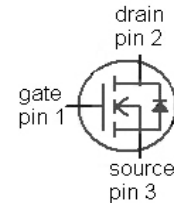


OptiMOS[®] 2 Power-Transistor
Features

- Ideal for high-frequency dc/dc converters
- Qualified according to JEDEC¹⁾ for target applications
- N-channel, logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant

Product Summary


V_{DS}	25	V
$R_{DS(on),max}$ (SMD Version)	4.2	m Ω
I_D	90	A



Type	IPDH4N03LA G	IPSH4N03LA G
Package	P-TO252-3-11	P-TO251-3-11
Ordering Code	Q67042-S4250	Q67042-S4254
Marking	H4N03LA	H4N03LA

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}^{2)}$	90	A
		$T_C=100\text{ °C}$	77	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}^{3)}$	360	
Avalanche energy, single pulse	E_{AS}	$I_D=90\text{ A}$, $R_{GS}=25\ \Omega$	150	mJ
Reverse diode dv/dt	dv/dt	$I_D=90\text{ A}$, $V_{DS}=20\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=175\text{ °C}$	6	kV/ μs
Gate source voltage ⁴⁾	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	94	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1.6	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	75	
		6 cm ² cooling area ⁵⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=40\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=50\text{ A}$	-	6.1	7.6	m Ω
		$V_{GS}=4.5\text{ V}, I_D=50\text{ A},$ SMD version	-	5.9	7.4	
		$V_{GS}=10\text{ V}, I_D=60\text{ A}$	-	3.7	4.4	
		$V_{GS}=10\text{ V}, I_D=60\text{ A},$ SMD version	-	3.5	4.2	
Gate resistance	R_G		-	1.3	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max},$ $I_D=60\text{ A}$	45	90	-	S

¹⁾ J-STD20 and JESD22

¹⁾ Current is limited by bondwire; with an $R_{thJC}=1.6\text{ K/W}$ the chip is able to carry 109 A.

³⁾ See figure 3

⁴⁾ $T_{j,max}=150\text{ °C}$ and duty cycle $D<0.25$ for $V_{GS}<-5\text{ V}$
⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	2400	3200	pF
Output capacitance	C_{oss}		-	920	1200	
Reverse transfer capacitance	C_{rss}		-	110	160	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=25\text{ A}, R_G=2.7\ \Omega$	-	9	14	ns
Rise time	t_r		-	7	11	
Turn-off delay time	$t_{d(off)}$		-	29	44	
Fall time	t_f		-	4.6	7	

Gate Charge Characteristics⁶⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=45\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$	-	8	11	nC
Gate charge at threshold	$Q_{g(th)}$		-	3.9	5.1	
Gate to drain charge	Q_{gd}		-	5.6	8	
Switching charge	Q_{sw}		-	10	14	
Gate charge total	Q_g		-	19	26	
Gate plateau voltage	$V_{plateau}$		-	3.4	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }5\text{ V}$	-	17	23	nC
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	20	27	

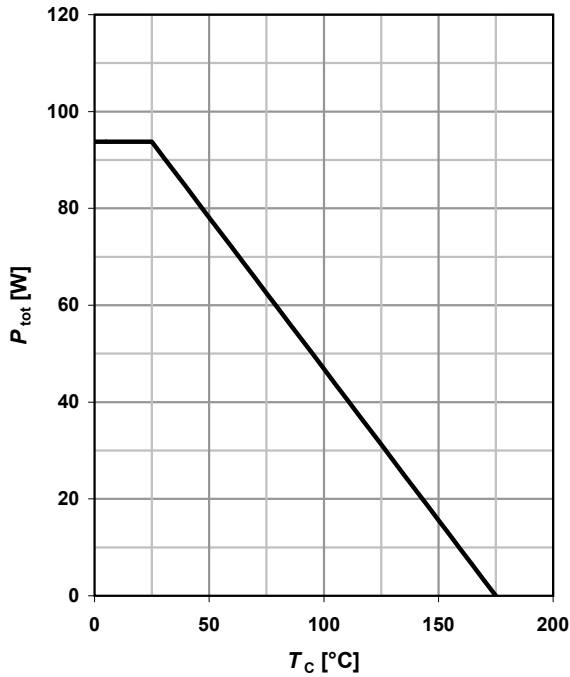
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	78	A
Diode pulse current	$I_{S,pulse}$		-	-	360	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=78\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.93	1.2	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	15	nC

⁶⁾ See figure 16 for gate charge parameter definition

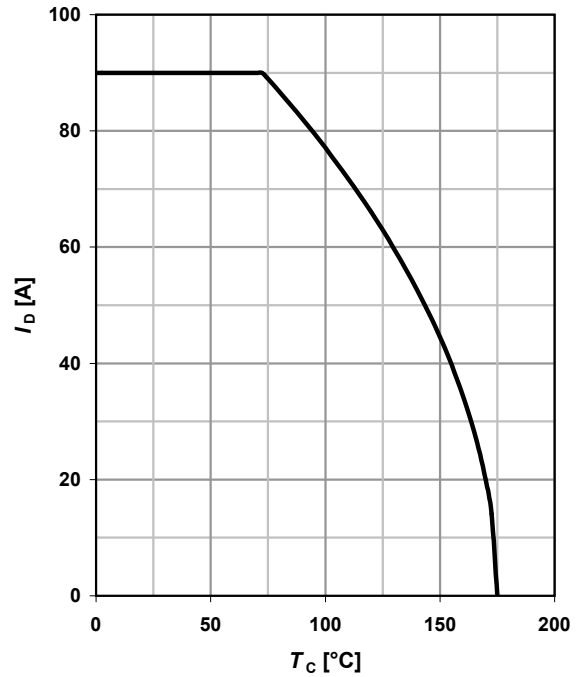
1 Power dissipation

$$P_{tot} = f(T_C)$$



2 Drain current

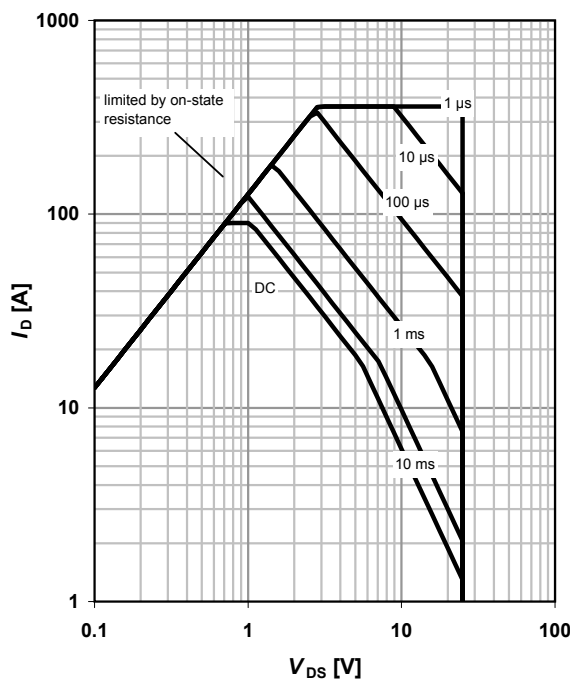
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

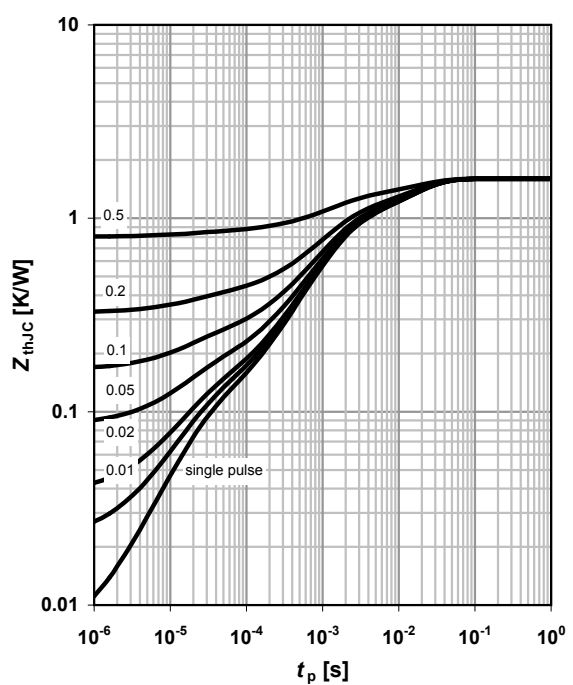
parameter: t_p



4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

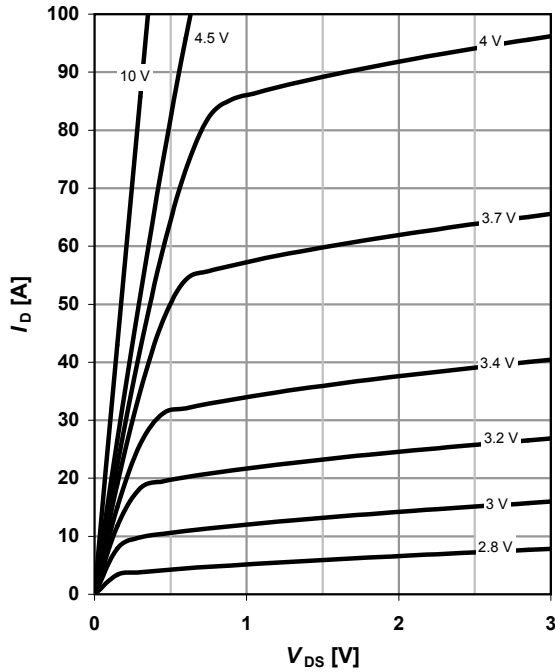
parameter: $D = t_p / T$



5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$$

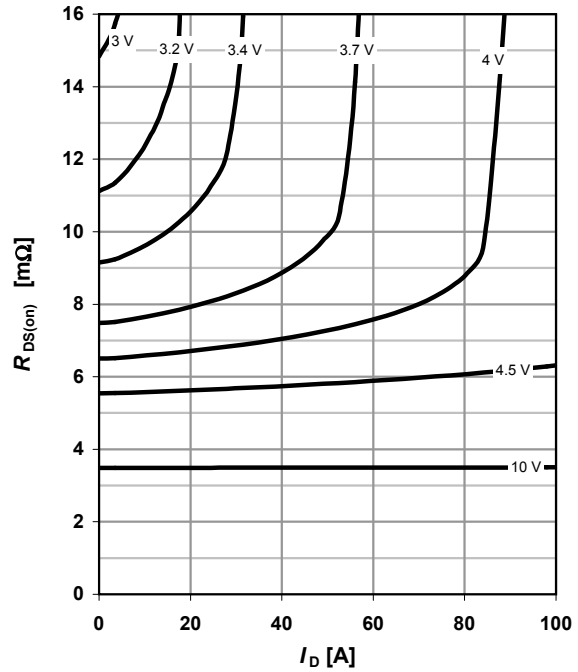
parameter: V_{GS}



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$$

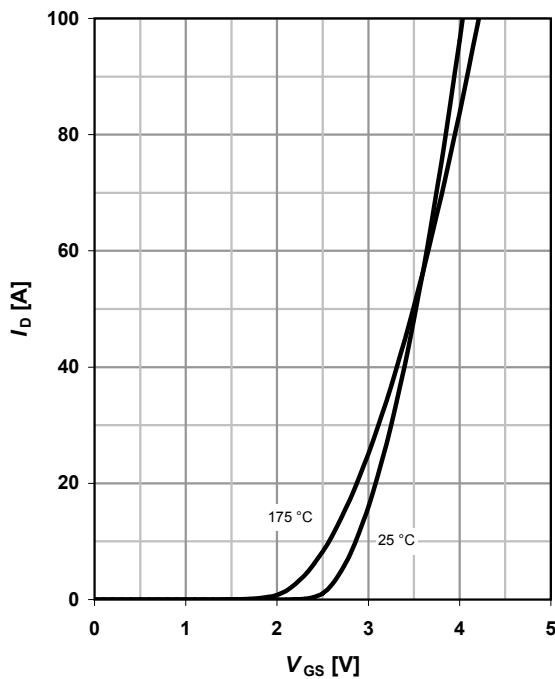
parameter: V_{GS}



7 Typ. transfer characteristics

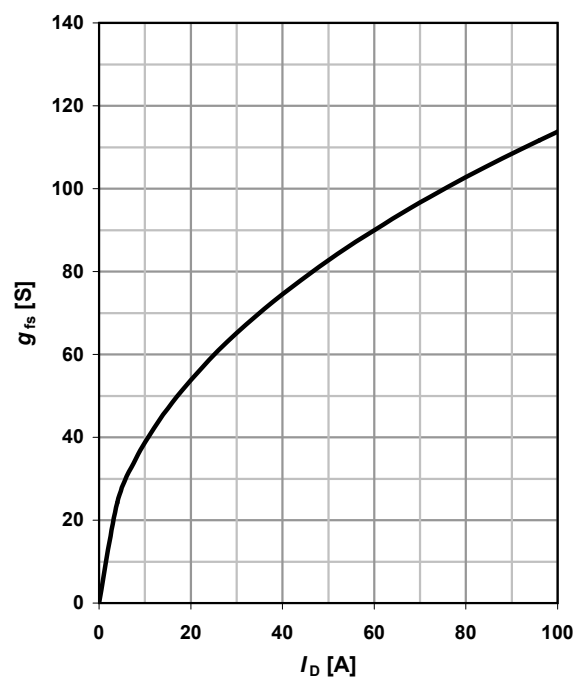
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

parameter: T_j



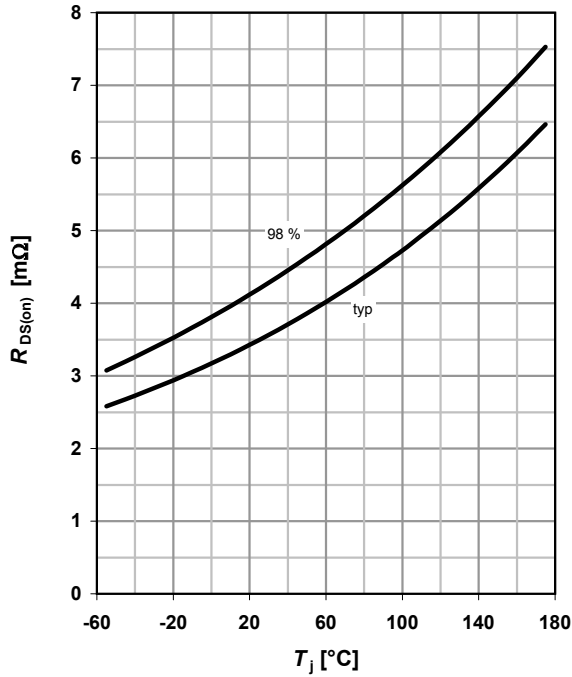
8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$$



9 Drain-source on-state resistance

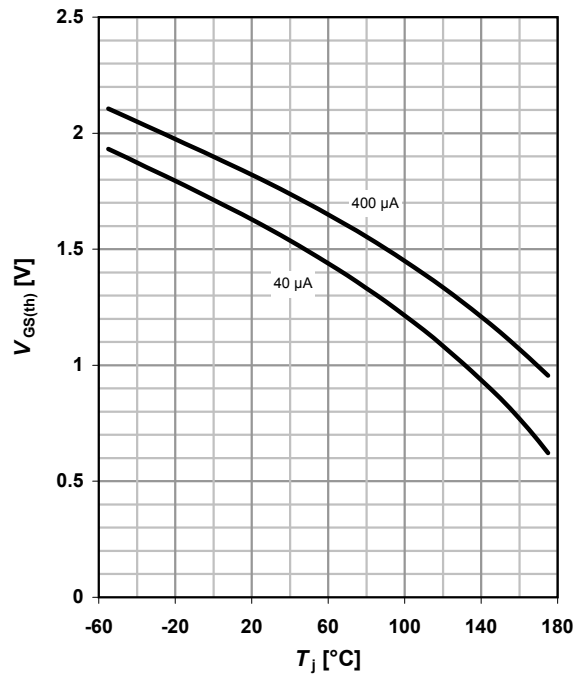
$$R_{DS(on)} = f(T_j); I_D = 60 \text{ A}; V_{GS} = 10 \text{ V}$$



10 Typ. gate threshold voltage

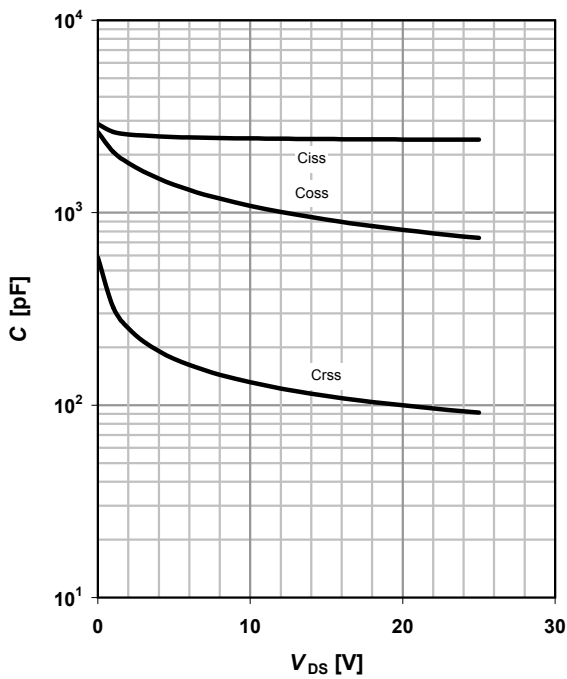
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



11 Typ. capacitances

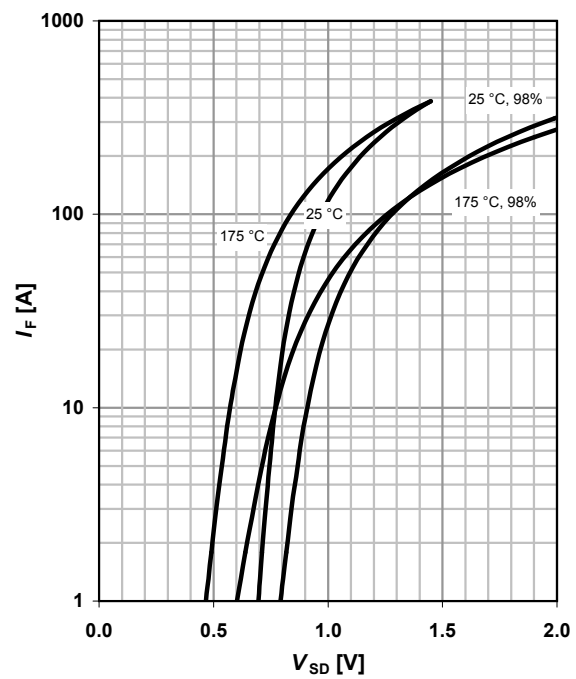
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

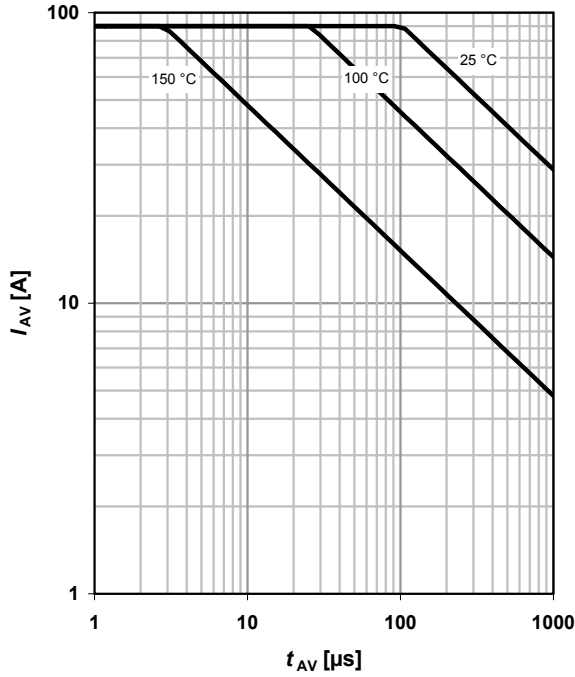
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

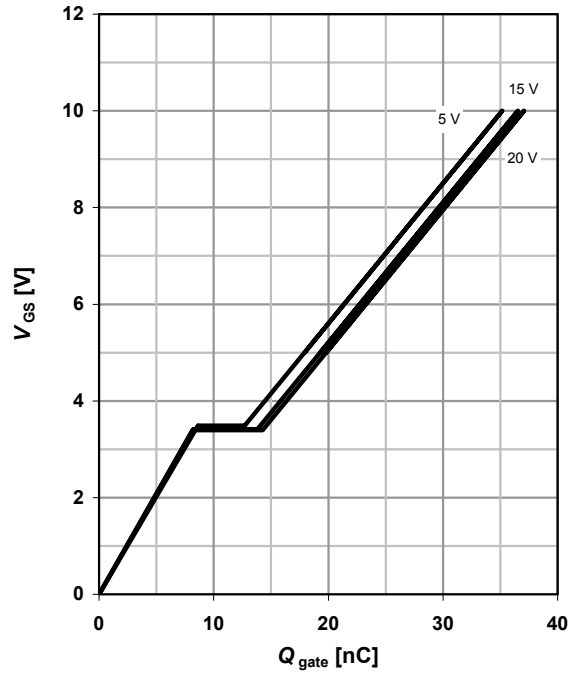
parameter: $T_{j(start)}$



14 Typ. gate charge

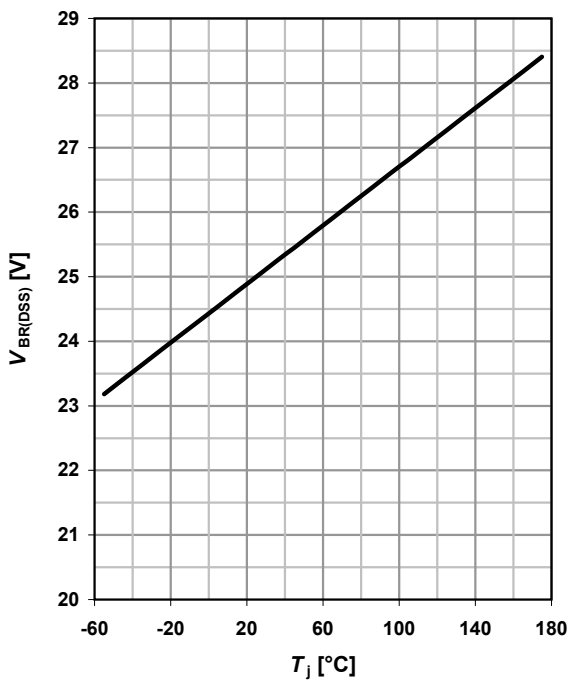
$V_{GS}=f(Q_{gate}); I_D=45 \text{ A pulsed}$

parameter: V_{DD}

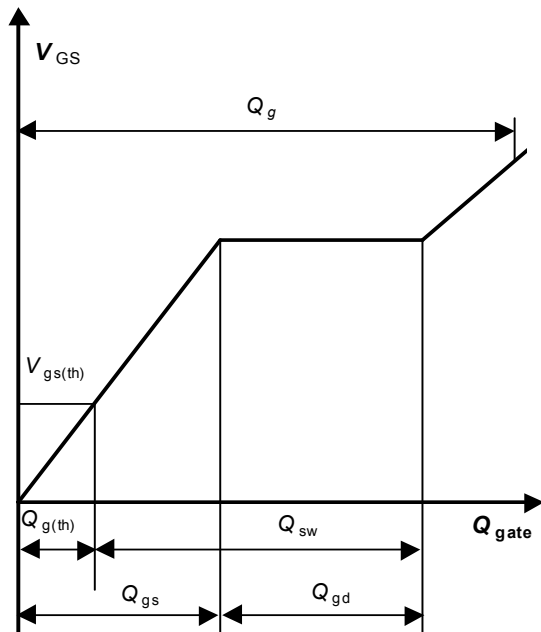


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

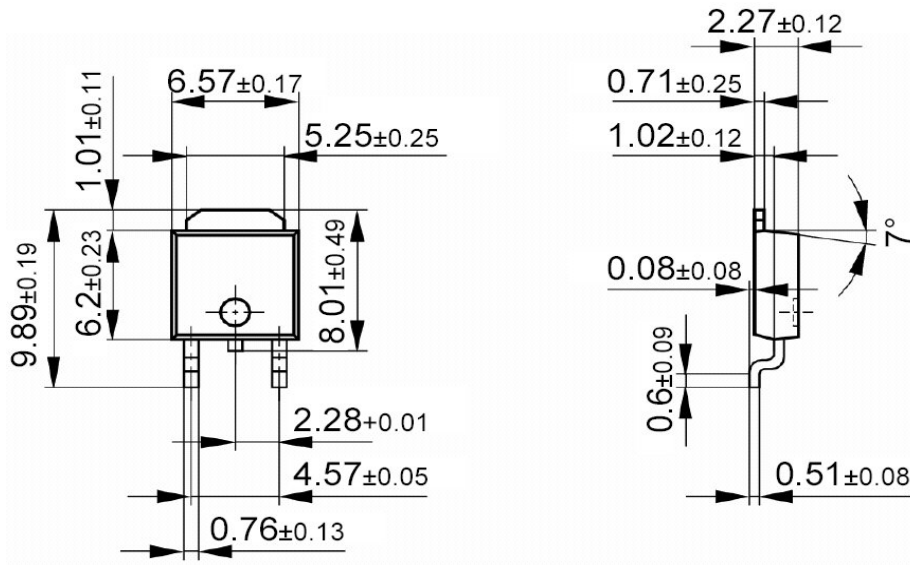


16 Gate charge waveforms

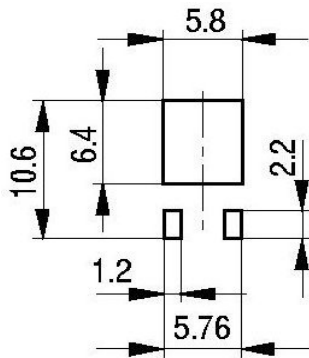


Package Outline

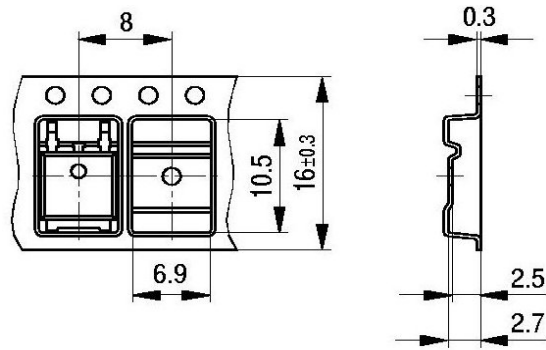
P-TO252-3-11: Outline



Footprint:



Packaging:



Dimensions in mm