MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ ThinkPAK 8x8

650V CoolMOS™ E6 Power Transistor
IPL65R420E6

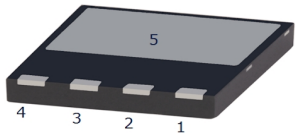
Data Sheet

Rev. 2.1
Final

Industrial & Multimarket

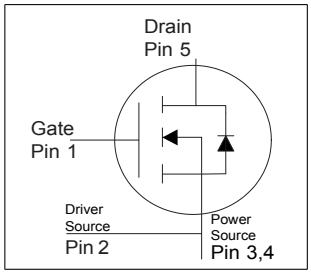
1 Description

ThinPAK 8x8



CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ E6 series combines the experience of the leading SJ MOSFET supplier with high class innovation.
The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter, and cooler.

ThinPAK
ThinPAK is a new leadless SMD package for HV MOSFETs. The new package has a very small footprint of only 64mm² (vs. 150mm² for the D²PAK) and a very low profile with only 1mm height (vs. 4.4mm for the D²PAK). The significantly smaller package size, combined with benchmark low parasitic inductances, provides designers with a new and effective way to decrease system solution size in power-density driven designs.



Features

- Reduced board space consumption
- Increased power density
- Short commutation loop
- Smooth switching waveform
- easy to use products
- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Pb-free plating, Halogen free
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD TV, Lighting, Server, Telecom.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j\,max}$	700	V
RDS(on),max	0.42	Ω
Qg,typ	39	nC
ID,pulse	26	A
Eoss @ 400V	2.8	µJ
Body diode di/dt	500	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPL65R420E6	PG-VSON-4	65E6420	see Appendix A

Table of Contents

2 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D			10.1	A	T_C = 25°C
				6.4		T_C = 100°C
Pulsed drain current [2]	$I_{D,pulse}$			26	A	T_C = 25°C
Avalanche energy, single pulse	E_{AS}			215	mJ	I_D = 1.8A, V_{DD} = 50V (see table 10)
Avalanche energy, repetitive	E_{AR}			0.32	mJ	I_D = 1.8A, V_{DD} = 50V
Avalanche current, repetitive	I_{AR}			1.8	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	V_{DS} = 0 ... 480V
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC (f > 1 Hz)
Operating and storage temperature	T_j, T_{stg}	-40		150	°C	
Continuous diode forward current	I_S			8.7	A	T_C = 25°C
Diode pulse current	$I_{S,pulse}$			26	A	T_C = 25°C
Reverse diode dv/dt [3]	dv/dt			15	V/ns	V_{DS} = 0 ... 400V, $I_{SD} \le I_D$, T_j = 25°C (see table 8)
Maximum diode commutation speed	di_f/dt			500	A/µs	
Power dissipation	P_{tot}			83	W	T_C=25°C

[1] Limited by $T_{j\,max}$. Maximum duty cycle D=0.75
[2] Pulse width t_p limited by $T_{j\,max}$
[3] Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics ThinPAK 8x8

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			1.5	°C/W	
Thermal resistance, junction - ambient [1]	R_{thJA}			65	°C/W	SMD version, device on PCB, minimal footprint
				45		SMD version, device on PCB, 6cm² cooling area
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}			260	°C	reflow MSL 3

[1] Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

at T_j = 25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	V_{GS} = 0V, I_D = 1mA
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	V_{DS} = V_{GS}, I_D = 0.3mA
Zero gate voltage drain current	I_{DSS}			1	µA	V_{DS} = 650V, V_{GS} = 0V, T_j = 25°C
			10			V_{DS} = 650V, V_{GS} = 0V, T_j = 150°C
Gate-source leakage current	I_{GSS}			100	nA	V_{GS} = 20V, V_{DS} = 0V
Drain-source on-state resistance	$R_{DS(on)}$		0.378	0.42	Ω	V_{GS} = 10V, I_D = 3.4A, T_j = 25°C
			0.983			V_{GS} = 10V, I_D = 3.4A, T_j = 150°C
Gate resistance	R_G		3.5		Ω	f = 1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		710		pF	V_{GS} = 0V, V_{DS} = 100V, f = 1MHz
Output capacitance	C_{oss}		41		pF	
Effective output capacitance, energy related [1]	$C_{o(er)}$		32		pF	V_{GS} = 0V, V_{DS} = 0 ... 480V
Effective output capacitance, time related [2]	$C_{o(tr)}$		140		pF	I_D = constant, V_{GS} = 0V, V_{DS} = 0 ... 480V
Turn-on delay time	$t_{d(on)}$		10		ns	V_{DD} = 400V, V_{GS} = 13V, I_D = 5.2A, R_G = 3.4Ω (see table 9)
Rise time	t_r		7		ns	
Turn-off delay time	$t_{d(off)}$		57		ns	
Fall time	t_f		8		ns	

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		4		nC	V_{DD} = 480V, I_D = 5.2A, V_{GS} = 0 to 10V
Gate to drain charge	Q_{gd}		20		nC	
Gate charge total	Q_g		39		nC	
Gate plateau voltage	$V_{plateau}$		5.5		V	

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

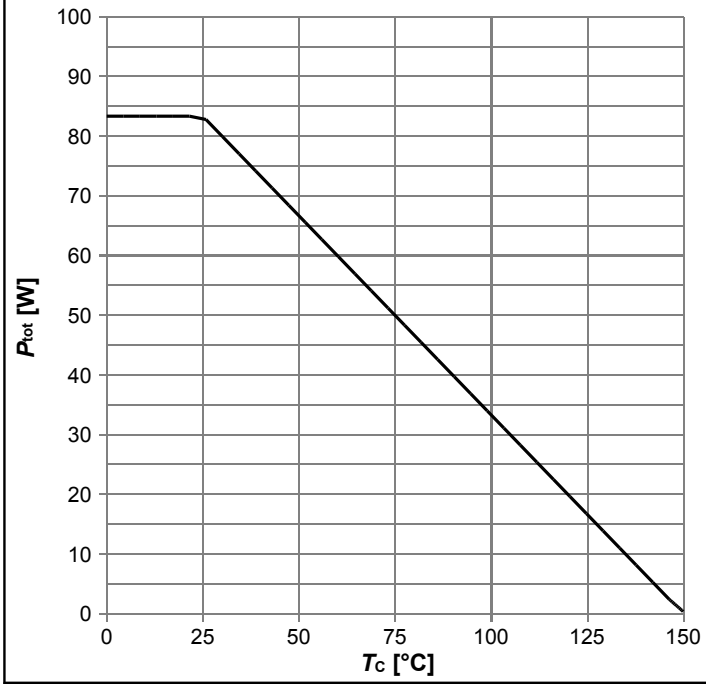
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	V_{GS} = 0V, I_F = 5.2A, T_j = 25°C
Reverse recovery time	t_{rr}		280		ns	V_R = 400V, I_F = 5.2A, di_F/dt = 100A/µs (see table 8)
Reverse recovery charge	Q_{rr}		2.8		µC	
Peak reverse recovery current	I_{rrm}		17		A	

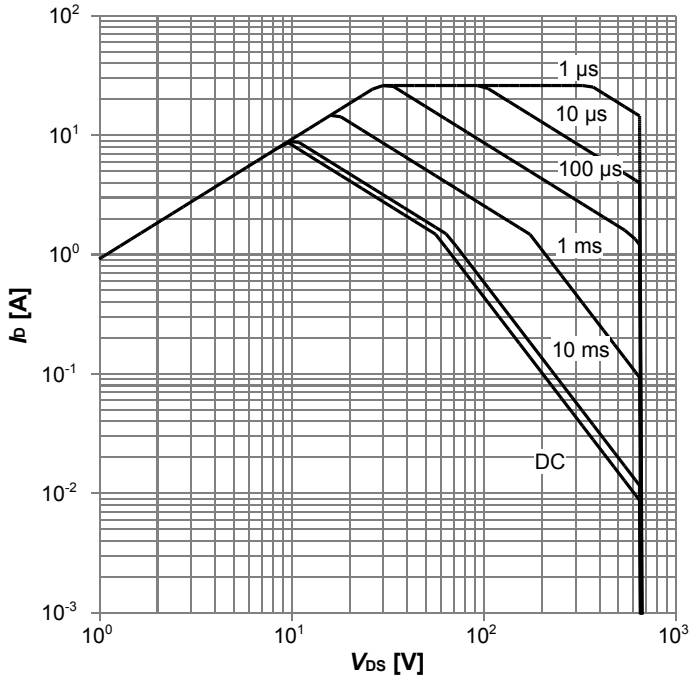
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



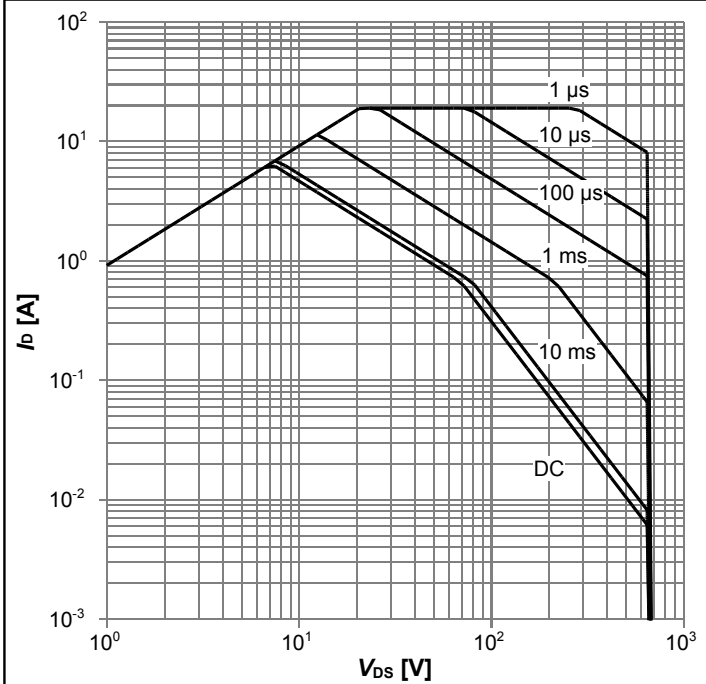
$P_{tot}=f(T_C)$

Diagram 2: Safe operating area



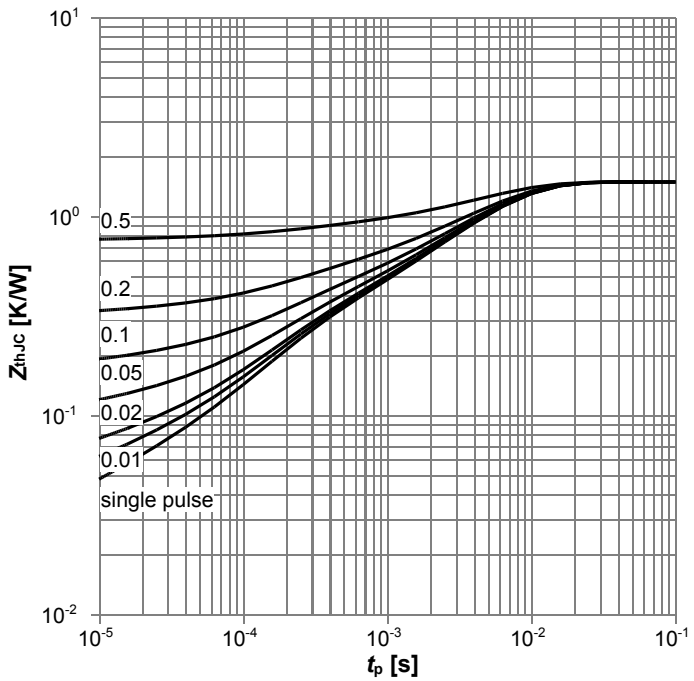
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 3: Safe operating area



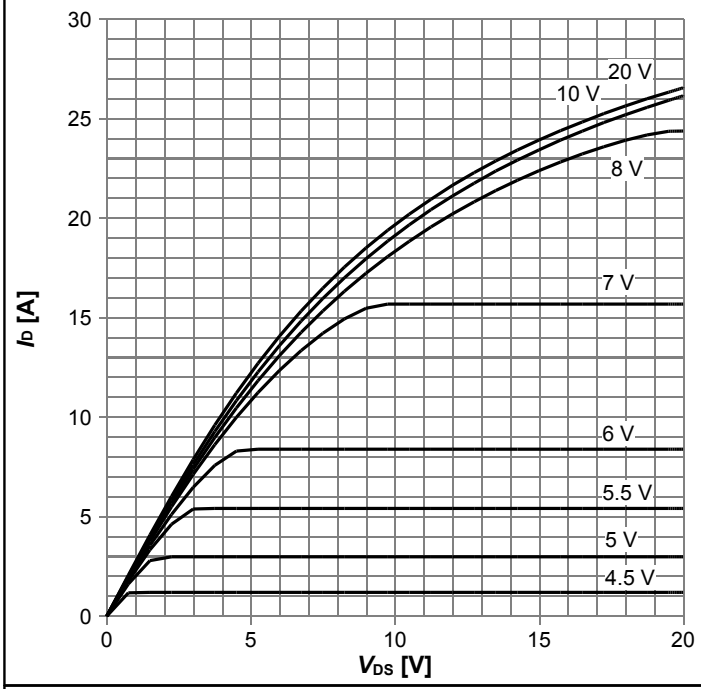
$I_D=f(V_{DS})$; $T_C=80$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



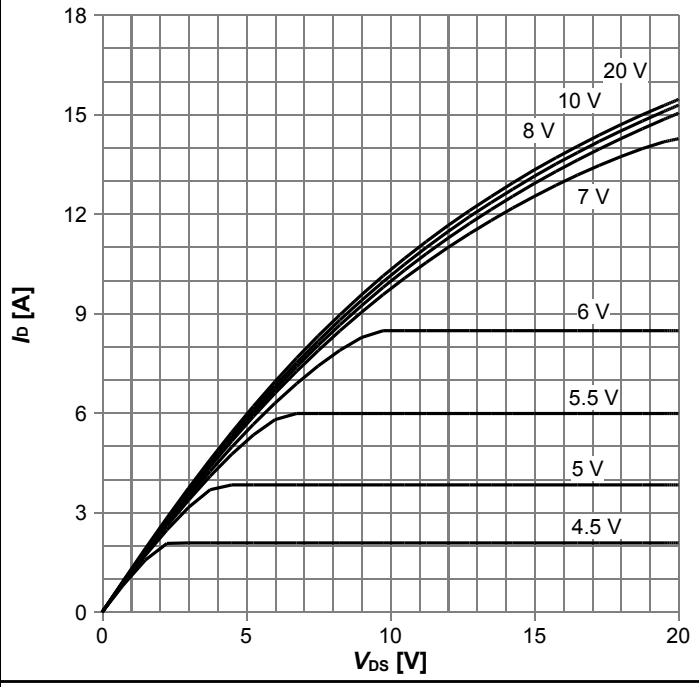
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



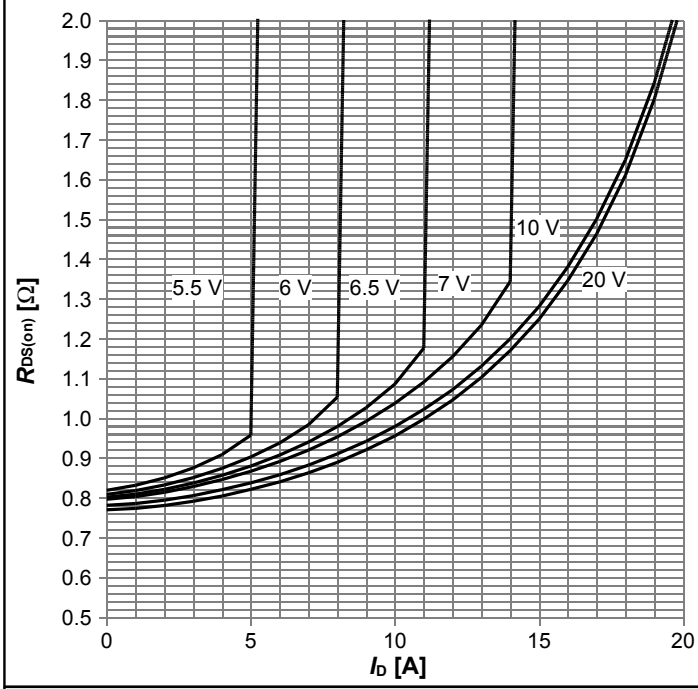
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



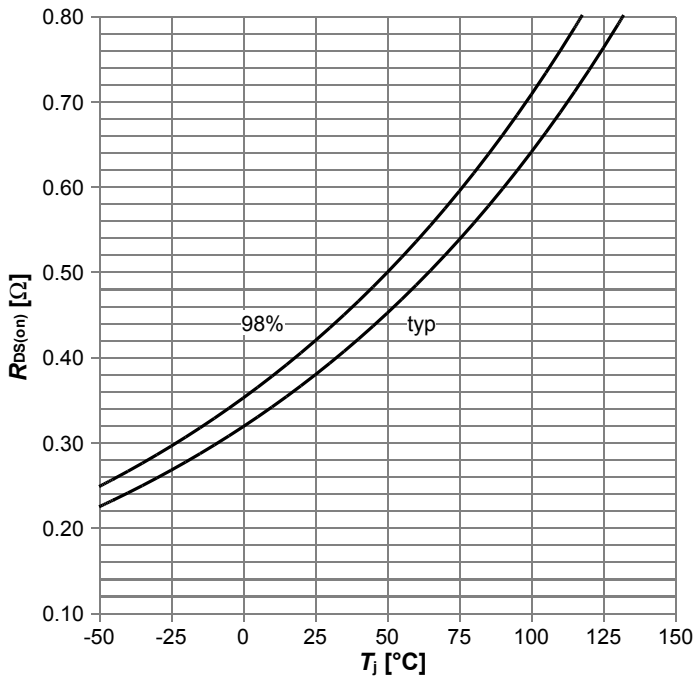
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



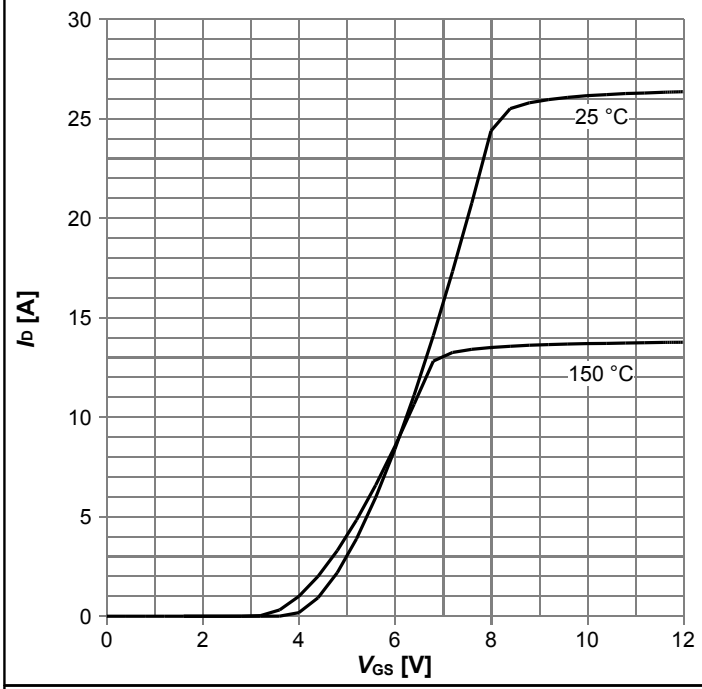
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



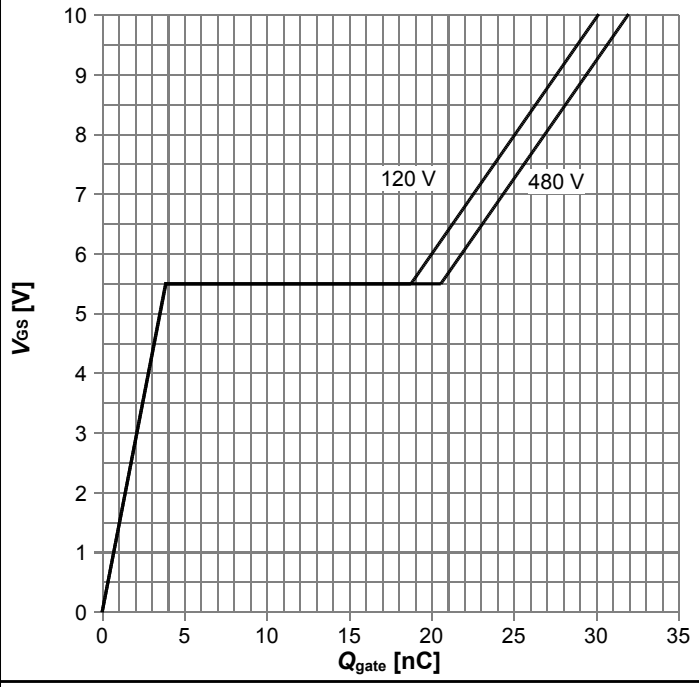
$R_{DS(on)}$=f(T_j); I_D=3.2 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



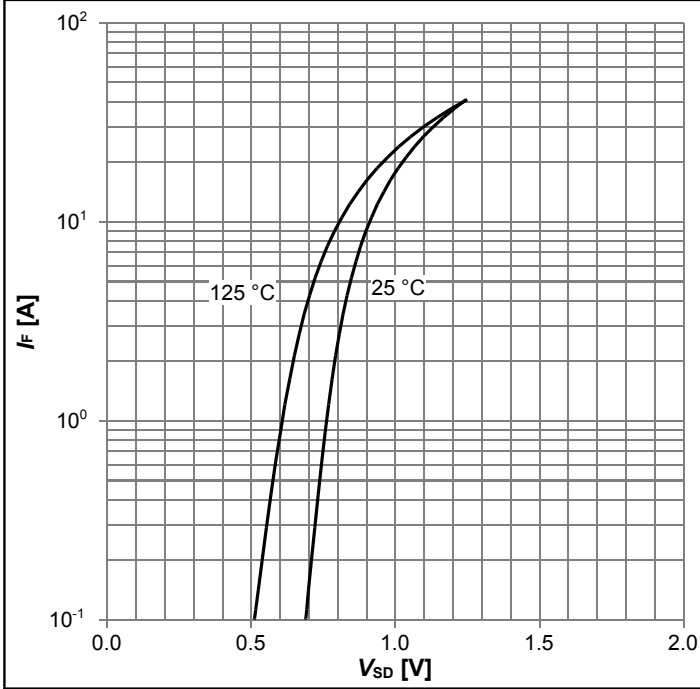
$I_D=f(V_{GS})$; V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



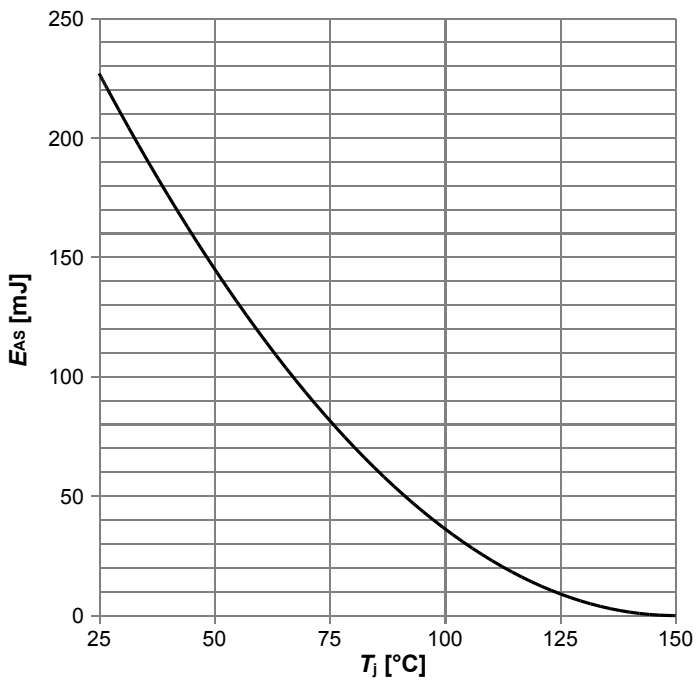
$V_{GS}=f(Q_{gate})$; I_D=4.9 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



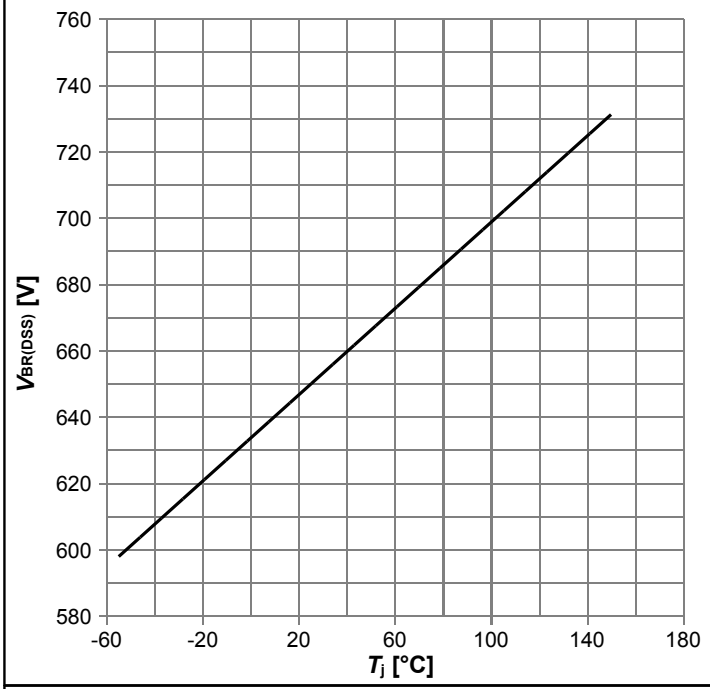
$I_F=f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



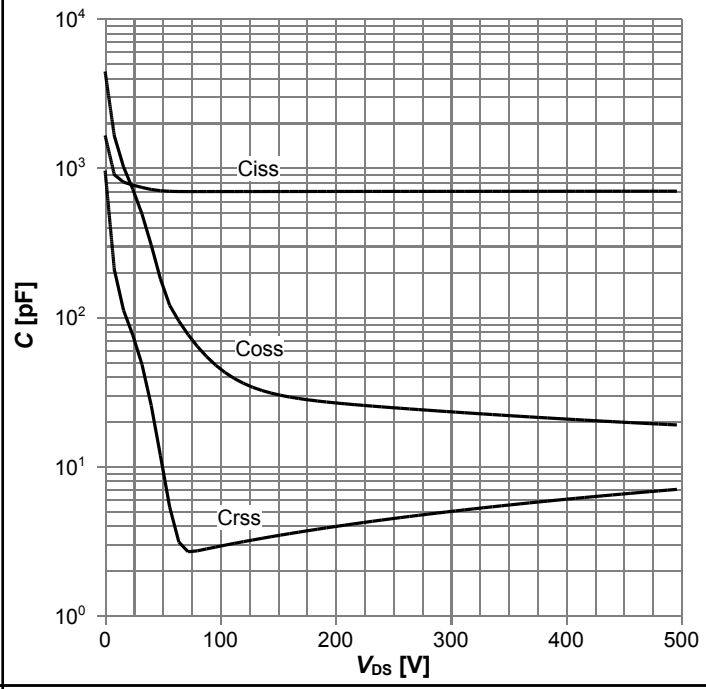
$E_{AS}=f(T_j)$; I_D=1.8 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



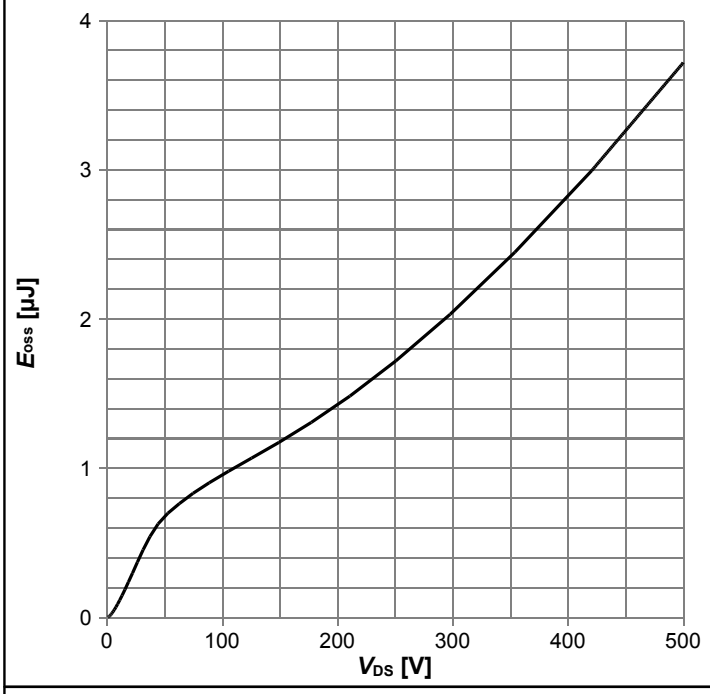
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

6 Test Circuits

Table 8 Diode characteristics

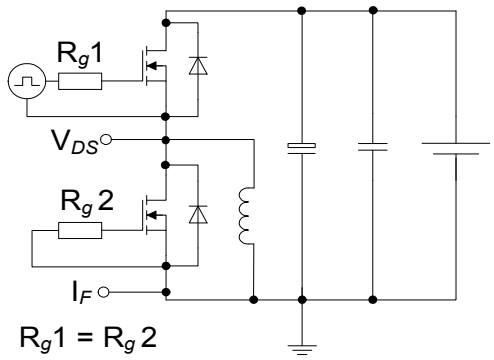
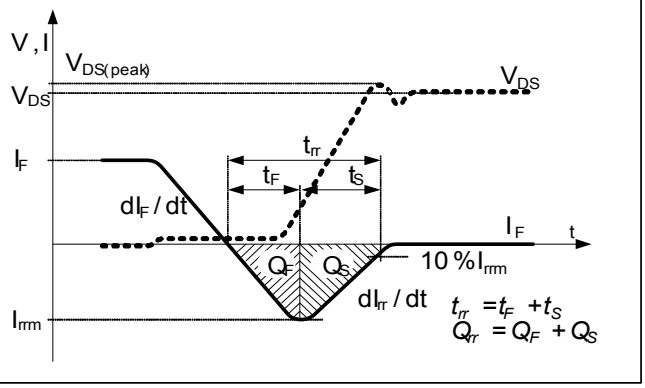
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

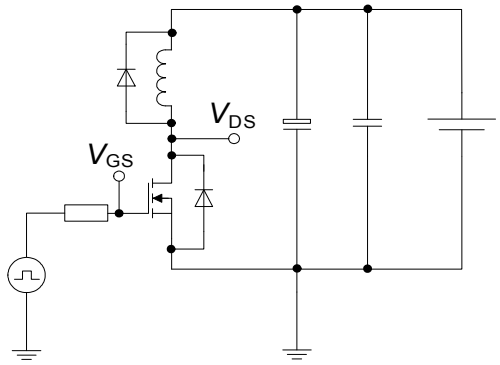
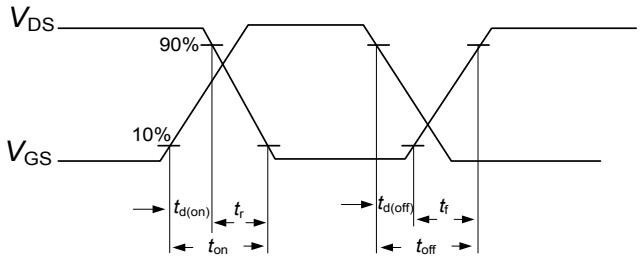
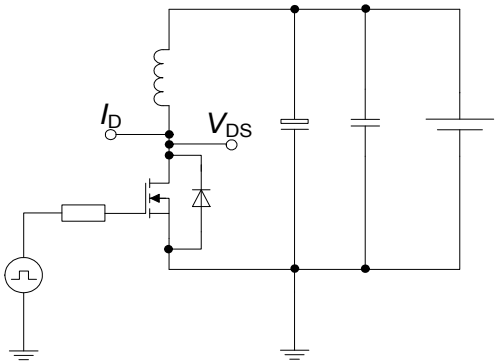
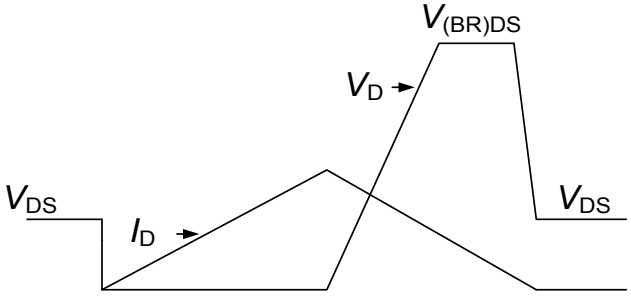
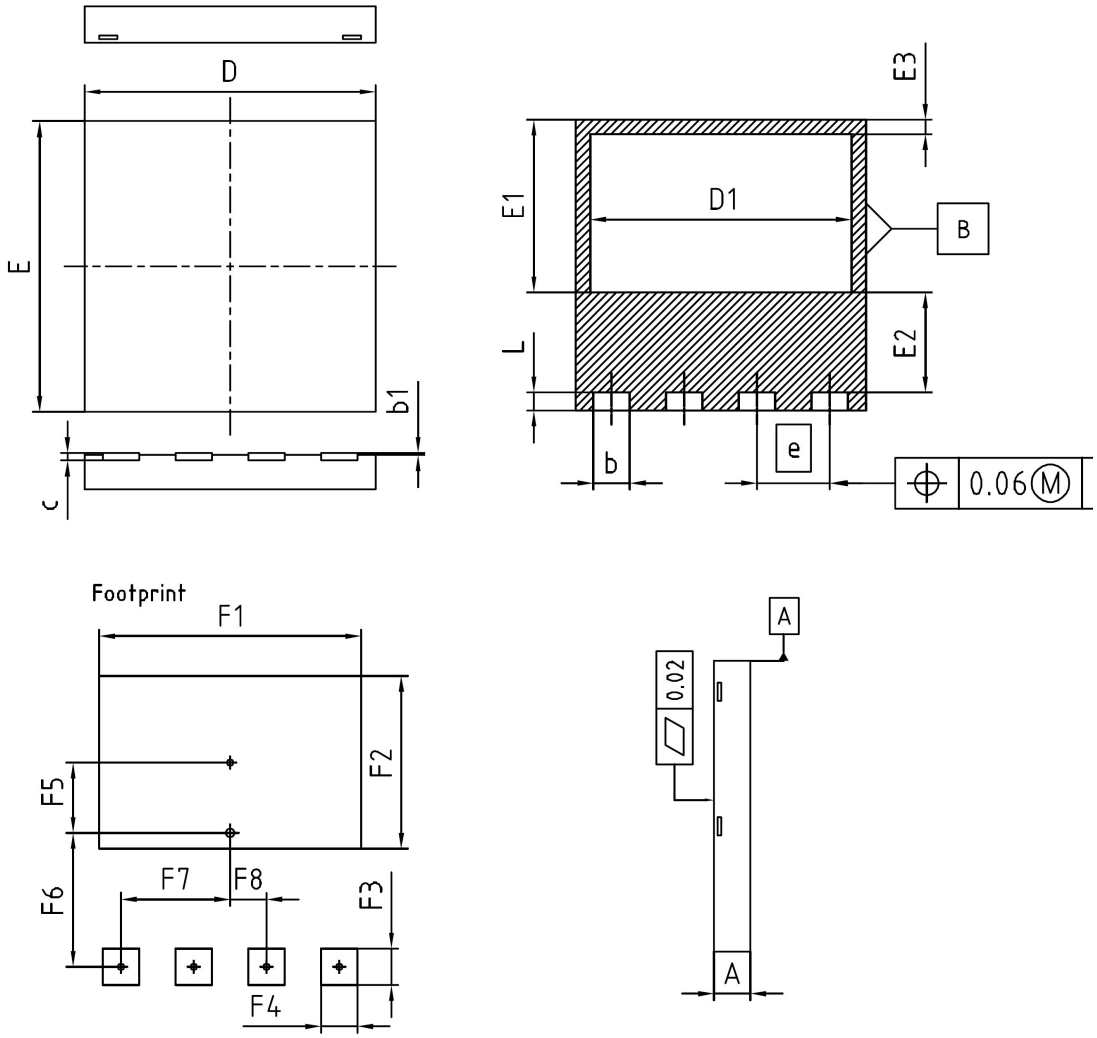
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.90	1.10	0.035	0.043
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.10	7.30	0.280	0.287
E	7.90	8.10	0.311	0.319
E1	4.65	4.85	0.183	0.191
E2	2.65	2.85	0.104	0.112
E3	0.30	0.50	0.012	0.020
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024
N	4		4	
F1	7.20		0.283	
F2	4.75		0.187	
F3	1.00		0.039	
F4	1.00		0.039	
F5	1.43		0.056	
F6	4.20		0.165	
F7	3.00		0.118	
F8	1.00		0.039	

DOCUMENT NO.
Z8B00156707

SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

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REVISION
01

Figure 1 Outline PG-VSON-4, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design Tools:** www.infineon.com

Revision History

IPL65R420E6

Revision: 2014-03-07, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2013-08-26	Release of final version
2.1	2014-03-07	Added in Features list: Qualified for industrial grade application

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