IPN10EL-S

PN Half Bridge Driver IC

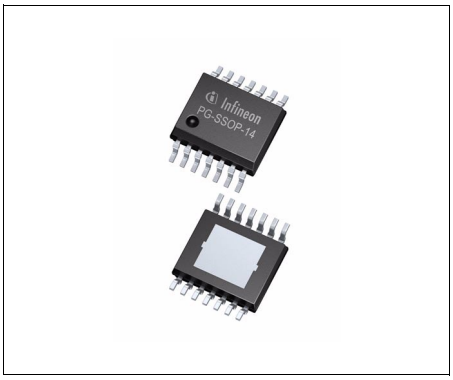
Data Sheet

Rev 1.1, 2014-01-21

Automotive Power

PN Half Bridge Driver IC

1 Overview



PG-SSOP-14

Features

- Driver IC for one P- and one N-Channel Power MOSFETs
- 0 ... 100 % Duty cycle of High- and Low Side MOSFETs
- Low quiescent current mode
- Adjustable dead time
- One Error output to µC
- Over temperature protection
- Under voltage lock out
- Green Product (RoHS compliant)
- AEC Qualified
- Programmable supply function for normal and logic level MOSFETs

Description

The IPN10EL-S is a gate driver IC dedicated to drive one p-channel and one n-channel MOSFET. Typically these two MOSFETs are used as one leg in a bridge topology forming the converter for DC motor drives in automotive applications. Due to the p-channel highside switch the need for a charge pump is eliminated thus minimizing electro magnetic interference (EMI). The driver IC contains an interface to the microcontroller, adjustable dead time generation and basic protection features like short circuit, undervoltage and overtemperature.

Table 1 Product Summary

Specified supply voltage range	V_{VS1}	Vs = VUVOFF to 40V
Junction temperature	T_j	Tj = -40 to +150°C
Quiescent current at VS[1)]	I_{qVS}	3 µA @ T_J = 105°C

1) typical value at T_j=15°C

Type	Package	Marking
IPN10EL-S	PG-SSOP-14	IPN10EL

2 Block Diagram

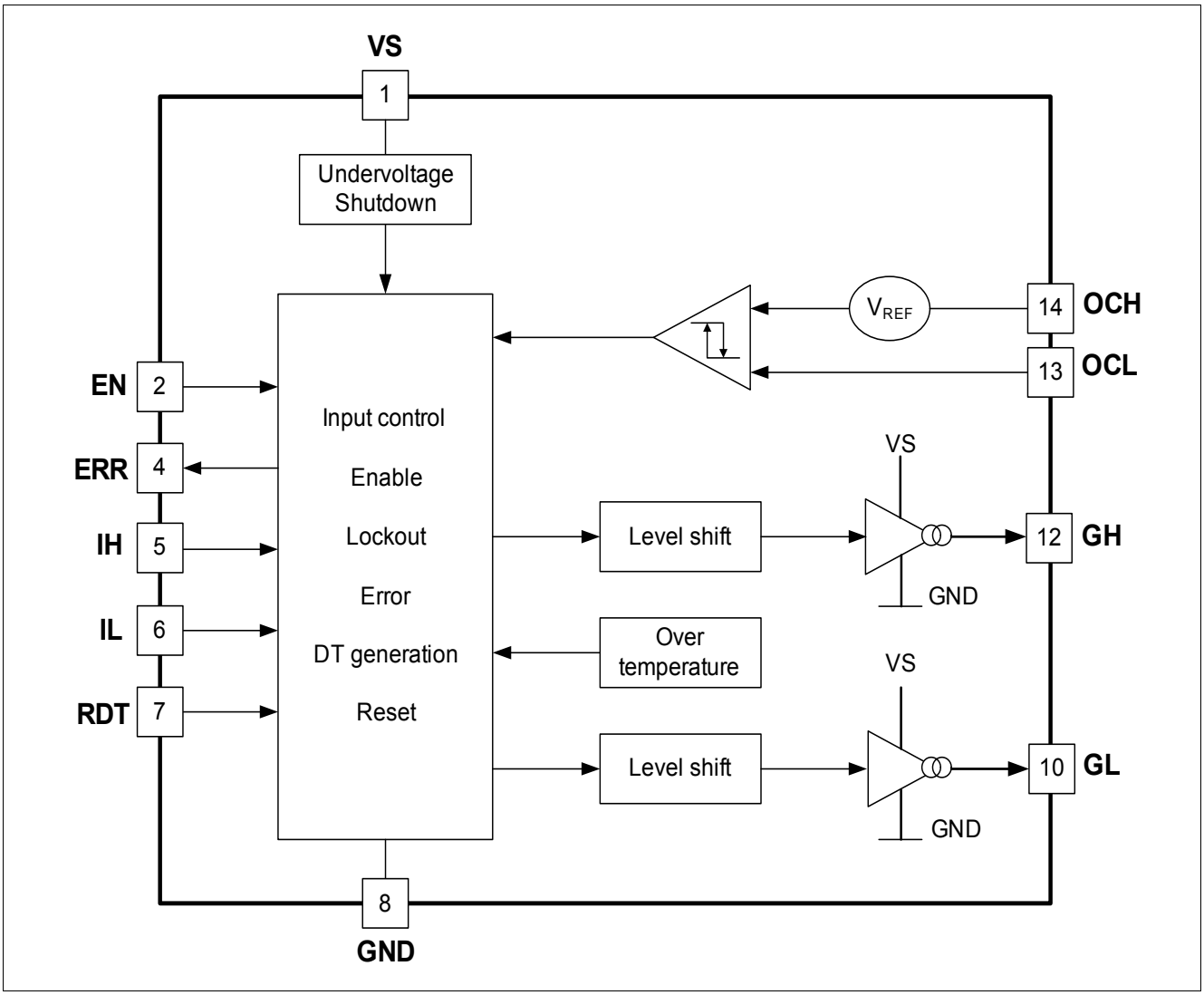


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

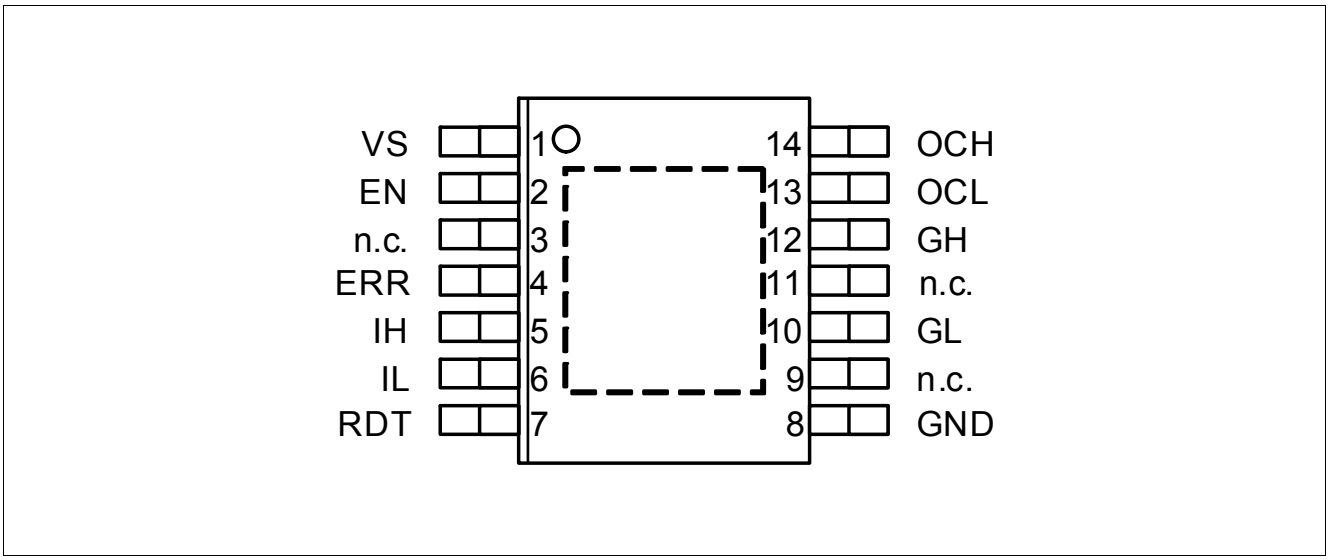


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

# of Pins	Symbol	Function
1	VS	Power supply
2	EN	Enable input (active high)
3	n.c.	not connected
4	ERR	Error output to µC (active low)
5	IH	Input for high side MOSFET (active low)
6	IL	Input for low side MOSFET (active high)
7	RDT	Dead time resistor to ground; no internal DT generation
8	GND	Ground
9	n.c.	not connected
10	GL	Gate output for low side MOSFET
11	n.c.	not connected
12	GH	Gate output for high side MOSFET
13	OCL	Shunt input for overcurrent detection - low side
14	OCH	Shunt input for overcurrent detection - high side

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_J ≤ -40 °C ≤ +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage at VS	V_S	-0.3	–	40	V	–	P_4.1.1
Voltage range at EN	V_{EN}	-0.3	–	40	V	–	P_4.1.2
Voltage range at OCL	V_{OCL}	-0.3	–	40	V	–	P_4.1.3
Voltage range at OCH	V_{OCH}	-0.3	–	40	V	–	P_4.1.4
Voltage between OCH and OCL	$V_{OCH-OCL}$	-0.3	–	0.3	V	–	P_4.1.5
Voltage range at RDT	V_{RDT}	-0.3	–	6	V	–	P_4.1.6
Voltage range at ERR	V_{ERR}	-0.3	–	6	V	–	P_4.1.7
Voltage range at GH	V_{GH}	-0.3	–	40	V	–	P_4.1.8
Voltage range at GL	V_{GL}	-0.3	–	10	V	–	P_4.1.9
Voltage between VS and GH	V_S-V_{GH}	-0.3	–	10	V	–	P_4.1.10
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.11
Storage temperature	T_{stg}	-40	–	150	°C	–	P_4.1.12
Lead soldering temperature (1/16'' from body)	T_{sol}	–	–	260	°C	–	P_4.1.13
Peak reflow soldering temperature[2)]	T_{ref}	–	–	260	°C	–	P_4.1.14
Power Dissipation							
Power Dissipation (DC) @ TCASE=140°C	P_{tot}	–	–	1	Ω	–	P_4.1.15
ESD Susceptibility							
ESD Resistivity[3)]	V_{ESD}	–	–	2	kV	–	P_4.1.16
CDM	V_{CDM}	–	–	1.5	kV	–	P_4.1.17

1) Not subject to production test, specified by design.
2) Reflow profile IPC/JEDEC J-STD-020C
3) ESD susceptibility HBM according to EIA/JESD 22-A 114B

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified supply voltage range	V_{VS1}	V_{UVOFF}	–	40	V	–	P_4.2.1
Duty cycle high side output stage	D_{HS}	0	–	100	%	–	P_4.2.2
Duty cycle low side output stage	D_{LS}	0	–	100	%	–	P_4.2.3
Minimum pulse width[1)]	t_{pulse}	5	–	–	µs	–	P_4.2.4

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case[1)]	R_{thJC}	–	–	10	K/W	–	P_4.3.1
Junction to Ambient	R_{thJA}	–	50	–	K/W	[2)]	P_4.3.2
Junction to Ambient	R_{thJA}	–	140	–	K/W	Footprint only[3)]	P_4.3.3
Junction to Ambient	R_{thJA}	–	60	–	K/W	300mm^2 footprint area on PCB	P_4.3.4
Junction to Ambient	R_{thJA}	–	50	–	K/W	600mm^2 footprint area on PCB	P_4.3.5

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

5 Description and Electrical Characteristics

5.1 MOSFET Driver

The Driver IC IPN10EL-S level shifts, amplifies and buffers the control signals coming from the µC to provide the gate charge for the High Side and Low Side MOSFET. It acts as the interface between the µC and the power MOSFETs.

5.1.1 Driving MOSFET Output Stages

By applying a High signal on the enable pin (EN), the IPN10EL-S will be activated and the two output stages can be used.

By leaving the dead time pin (RDT) open (a resistor of 1MOhm between RDT and GND is recommended to avoid noise coupling) or shorted to ground, the high side MOSFET and the low side MOSFET can be individually controlled by the IH and IL pin. Any kind of PWM pattern can be generated.

Additionally the IPN10EL-S offers the possibility of an internal deadtime generation / shoot-through protection. By applying an external resistor between the RDT pin and GND, the value for the deadtime will be determined. Using the internal dead time generation, the IH input will be disabled. The MOSFETs will be switched on and off alternating by the IL input only.

5.1.2 Dead Time

IPN10EL-S offers a flexible concept for the deadtime generation. Both driver stages can be 100% controlled individually, thus providing full compatibility to any application requirement (e.g. driving an injector with the load is connected between the high side MOSFET and the low side MOSFET).

For drives applications, where the p-channel and the n-channel MOSFETs are connected in serial, it has to be avoided that both MOSFETs are turned on at the same time. The IPN10EL-S offers an internal dead time generation to avoid cross conduction via these two devices. The deadtime can be adjusted by an external resistor between the RDT pin and GND over a wide range (200ns up to 2µs).

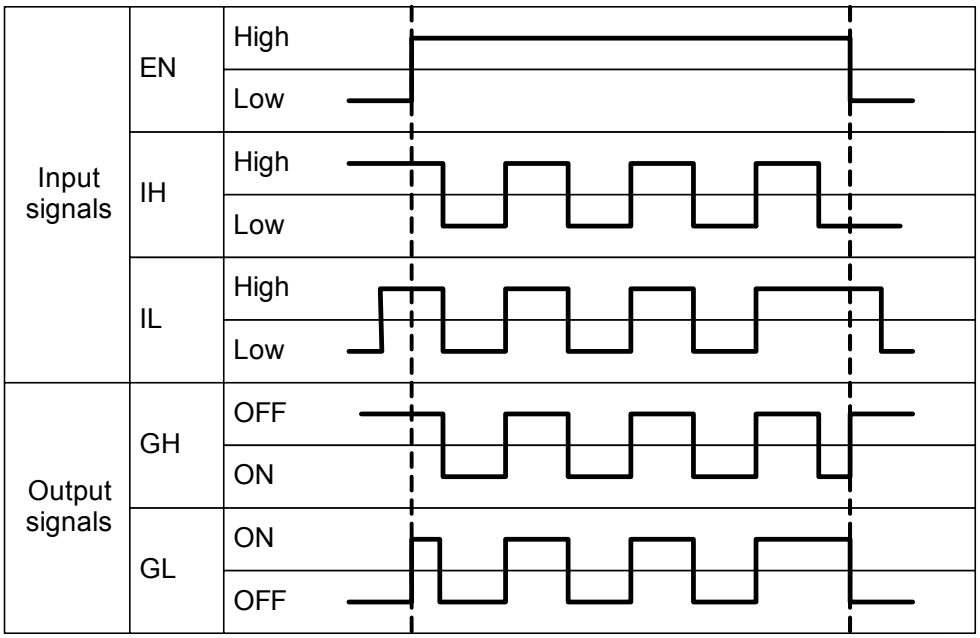
External dead time generation with open RDT pin

IH	High side MOSFET	IL	Low side MOSFET
0	ON	0	OFF
1	OFF	1	ON

Internal dead time generation using the RDT pin to set the value

IH	High side MOSFET	IL	Low side MOSFET
no influence	ON	0	OFF
no influence	OFF	1	ON

External dead time generation



Internal dead time generation

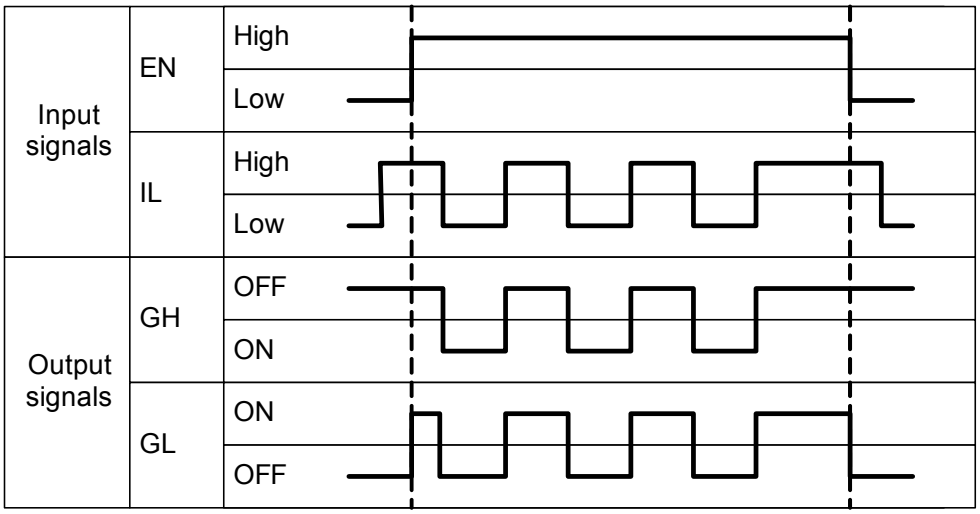


Figure 3 Timing diagram PWM/interface

5.1.3 MOSFET Output Stages

The lowside and highside driver stages of the IPN10EL-S are realized as a push pull stage. The Gate to Source voltage is regulated to typical values of 10V. Due to the fact that a p-channel MOSFET will be driven as the high side switch, no charge pump or bootstrap circuits are required. The high side driver refers to VS or battery whereas the low side driver refers to Ground. Due to absence of a charge pump with its high switching frequencies the EMI of the product is improved.

Duty cycles in between 0% to 100% for both channels are possible.

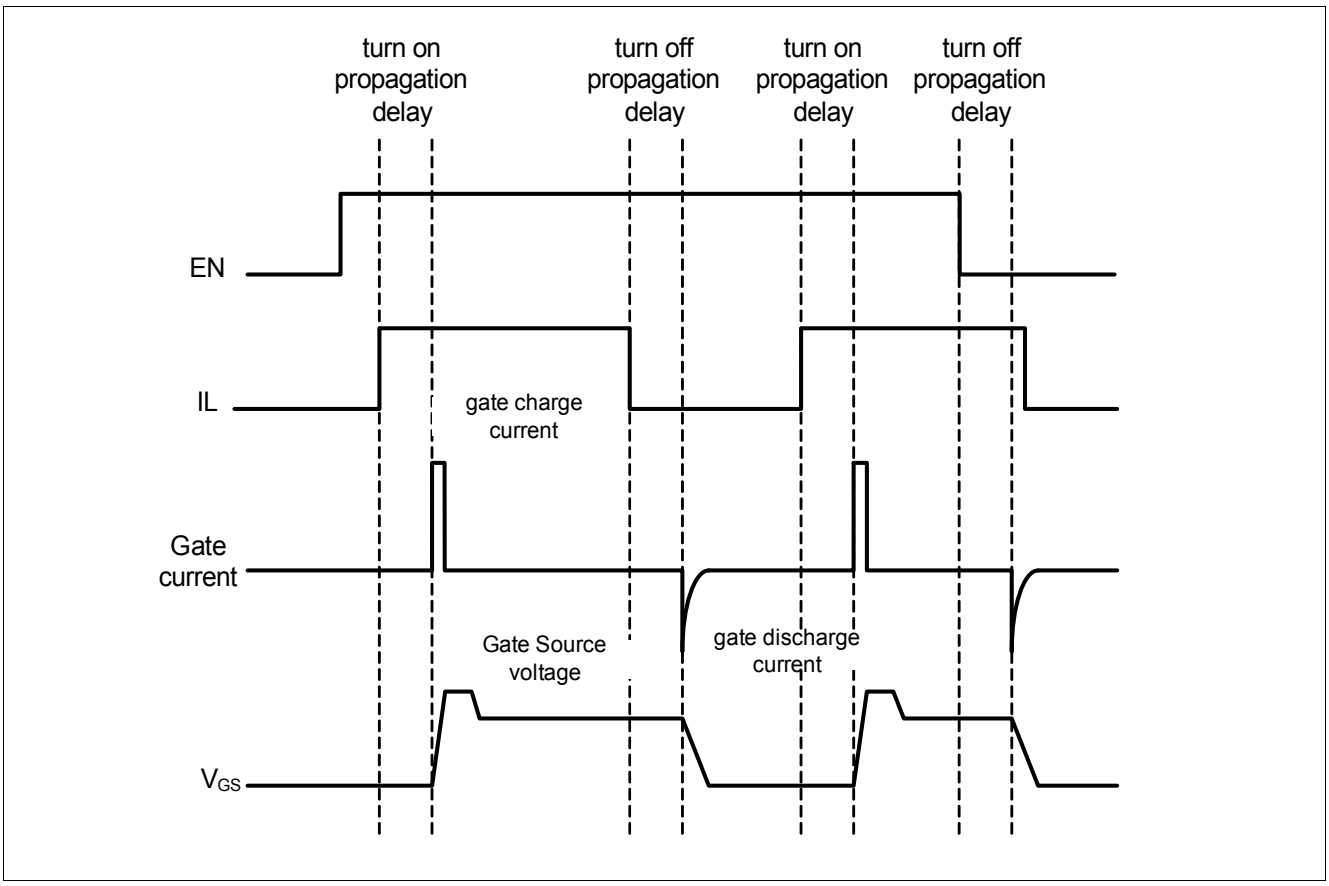


Figure 4 Principle operation of output stage (example: low side driver)

5.1.4 Start up procedure

The status and behavior of the ERR pin during start up of the driver IC depends on the EN input. If the EN input is low, the ERR output is high, due to missing internal supply voltage. If the EN pin rises up, the ERR pin goes to low as long as the internal supply is below the threshold of the logic. If the EN pin is high, the ERR goes to high.

For a proper start up behavior it is recommended to use following sequence:

1. Provide the supply voltage
2. Set IL to high (low) level
3. Switch EN from low to high
4. Toggle IL to low (high) level with a minimum pulse of 200ns length

5.1.5 Electrical Characteristics

Table 5 Electrical Characteristic MOSFET Drivers

V_S = V_{UVOFF} to 40V, T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Control inputs							
Low level input voltage of IH	V_{IH_LL}	–	–	0.8	V	tested at V_S =18V	P_5.1.5
High level input voltage of IH	V_{IH_HL}	3.5	–	–	V		P_5.1.6
Input hysteresis of IH	d_{VIH}	100	400	–	mV		P_5.1.7
IH pull-up current	I_{IHH}	-6.0	-3.0	-1.0	µA	EN=5V, VS=18V, IH=1V	P_5.1.8
Low level input voltage of IL	V_{IL_LL}	–	–	0.8	V	tested at V_S =18V	P_5.1.9
High level input voltage of IL	V_{IL_HL}	3.5	–	–	V		P_5.1.10
Input hysteresis of IL	d_{VIL}	100	400	–	mV		P_5.1.11
IL pull-up current	I_{ILH}	-6.0	-3.0	-1.0	µA	EN=5V, VS=18V, IL=1V, int deadtime	P_5.1.12
IL pull-down resistor to GND	R_{ILL}	0.35	0.8	1.4	MΩ	EN=5V, VS=18V, IL=4V, external deadtime	P_5.1.13
MOSFET driver output							
Gate peak current high side	I_{GHP}	–	400	–	mA	C_{Load}=16nF; V_S=18V; 10-90%	P_5.1.14
Gate peak current low side	I_{GLP}	–	400	–	mA		P_5.1.15
Gate Source voltage high side	V_{GSH}	-14	–	–	V		P_5.1.16
Gate Source voltage low side	V_{GSL}	–	–	14	V		P_5.1.17
Rise time	t_{rise}	–	380	–	ns		P_5.1.18
Fall time	t_{fall}	–	380	–	ns		P_5.1.19
Gate Charge	Q_{Gtot}	–	–	288	nC		P_5.1.20
Dead time & input propagation delay times measured at 10% (90%) of the rising (falling) edge							
Programmable internal dead time logic level MOSFETs[1)]	t_{DT}	0.14 1.4	0.21 2.1	0.28 2.8	µs	R_{DT}=18kΩ R_{DT}=180kΩ; V_S=18V	P_5.1.21
Programmable internal dead time normal level MOSFETs[1)]	t_{DT}	0.14 1.4	0.21 2.1	0.28 2.8	µs	R_{DT}=1kΩ R_{DT}=10kΩ; V_S=18V	P_5.1.22
Input propagation time (low on)	$t_{P(ILN)}$	–	100	250	ns	V_S=18V; tested with no load condition	P_5.1.23
Input propagation time (low off)	$t_{P(ILF)}$	–	100	250	ns		P_5.1.24
Input propagation time (high on)	$t_{P(IHN)}$	–	100	250	ns		P_5.1.25
Input propagation time (high off)	$t_{P(IHF)}$	–	100	250	ns		P_5.1.26
Absolute input propagation time difference between above propagation times see figure 5	$t_{P(diff)}$	–	50	150	ns		P_5.1.27
Enable and low quiescent current mode							
EN propagation time to output stages switched off	t_{PENA_H-L}	–	2.0	3.0	µs	–	P_5.1.28

Table 5 Electrical Characteristic MOSFET Drivers

V_S = V_{UVOFF} to 40V, T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Quiescent current at VS	I_{qVS}	-	-	3	µA	V_S=18V; EN=0V; T_J=105°C	P_5.1.29
Supply current at VS (device enable)	I_{VS}	-	5.0	7.0	mA	no switching; R_{DT}=10kΩ; V_S=18V; EN=high	P_5.1.30
Supply current at VS (device enable)	I_{VS}	-	25	35	mA	C_{Load}=16nF; f=20kHz; V_S=18V; R_{DT}=10kΩ	P_5.1.31

1) Not subject to production test, specified by design.

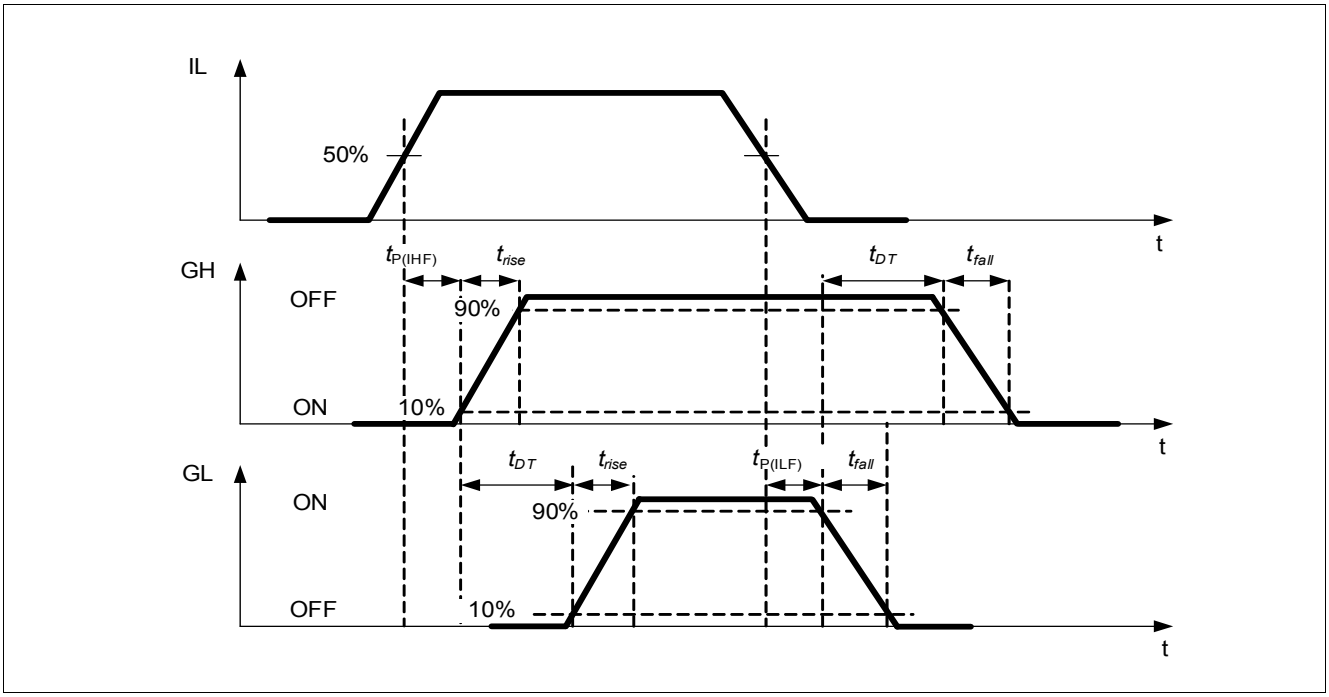


Figure 5 Definition of timings

5.2 Protection and Diagnoses Functions

5.2.1 VS Under Voltage lock out

The IPN10EL-S has an integrated VS Under Voltage lock out to assure that the behavior of the complete IC is predictable in all supply voltage ranges. As soon as the under voltage threshold V_{UVOFF} is reached for a specified filter time the IPN10EL-S will set the ERR flag and turn off.

The undervoltage lock out level is programmable by the external dead time resistor applied to the RDT pin. Depending on the resistor range, the undervoltage lock out will be adjusted for operation with logic level MOSFETs or normal level MOSFETs. The range of 1kΩto 10kΩ will adjust the lockout for normal level MOSFETs, the range of 18kΩ to 180kΩ for logic level MOSFETs.

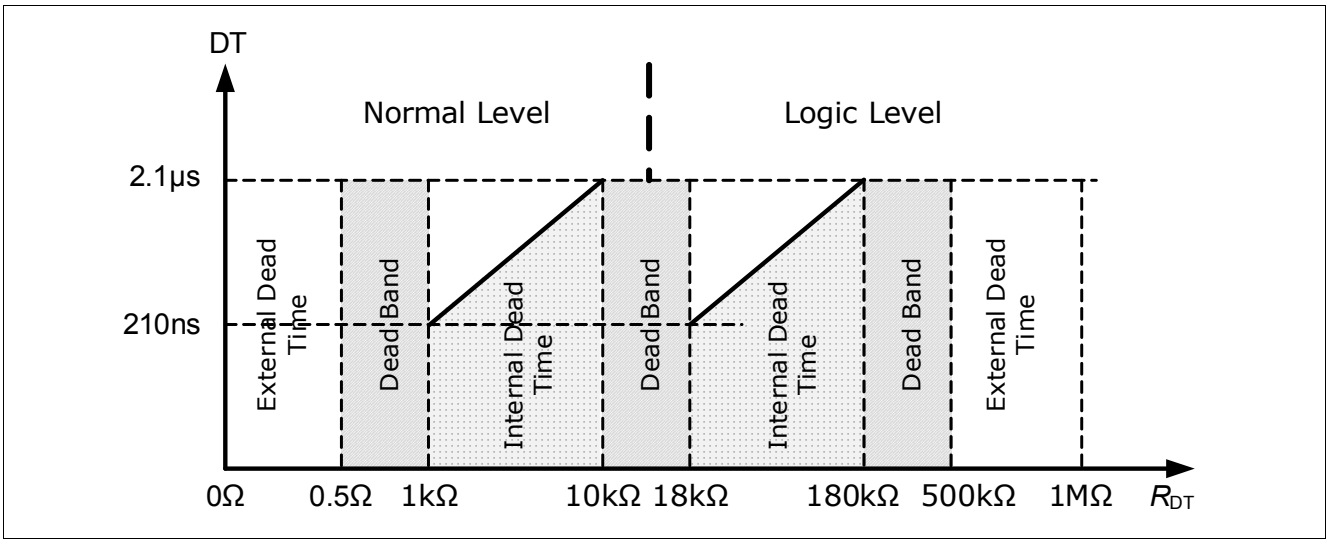


Figure 6 Internal dead time adjustment

5.2.2 Over Temperature shut down

The IPN10EL-S provides an integrated digital over temperature shut down to avoid destruction of the IC at high temperature. The temperature will be detected by a temperature sensor. During over temperature warning the ERR signal is set to low and the IPN10EL-S turns off the high side and low side MOSFET.

5.2.3 Over Current shut down

The IPN10EL-S provides an integrated overcurrent shut down to avoid destruction of the MOSFETs during a short circuit of the application. The current will be measured via an external shunt resistor. During over current detection the ERR signal is set to low and the IPN10EL-S turns off the high side and low side MOSFET.

Please note that a short of the OCL pin to battery will override the overcurrent detection (under the assumption that OCH is connected to battery). A short between OCL and OCH will override the overcurrent detection as well.

5.2.4 ERR Pin

The IPN10EL-S has a status pin to provide diagnostic feedback to the µC. The logical output of this pin is open Drain circuit. An external pull up resistor has to be implemented for functionality and to limit the current into the pin; connecting the ERR pin to a supply voltage may damage the device.

The IPN10EL-S can be reset by the enable pin EN. If the EN pin is pulled to low for a minimum time of 5µs, the error registers are cleared. If the EN pin is pulled to low, the ERR output should be ignored due to missing internal supply voltage. For start up, please refer to 5.1.4.

Table 6 Overview of error condition

ERR	Driver conditions	Driver action	Restart
High	no errors	Fully functional	–
Low	Over temperature	high side and low side MOSFETs switched off	restart
Low	Overcurrent	high side and low side MOSFETs switched off	latched
Low	Under voltage lock out	high side and low side MOSFETs switched off	restart

5.2.5 Electrical Characteristics

Table 7 Electrical Characteristic - Protection and Diagnostic functions

V_S = V_{UVOFF} to 40V, T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Under voltage lock out							
Under voltage lock out at Vs, logic level MOSFET	V_{UVOFF}	4.0	4.5	–	V	V_S decreasing	P_5.2.1
Under voltage lock out at Vs, normal level MOSFET	V_{UVOFF}	6.5	7.5	–	V		P_5.2.2
Under voltage lock out filter time for VS	t_{UVLO}	–	25	–	µs		P_5.2.3
Temperature monitoring							
Over temperature warning	$T_{j(PW)}$	150	170	200	°C	–	P_5.2.4
Hysteresis for over temperature warning	$dT_{j(OW)}$	–	10	–	°C	–	P_5.2.5
Over current detection							
Over current detection level	V_{OCTH}	30	50	70	mV	V_S=V_{OCH} =18V	P_5.2.6
Filter time for over current detection	t_{OC}	4	–	12	µs	V_S=V_{OCH} =18V	P_5.2.7
Time to clear error register	t_{ENL}	5	–	–	µs	V_S=V_{OCH} =18V	P_5.2.8
ERR pin							
Error output low current	I_{ERRL}	–	–	1.1	mA	V_{ERR}<0.4V, tested at VS=18V	P_5.2.9
Error output low voltage	V_{ERR}	–	0.15	0.25	V	ISO<200µA, tested at VS=18V	P_5.2.10
Error high leakage current	I_{ERRLK}	–	–	3	µA	tested at VS=18V	P_5.2.11

6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

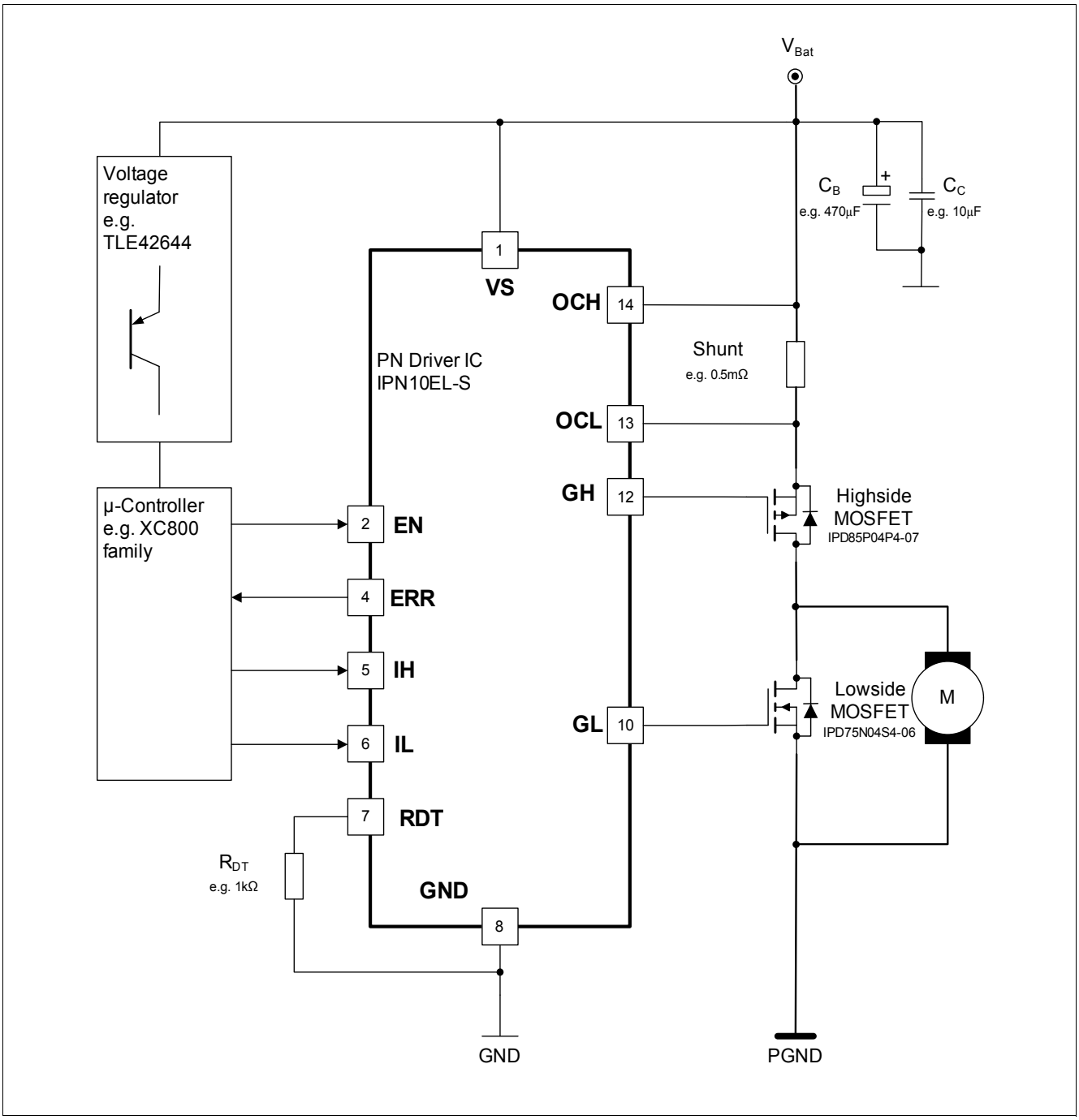


Figure 7 Application Diagram - DC-Brush motor controlled by IPN10EL-S

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

6.1 Layout Guide Lines

Please refer also to the simplified application example.

- One separated bulk capacitor CB should be used
- One separated ceramic capacitor CC should be used
- Both capacitors CB and CC should be placed very close to the power MOSFETs
- The components within the half bridge should be placed close to each other: high side MOSFET, low side MOSFET, bulk capacitor CB and ceramic capacitor CC (CB and CC are in parallel) and the shunt resistor form a loop that should be as small and tight as possible. The traces should be short and wide
- The connection between the drain of the high side MOSFET and the drain of the low side MOSFET should be as low inductive and as low resistive as possible.
- Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors)
- The exposed pad on the backside of the package should be connected to GND
- The R_{DT} resistor should be placed as close as possible to the RDT pin; no additional capacitance is allowed on the RDT pin
- The shunt resistor for over current detection should be placed as close as possible to the OCL and OCH pin.
- If the driver IC operates without internal dead time generation, the RDT pin should be connected either to GND or a 1MOhm resistor should be applied between RDS and GND to avoid noise coupling.
- If the driver IC operates in internal mode (internal dead time generation), the IH pin should be connected to ground.

6.2 Further Application Information

- For further information you may contact **http://www.infineon.com/**

7 Package Outlines

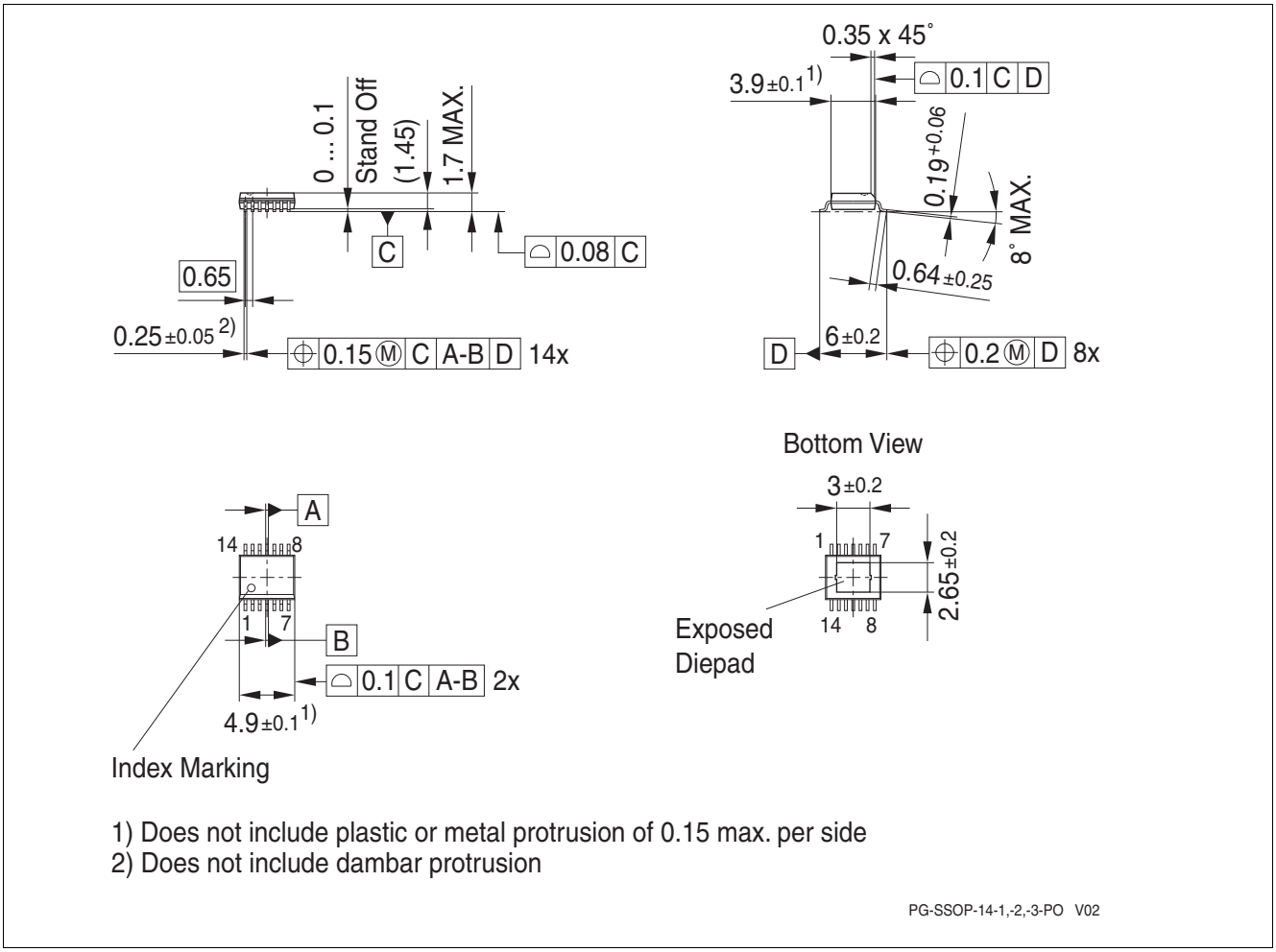


Figure 8 PG-SSOP-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb?free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision History

Revision	Date	Changes
1.1	2014-01-21	Update of marking
1.0	2013-06-12	Initial Data Sheet

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