

# MOSFET

## 650V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.



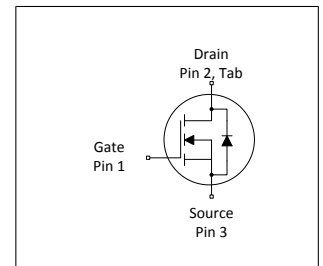
### Features

- Extremely low losses due to very low FOM  $R_{DS(on)} \cdot Q_g$  and  $E_{oss}$
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

### Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor lighting.

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	650	mΩ
$I_D$	10.1	A
$Q_{g,typ}$	23	nC
$I_{D,pulse}$	18	A
$E_{oss@400V}$	2	μJ

Type / Ordering Code	Package	Marking	Related Links
IPS65R650CE	PG-TO 251	65S650CE	see Appendix A

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	10.1 6.4	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	18	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	142	mJ	$I_D=1.3\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 11
Avalanche energy, repetitive	$E_{AR}$	-	-	0.21	mJ	$I_D=1.3\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 11
Avalanche current, repetitive	$I_{AR}$	-	-	1.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots480\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation (Non FullPAK) TO-252	$P_{tot}$	-	-	86	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	$I_S$	-	-	7.1	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	18	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 9
Maximum diode commutation speed	di <sub>f</sub> /dt	-	-	500	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 9

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum duty cycle  $D=0.50$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_G$

## 2 Thermal characteristics

**Table 3 Thermal characteristics TO-252**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	1.45	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm <sup>2</sup> (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave & reflow soldering allowed	$T_{sold}$	-	-	260	°C	reflow MSL1

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	$V_{DS}=V_{GS}, I_D=0.21mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=650, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=650, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.54	0.65	$\Omega$	$V_{GS}=10V, I_D=2.1A, T_j=25^\circ C$ $V_{GS}=10V, I_D=2.1A, T_j=150^\circ C$
Gate resistance	$R_G$	-	10.5	-	$\Omega$	$f=1MHz, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	440	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Output capacitance	$C_{oss}$	-	30	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	21	-	pF	$V_{GS}=0V, V_{DS}=0...480V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	88	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...480V$
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=3.2A,$ $R_G=6.8\Omega; \text{see table 10}$
Rise time	$t_r$	-	8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=3.2A,$ $R_G=6.8\Omega; \text{see table 10}$
Turn-off delay time	$t_{d(off)}$	-	64	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=3.2A,$ $R_G=6.8\Omega; \text{see table 10}$
Fall time	$t_f$	-	11	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=3.2A,$ $R_G=6.8\Omega; \text{see table 10}$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	2.75	-	nC	$V_{DD}=480V, I_D=3.2A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	$Q_{gd}$	-	12	-	nC	$V_{DD}=480V, I_D=3.2A, V_{GS}=0 \text{ to } 10V$
Gate charge total	$Q_g$	-	23	-	nC	$V_{DD}=480V, I_D=3.2A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	$V_{DD}=480V, I_D=3.2A, V_{GS}=0 \text{ to } 10V$

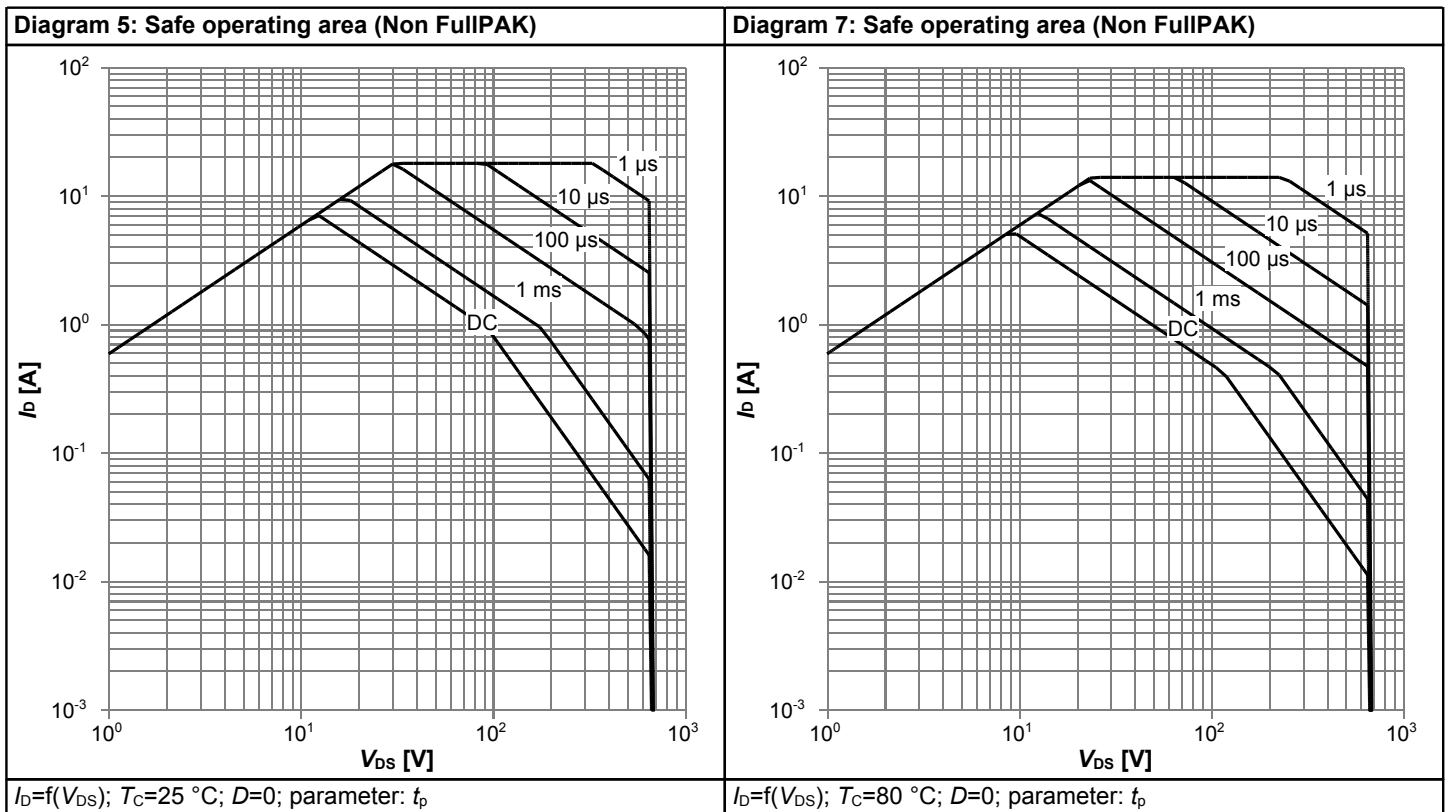
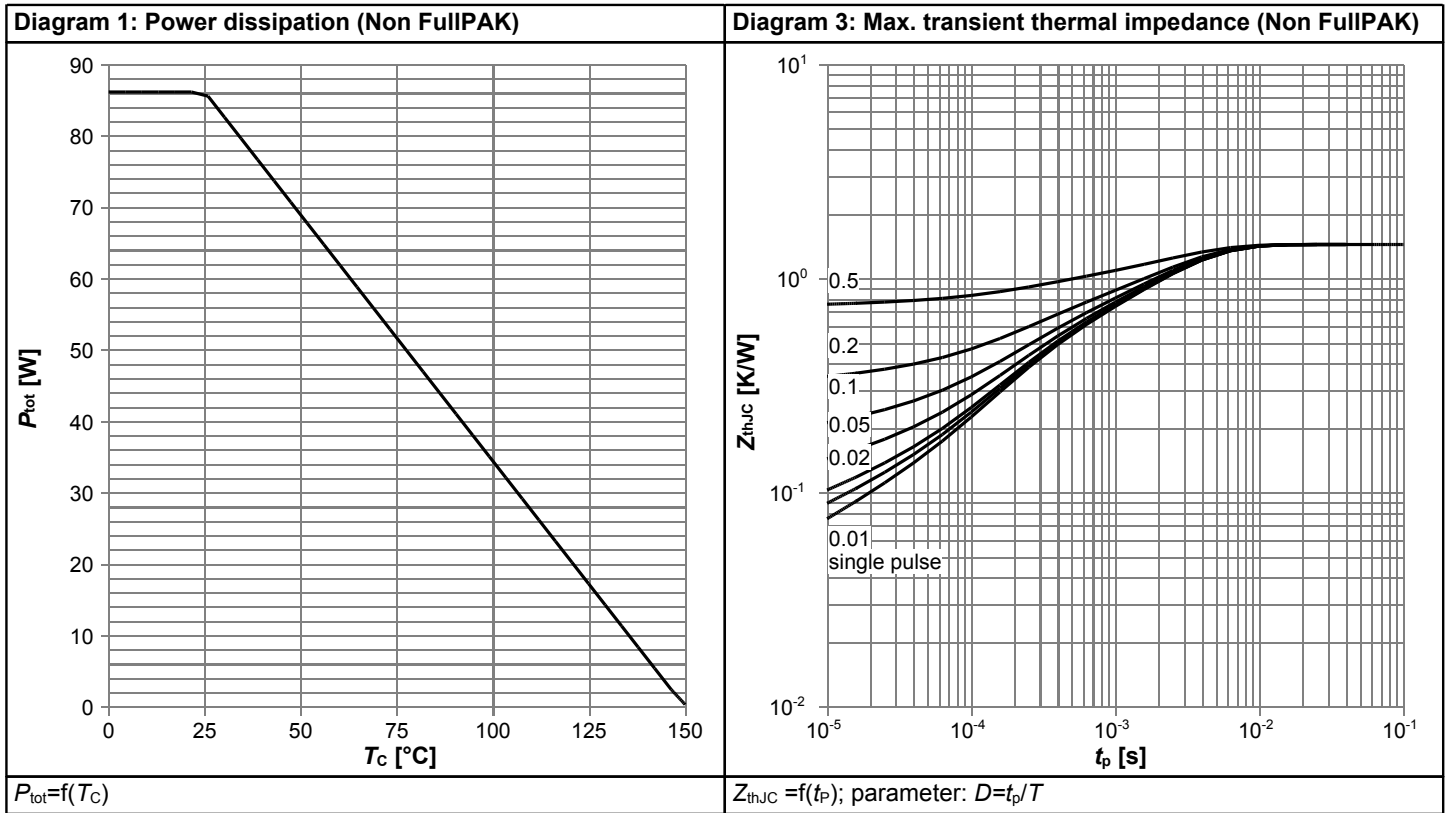
<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{o(BR)DSS}$

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{o(BR)DSS}$

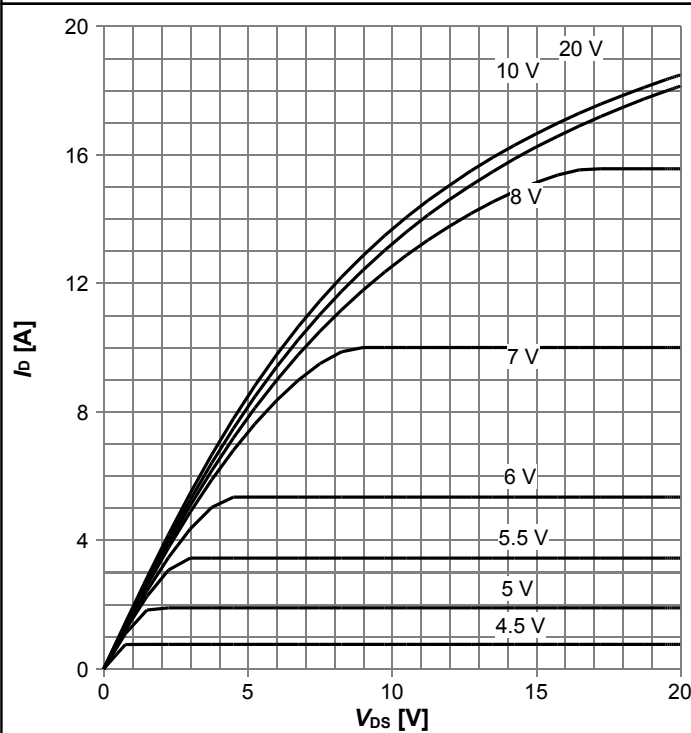
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=3.2A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	270	-	ns	$V_R=400V, I_F=3.2A, di_F/dt=100A/\mu s$ ; see table 9
Reverse recovery charge	$Q_{rr}$	-	2	-	$\mu C$	$V_R=400V, I_F=3.2A, di_F/dt=100A/\mu s$ ; see table 9
Peak reverse recovery current	$I_{rrm}$	-	13	-	A	$V_R=400V, I_F=3.2A, di_F/dt=100A/\mu s$ ; see table 9

4 Electrical characteristics diagrams

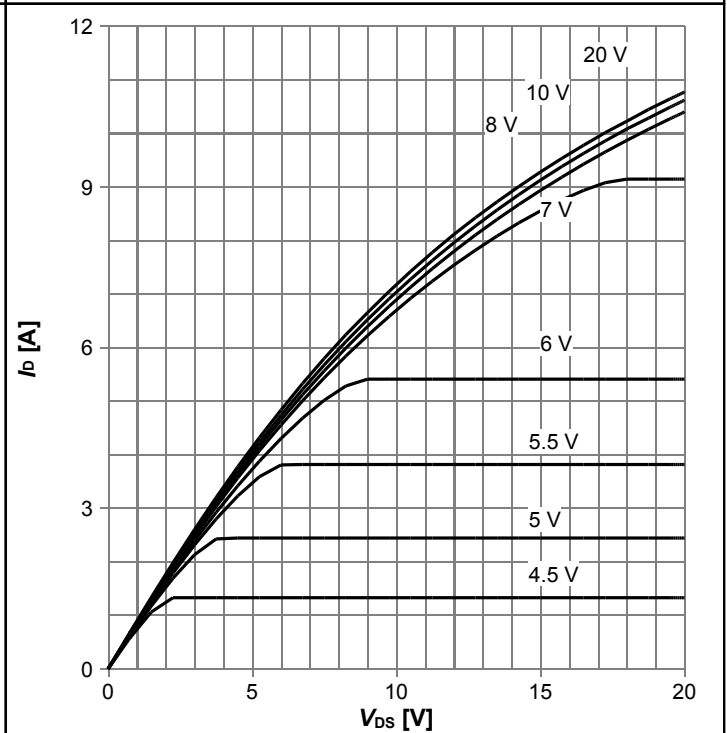


**Diagram 9: Typ. output characteristics**



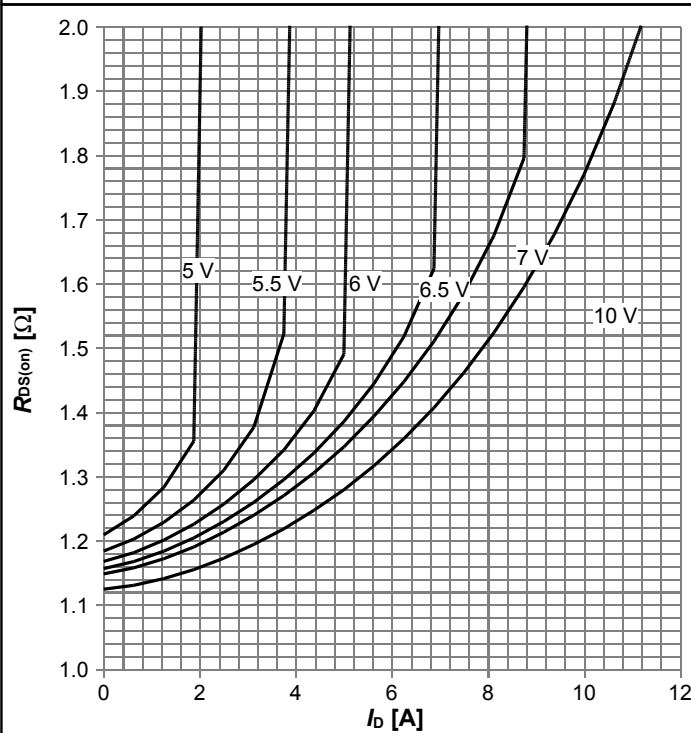
$I_D=f(V_{DS})$ ;  $T_j=25\text{ °C}$ ; parameter:  $V_{GS}$

**Diagram 10: Typ. output characteristics**



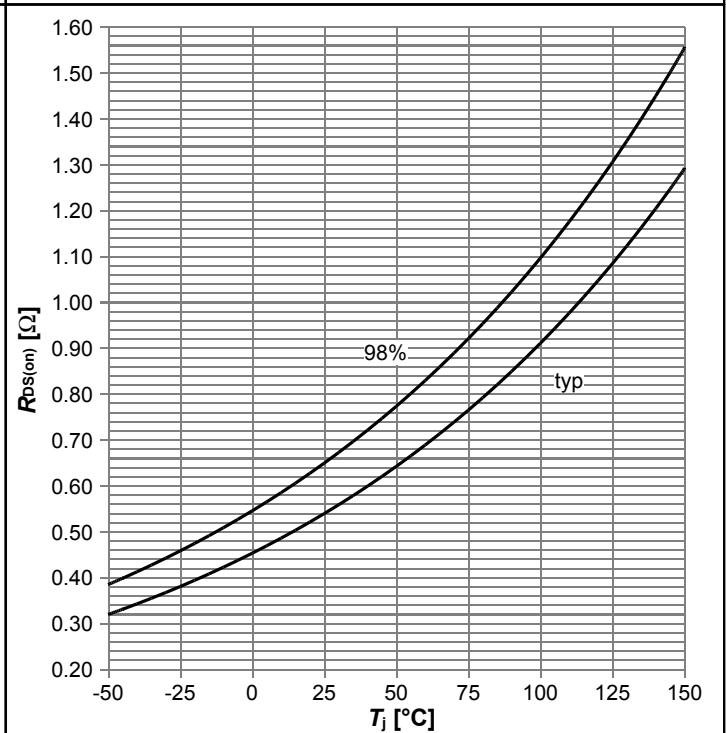
$I_D=f(V_{DS})$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

**Diagram 11: Typ. drain-source on-state resistance**



$R_{DS(on)}=f(I_D)$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

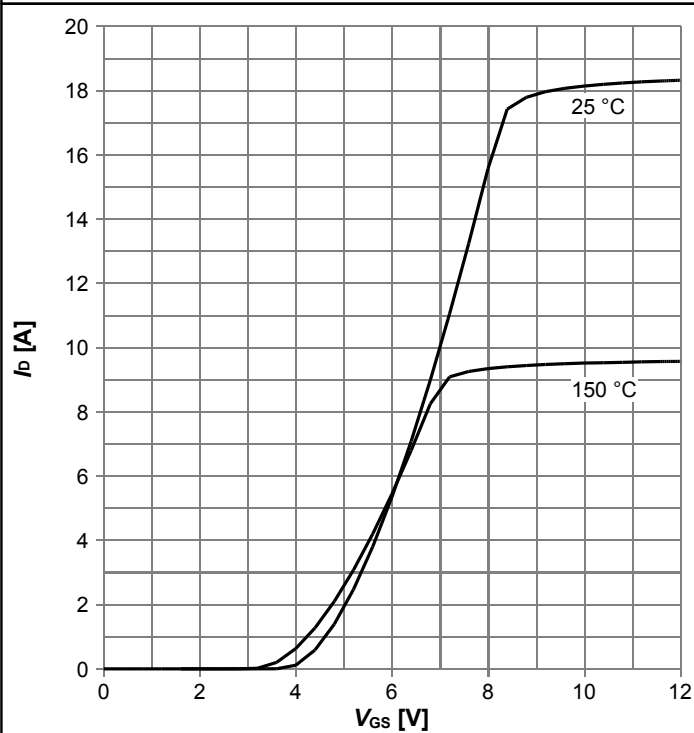
**Diagram 12: Drain-source on-state resistance**



$R_{DS(on)}=f(T_j)$ ;  $I_D=2.1\text{ A}$ ;  $V_{GS}=10\text{ V}$

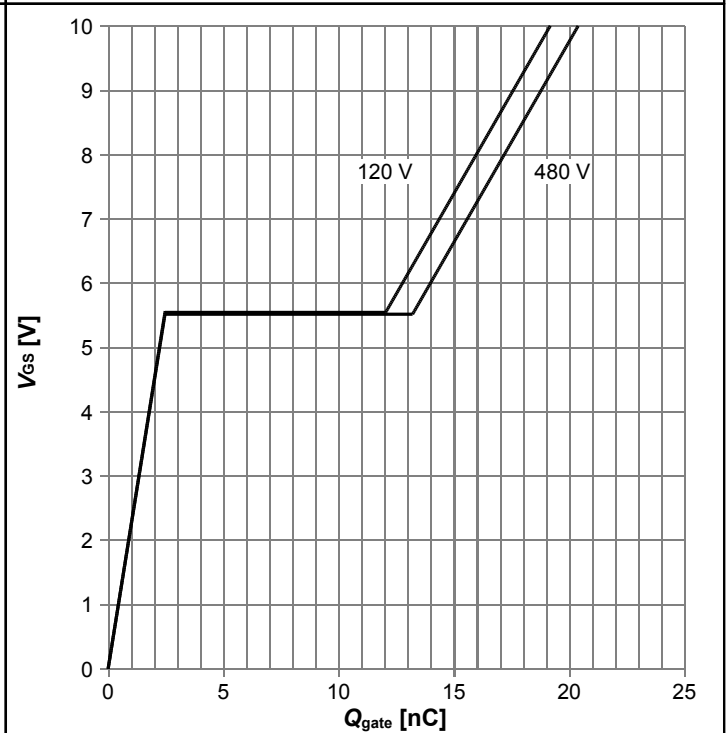


**Diagram 13: Typ. transfer characteristics**



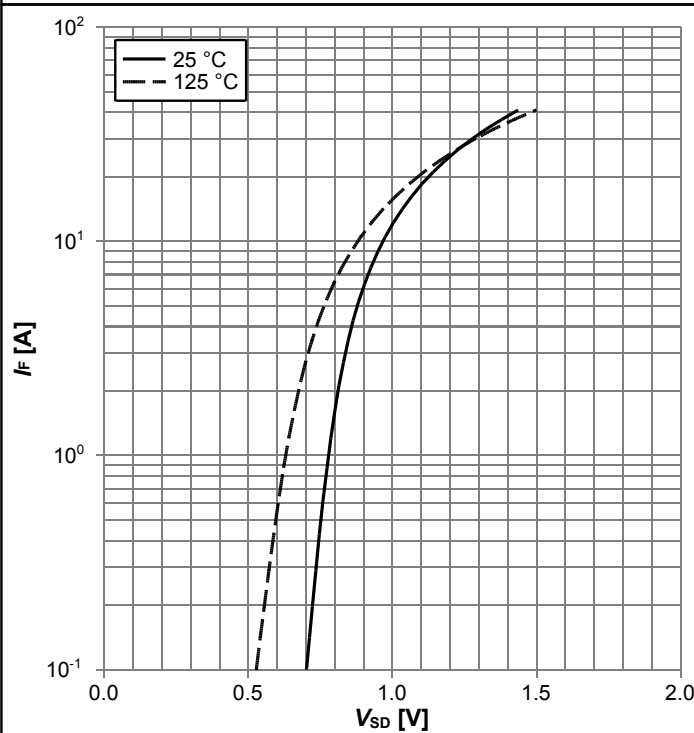
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

**Diagram 14: Typ. gate charge**



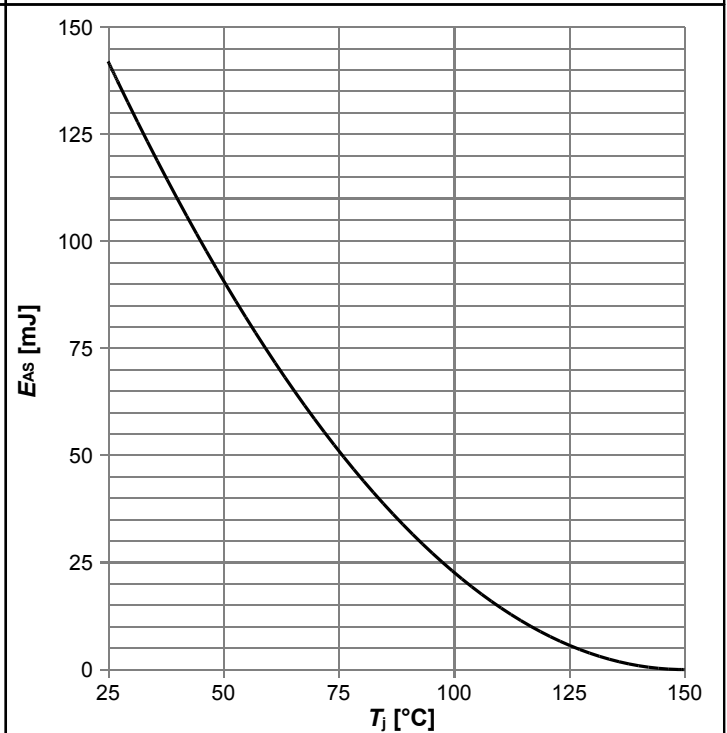
$V_{GS} = f(Q_{gate}); I_D = 3.2 \text{ A pulsed}; \text{parameter: } V_{DD}$

**Diagram 15: Forward characteristics of reverse diode**



$I_F = f(V_{SD}); \text{parameter: } T_j$

**Diagram 16: Avalanche energy**

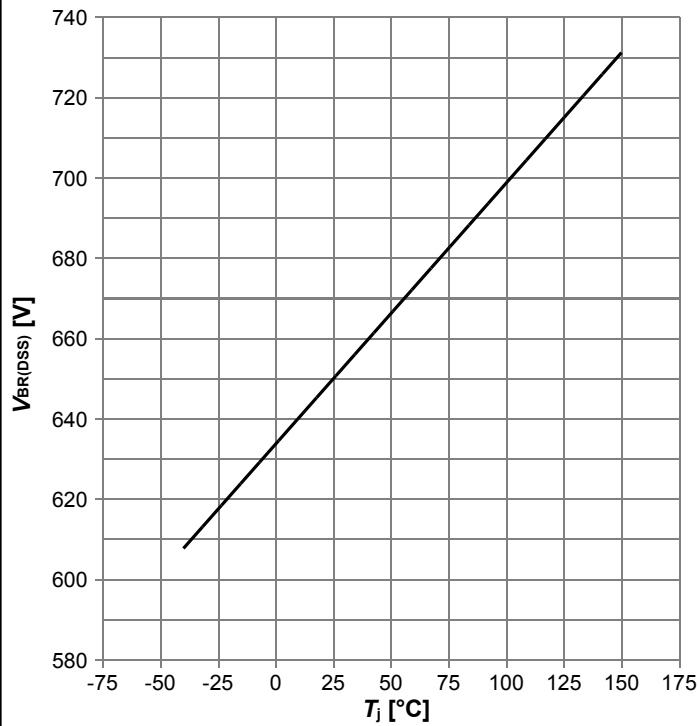


$E_{AS} = f(T_j); I_D = 1.3 \text{ A}; V_{DD} = 50 \text{ V}$

# 650V CoolMOS™ CE Power Transistor

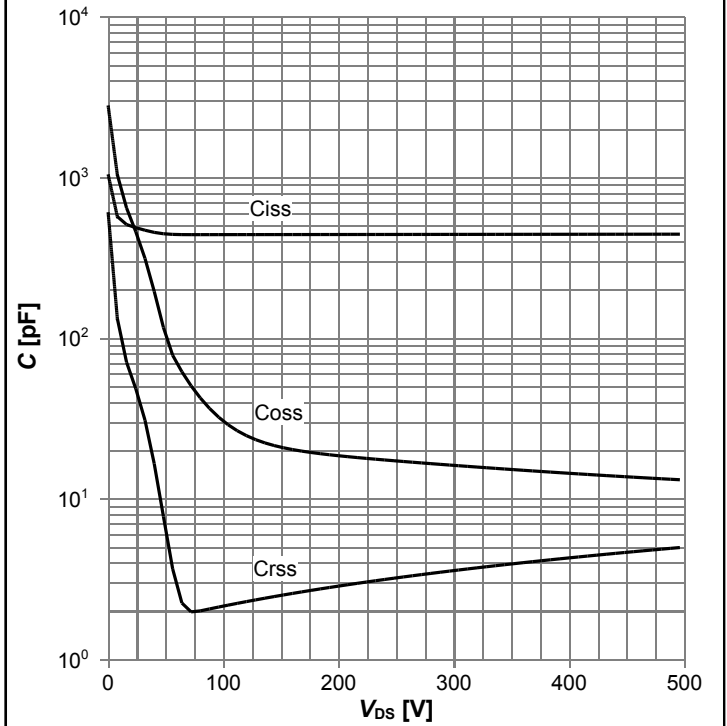
## IPS65R650CE

**Diagram 17: Drain-source breakdown voltage**



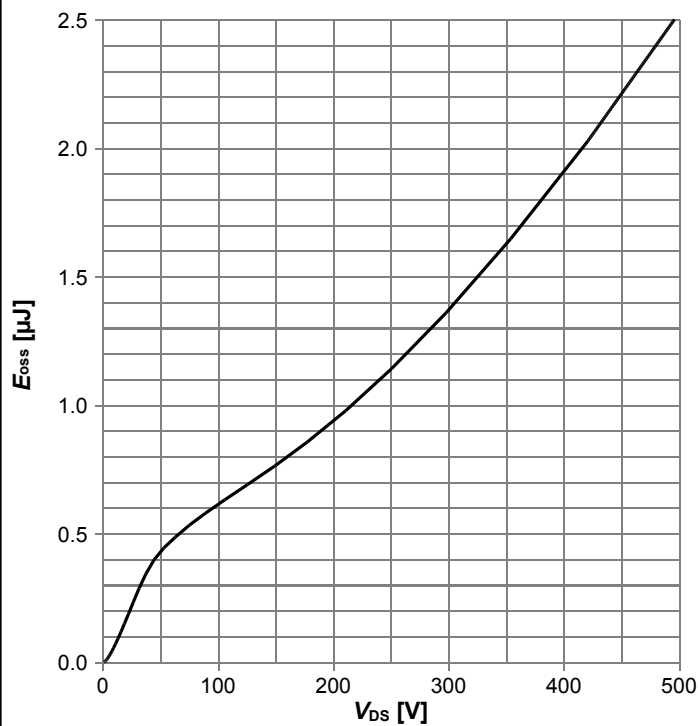
$V_{BR(DSS)}=f(T_j); I_D=1.0 \text{ mA}$

**Diagram 18: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

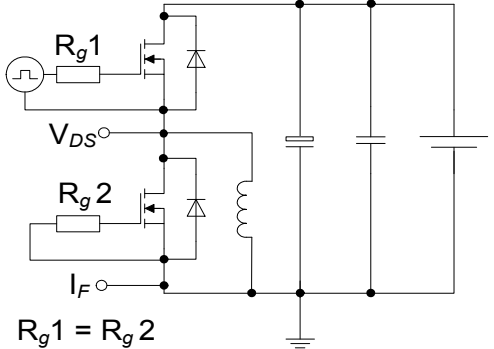
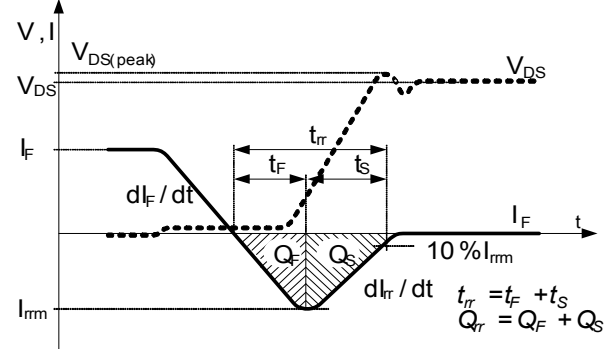
**Diagram 19: Typ. Coss stored energy**



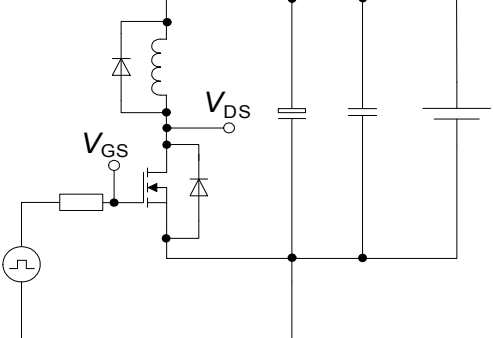
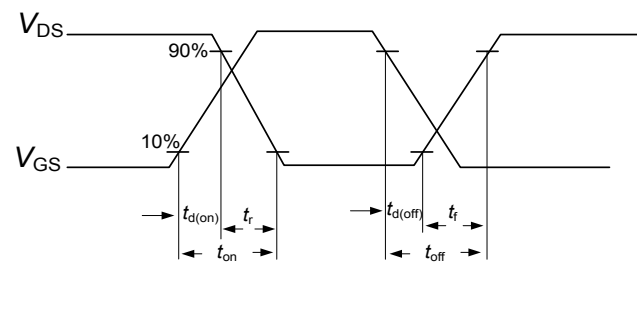
$E_{oss}=f(V_{DS})$

## 5 Test Circuits

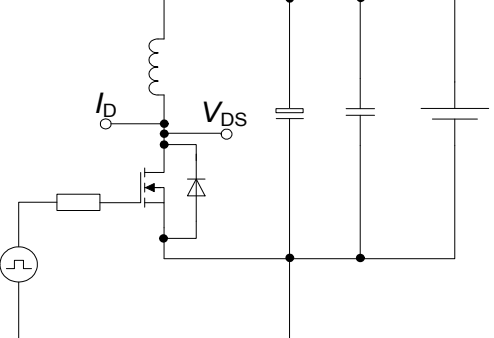
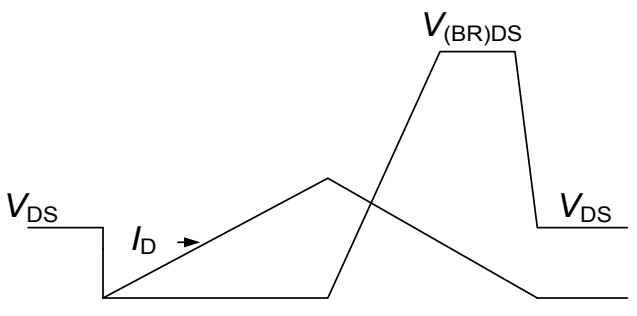
**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
 <p><math>R_{g1} = R_{g2}</math></p>	 <p><math>t_{tr} = t_F + t_S</math>  <math>Q_{tr} = Q_F + Q_S</math></p>

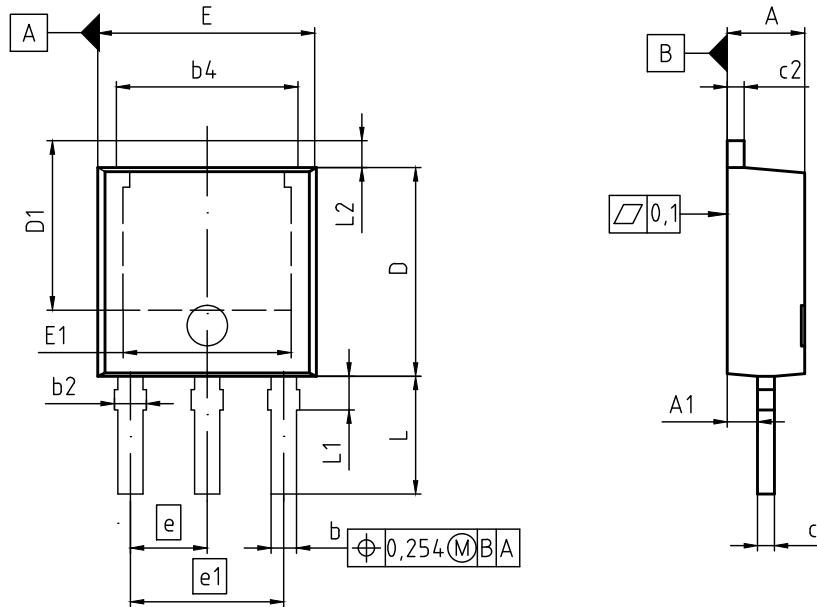
**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform
	

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform
	

## 6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.40	0.086	0.094
A1	0.80	1.14	0.031	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.59	0.018	0.023
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.55	0.198	0.219
E	6.35	6.73	0.250	0.265
E1	4.60	5.21	0.181	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	3.00	3.60	0.118	0.142
L1	0.80	1.25	0.031	0.049
L2	0.88	1.28	0.035	0.050

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Figure 1 Outline PG-TO 251, dimensions in mm/inches

## **7 Appendix A**

### **Table 11 Related Links**

- **IFX CoolMOS™ CE Webpage:** [www.infineon.com](http://www.infineon.com)
- **IFX CoolMOS™ CE application note:** [www.infineon.com](http://www.infineon.com)
- **IFX CoolMOS™ CE simulation model:** [www.infineon.com](http://www.infineon.com)
- **IFX Design tools:** [www.infineon.com](http://www.infineon.com)

# 650V CoolMOS™ CE Power Transistor

## IPS65R650CE

### Revision History

IPS65R650CE

**Revision: 2016-02-25, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-02-25	Release of final version

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