

## MOSFET

### OptiMOS™ 6 Power-Transistor, 120 V

#### Features

- N-channel, normal level
- Very low on-resistance  $R_{DS(on)}$
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low reverse recovery charge ( $Q_{rr}$ )
- High avalanche energy rating
- 175°C operating temperature
- Optimized for high frequency switching
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

#### Product validation

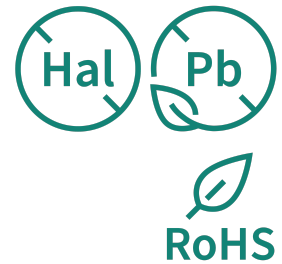
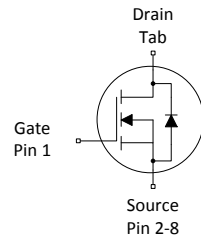
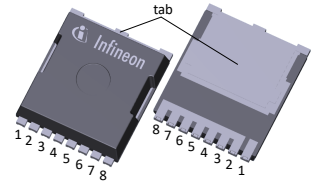
Fully qualified according to JEDEC for Industrial Applications

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	120	V
$R_{DS(on),max}$	2.6	mΩ
$I_D$	224	A
$Q_{oss}$	166	nC
$Q_G$ (0V...10V)	70	nC
$Q_{rr}$ (1000A/μs)	245	nC

Type/Ordering Code	Package	Marking	Related Links
IPT026N12NM6	PG-HSOF-8	026N12N6	-

TOLL





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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	224 158 144 23	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=8\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ °C/W}$ <sup>2)</sup>
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	896	A	$T_C=25\text{ °C}$
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	-	-	115	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	623	mJ	$I_D=62\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	283 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=50\text{ °C/W}$ <sup>2)</sup>
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.53	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$	-	-	50	°C/W	-

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	120	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.6	3.1	3.6	V	$V_{DS}=V_{GS}$ , $I_D=169\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.2 2.5	2.6 3.13	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=115\text{ A}$ $V_{GS}=8\text{ V}$ , $I_D=58\text{ A}$
Gate resistance	$R_G$	0.5	1.0	1.5	$\Omega$	-
Transconductance	$g_{fs}$	85	170	-	S	$ V_{DS} \geq 2 I_D $ , $R_{DS(on)max}$ , $I_D=115\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	5000	6500	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=60\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>6)</sup>	$C_{oss}$	-	1500	2000	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=60\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>6)</sup>	$C_{rss}$	-	27	47	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=60\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	17.1	-	ns	$V_{DD}=60\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=58\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	9.7	-	ns	$V_{DD}=60\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=58\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	28.0	-	ns	$V_{DD}=60\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=58\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	11.7	-	ns	$V_{DD}=60\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=58\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

<sup>6)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics** <sup>7)</sup>

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge <sup>8)</sup>	$Q_{gs}$	-	26	34	nC	$V_{DD}=60\text{ V}$ , $I_D=58\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold <sup>8)</sup>	$Q_{g(th)}$	-	15.5	19.4	nC	$V_{DD}=60\text{ V}$ , $I_D=58\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>8)</sup>	$Q_{gd}$	-	15.4	23	nC	$V_{DD}=60\text{ V}$ , $I_D=58\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	26	-	nC	$V_{DD}=60\text{ V}$ , $I_D=58\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>8)</sup>	$Q_g$	-	70	88	nC	$V_{DD}=60\text{ V}$ , $I_D=58\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.1	-	V	$V_{DD}=60\text{ V}$ , $I_D=58\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>8)</sup>	$Q_{oss}$	-	166	221	nC	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>7)</sup> See "Gate charge waveforms" for parameter definition

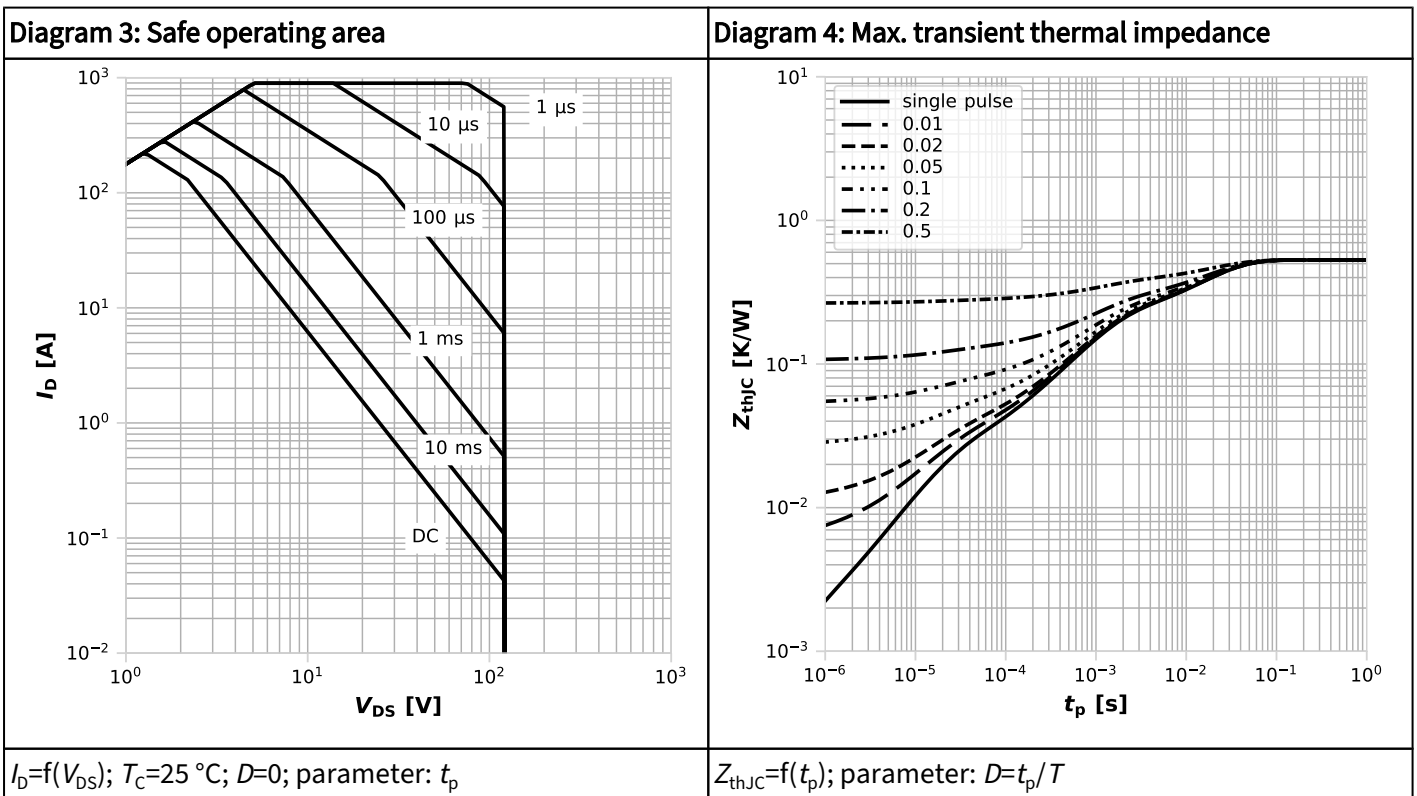
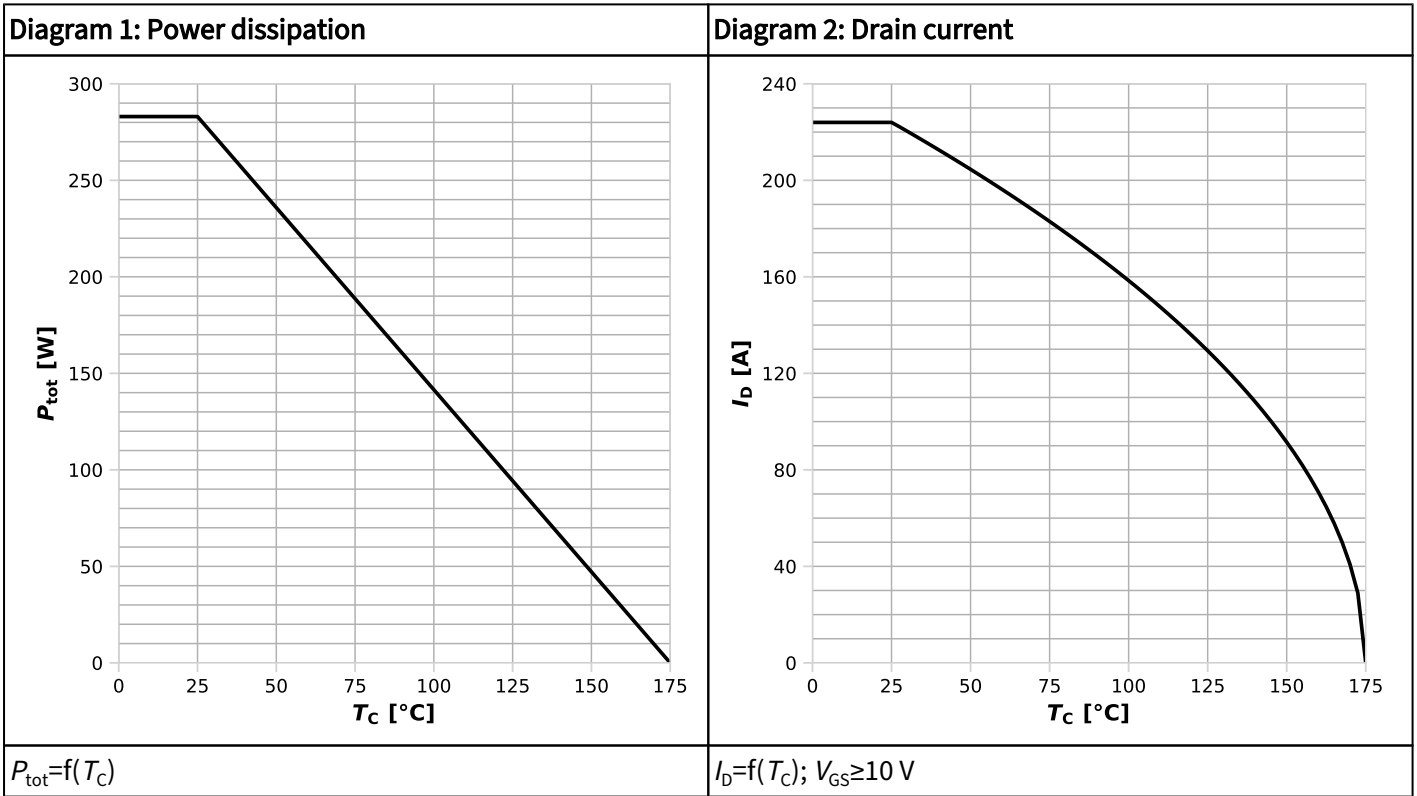
<sup>8)</sup> Defined by design. Not subject to production test.

**Table 7 Reverse diode**

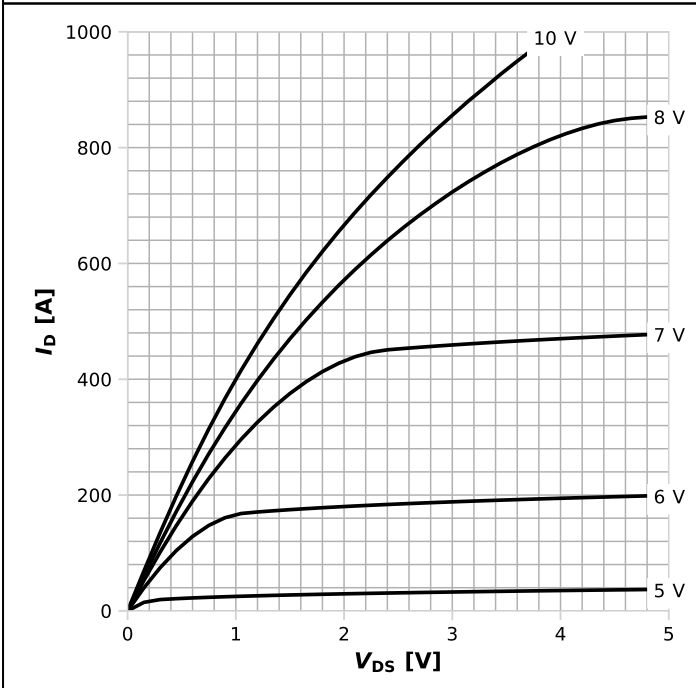
Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	224	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	896	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.87	1.0	V	$V_{GS}=0\text{ V}$ , $I_F=115\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery time <sup>9)</sup>	$t_{rr}$	-	35	70	ns	$V_R=60\text{ V}$ , $I_F=58\text{ A}$ , $di_F/dt=300\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>9)</sup>	$Q_{rr}$	-	85	170	nC	$V_R=60\text{ V}$ , $I_F=58\text{ A}$ , $di_F/dt=300\text{ A}/\mu\text{s}$
Reverse recovery time <sup>9)</sup>	$t_{rr}$	-	30	60	ns	$V_R=60\text{ V}$ , $I_F=58\text{ A}$ , $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>9)</sup>	$Q_{rr}$	-	245	490	nC	$V_R=60\text{ V}$ , $I_F=58\text{ A}$ , $di_F/dt=1000\text{ A}/\mu\text{s}$

<sup>9)</sup> Defined by design. Not subject to production test.

## 4 Electrical characteristics diagrams

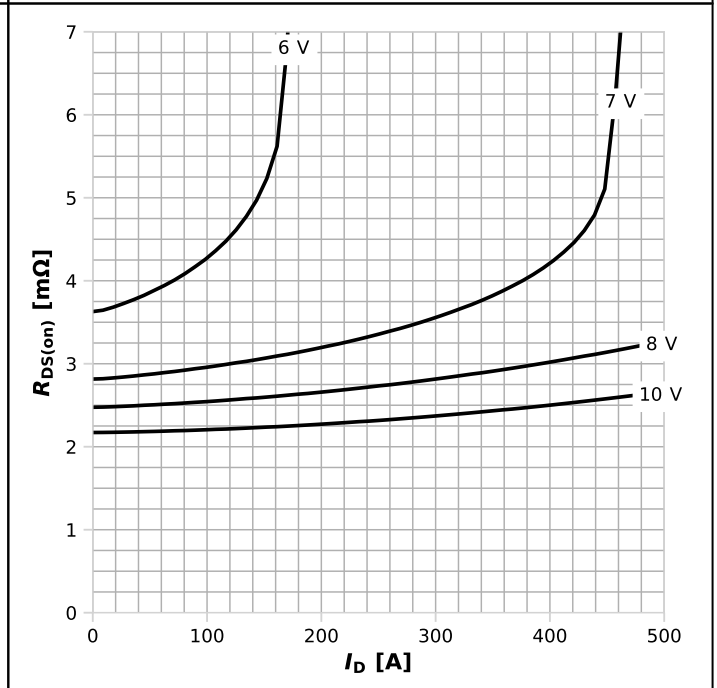


**Diagram 5: Typ. output characteristics**



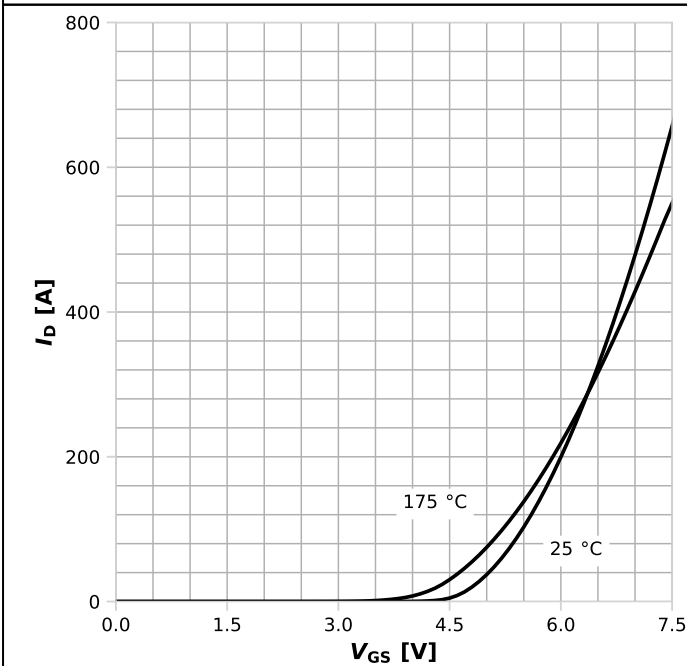
$I_D = f(V_{DS}), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



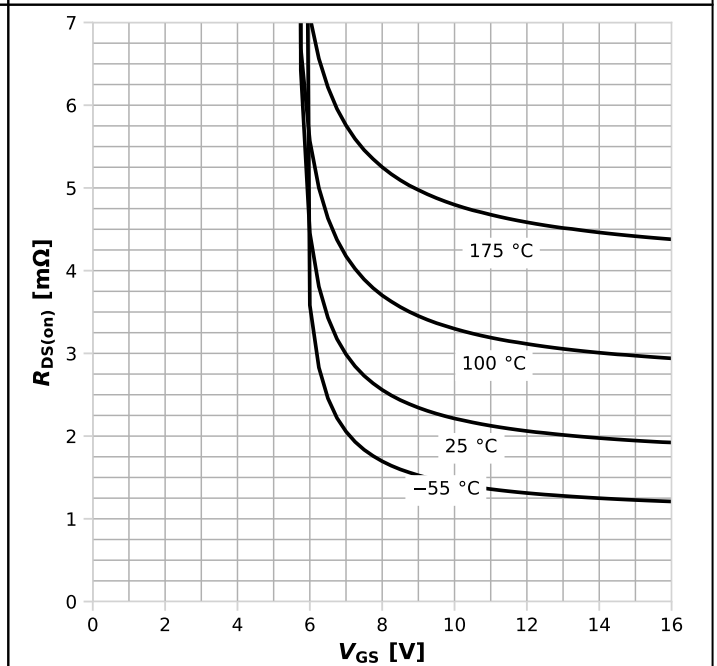
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



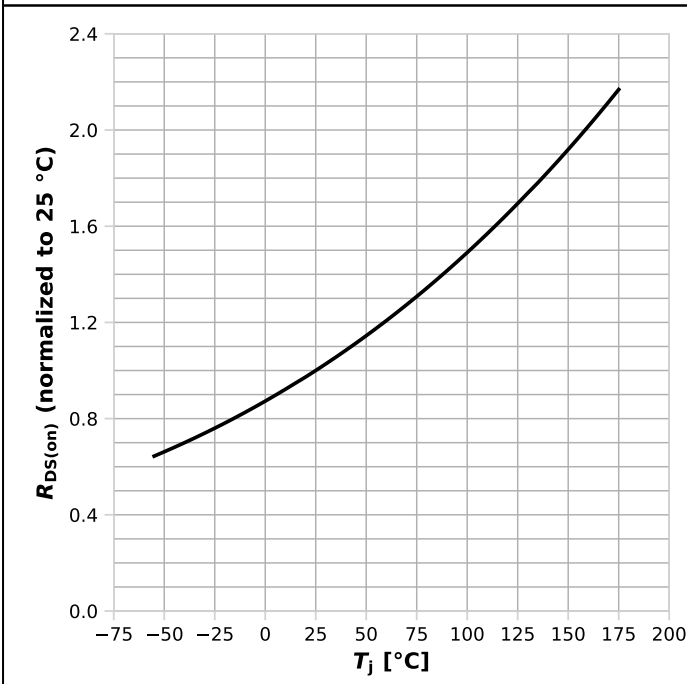
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

**Diagram 8: Typ. drain-source on resistance**



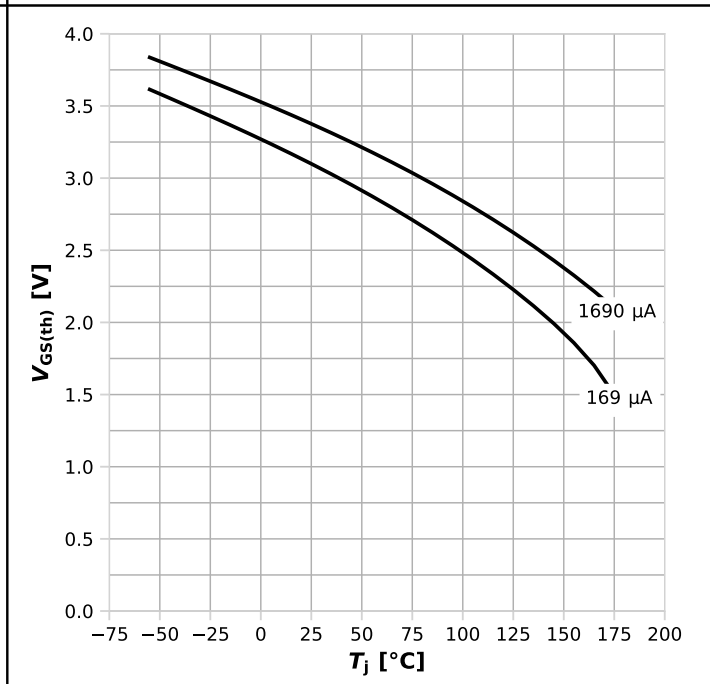
$R_{DS(on)} = f(V_{GS}), I_D = 115\text{ A};$  parameter:  $T_j$

Diagram 9: Normalized drain-source on resistance



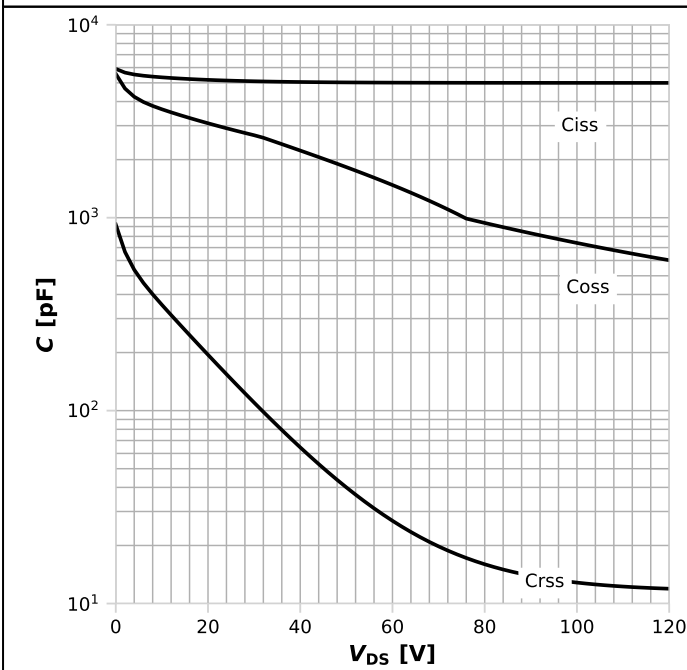
$R_{DS(on)}=f(T_j), I_D=115\text{ A}, V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



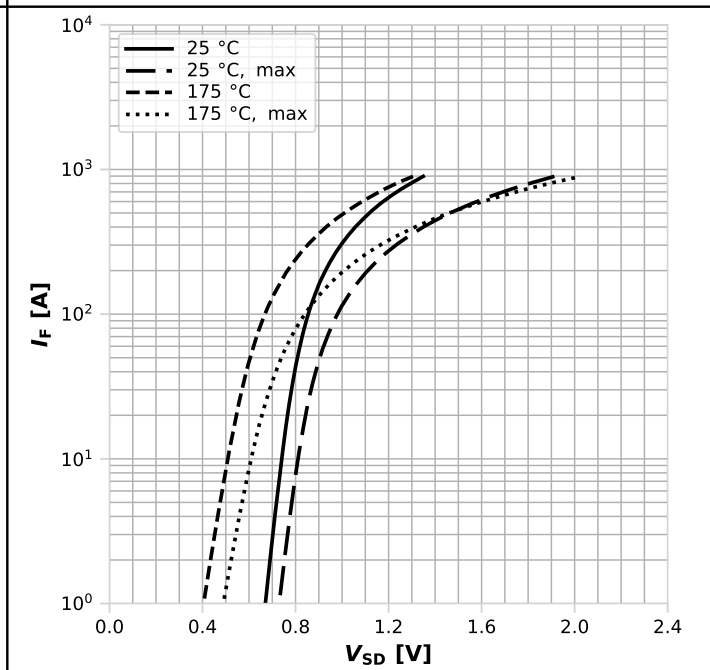
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS}; \text{parameter: } I_D$

Diagram 11: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

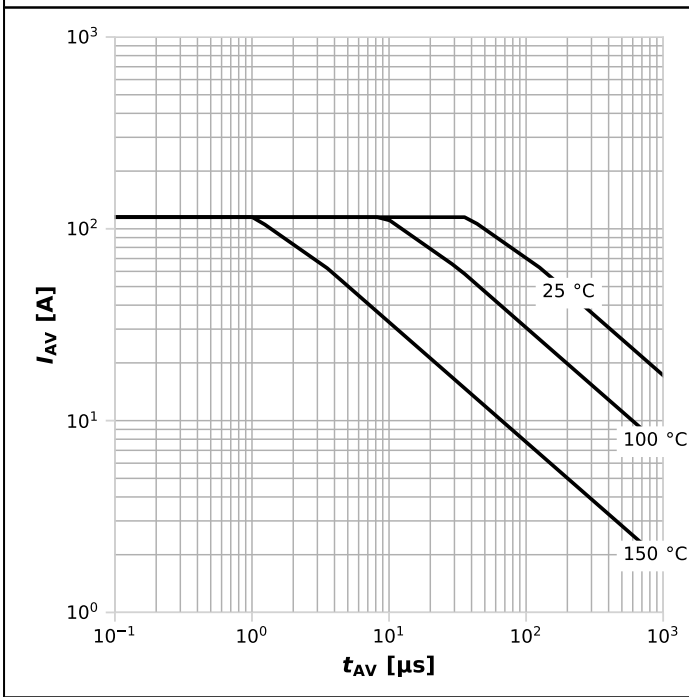
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD}); \text{parameter: } T_j$

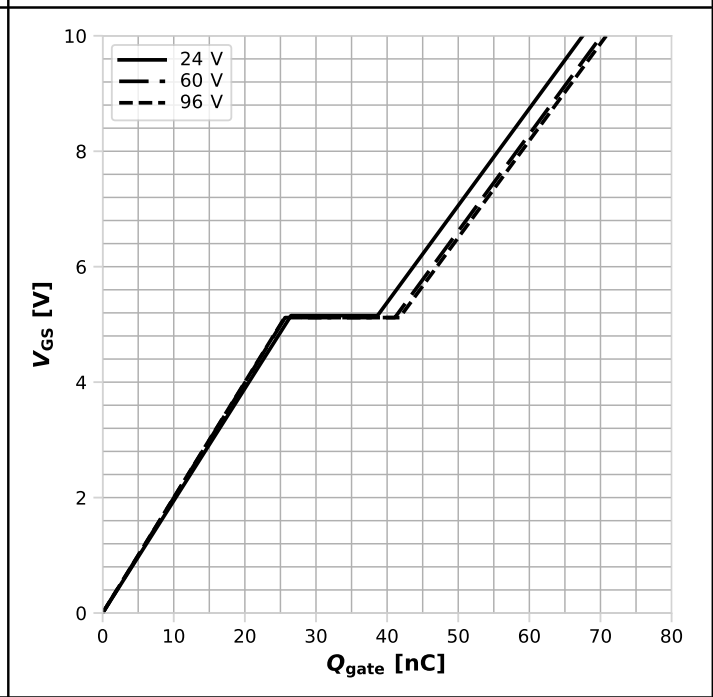


**Diagram 13: Avalanche characteristics**



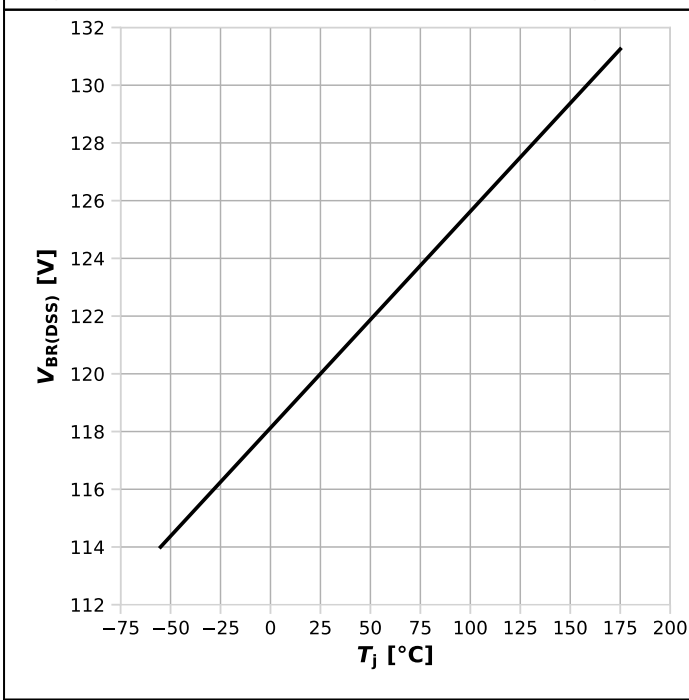
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

**Diagram 14: Typ. gate charge**



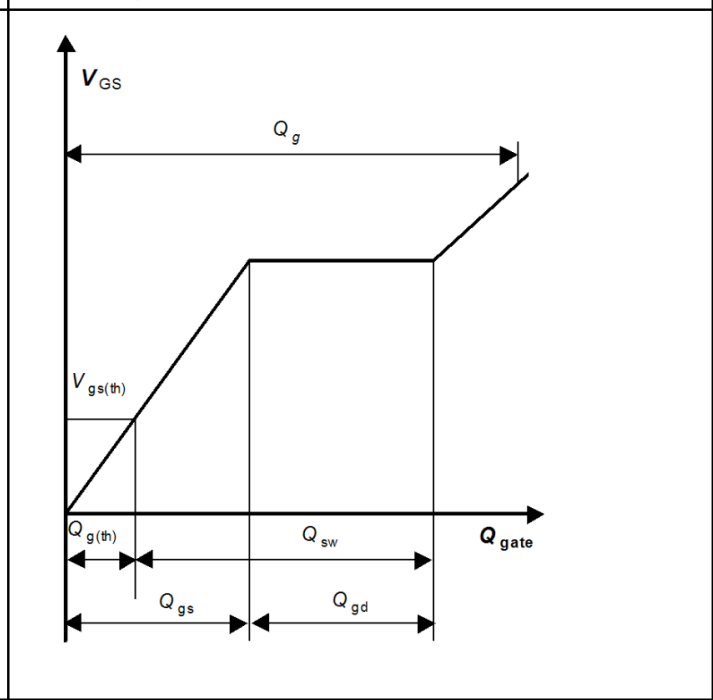
$V_{GS}=f(Q_{gate}), I_D=58 \text{ A pulsed}, T_j=25 \text{ °C}$ ; parameter:  $V_{DD}$

**Diagram 15: Min. drain-source breakdown voltage**



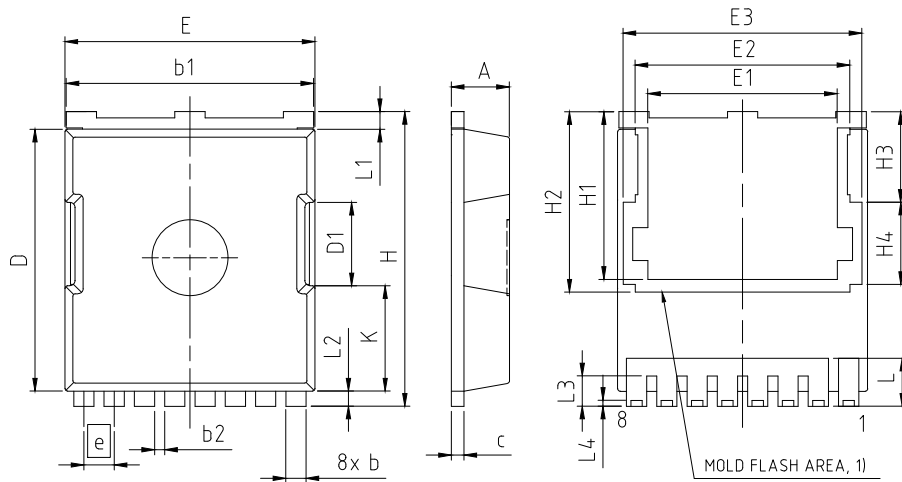
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Gate charge waveforms**



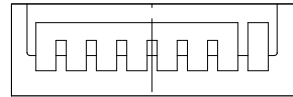
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## 5 Package Outlines



PACKAGE - GROUP NUMBER:		PG-HSOF-8-U01	
DIMENSIONS	MILLIMETERS		
	MIN.	MAX.	
A	2.20	2.40	
b	0.70	0.90	
b1	9.70	9.90	
b2	0.42	0.50	
c	0.40	0.60	
D	10.28	10.58	
D1	3.30		
E	9.70	10.10	
E1	7.50		
E2	8.50		
E3	9.46		
e	1.20 (BSC)		
H	11.48	11.88	
H1	6.55	6.95	
H2	7.15		
H3	3.59		
H4	3.26		
N	8		
K	4.18		
L	1.60	2.10	
L1	0.50	0.90	
L2	0.50	0.70	
L3	1.00	1.30	
L4	0.13	0.33	

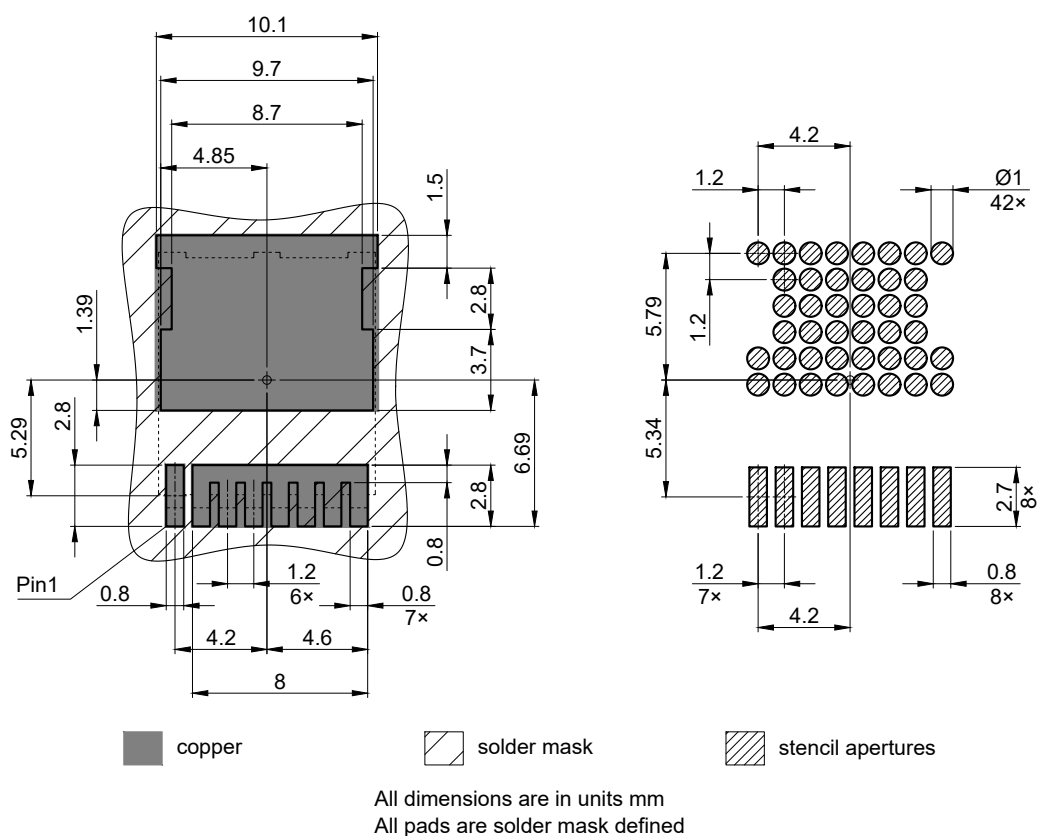
5:1



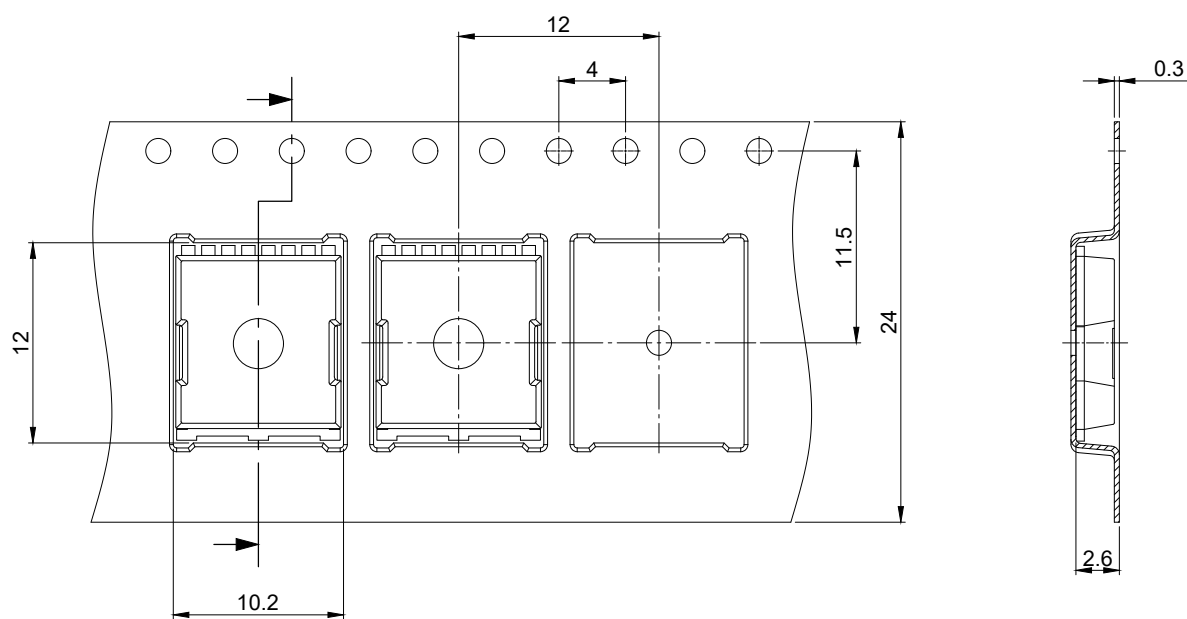
OPTIONAL LEAD FORM:  
WITHOUT LTI OPTION


1) PARTIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm



**Figure 2** Outline PG-HSOF-8, dimensions in mm



All dimensions are in units mm  
The drawing is in compliance with ISO 128-30, Projection Method 1 [  ]

**Figure 3** Outline PG-HSOF-8, dimensions in mm

## Revision History

IPT026N12NM6

### Revision 2024-07-29, Rev. 1.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-07-29	Release of final datasheet

#### Trademarks

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