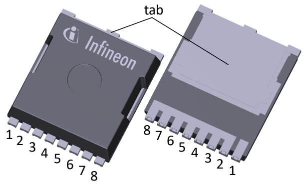
MOSFET

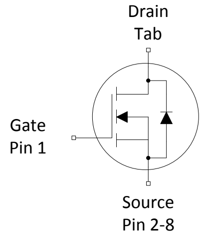
OptiMOS™ 5 Power-Transistor, 150 V

TOLL



Features

- N-channel
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	3.9	mΩ
I_D	190	A
Q_{oss}	219	nC
Q_G	78	nC

Type/Ordering Code	Package	Marking	Related Links
IPT039N15N5	PG-HSOF-8	039N15N5	-

Table of Contents

1 Maximum ratings

unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	190 134 128 21	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=8 V, T_C=100 °C V_{GS}=10V, T_A=25°C, R_{thJA}=40°C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	760	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	255	mJ	I_D=100 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	319 3.8	W	T_C=25 °C T_A=25 °C, R_{thJA}=40 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

1) Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

2) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3) See Diagram 3 for more detailed information

4) See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.47	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5]	R_{thJA}	-	-	40	°C/W	-

5) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	3.0	3.8	4.6	V	V_{DS}=V_{GS}, I_D=257 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1.0 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	3.3 3.6	3.9 4.3	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=8 V, I_D=25 A
Gate resistance [6)]	R_G	-	1.1	1.6	Ω	-
Transconductance	g_{fs}	-	110	-	S	$\lvert V_{DS}\rvert \geq 2\lvert I_D\rvert R_{DS(on)max}$, I_D=50 A

6) Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance [7)]	C_{iss}	-	5900	7700	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Output capacitance [7)]	C_{oss}	-	1500	1930	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Reverse transfer capacitance [7)]	C_{rss}	-	33	58	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	18.7	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	4.5	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	23.5	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	5.4	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω

7) Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	31	-	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	22	-	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate to drain charge [9)]	Q_{gd}	-	15.5	23	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	24	-	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total [9)]	Q_g	-	78	98	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Output charge [9)]	Q_{oss}	-	219	291	nC	V_{DS}=75 V, V_{GS}=0 V

8) See "Gate charge waveforms" for parameter definition

9) Defined by design. Not subject to production test.

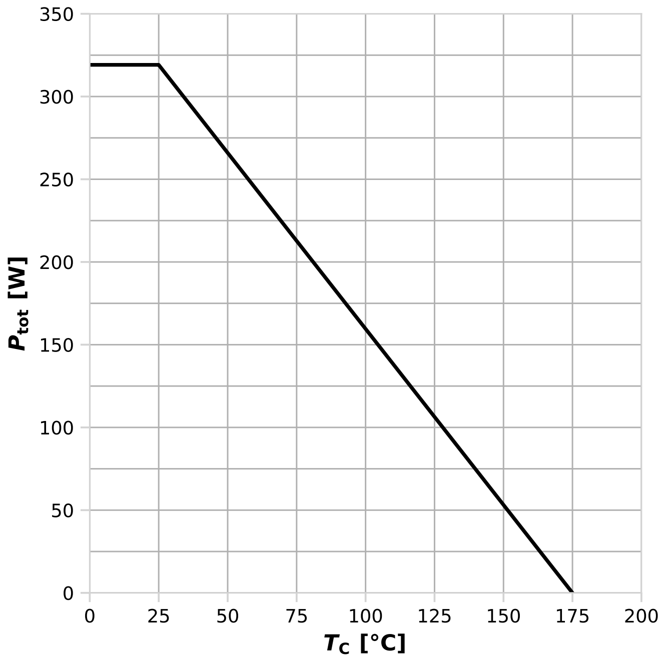
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	190	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	760	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.81	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [10)]	t_{rr}	-	53.4	106.8	ns	V_R=75 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge [10)]	Q_{rr}	-	77.2	154.4	nC	V_R=75 V, I_F=50 A, di_F/dt=100 A/µs

10) Defined by design. Not subject to production test.

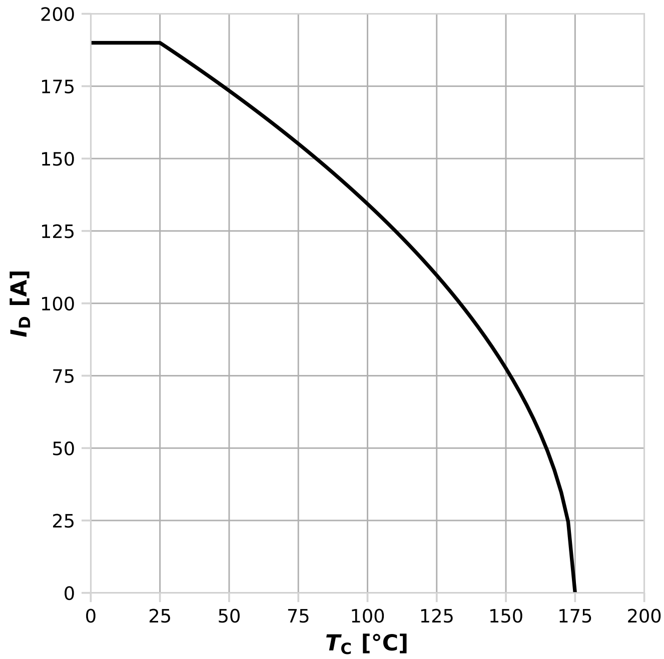
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



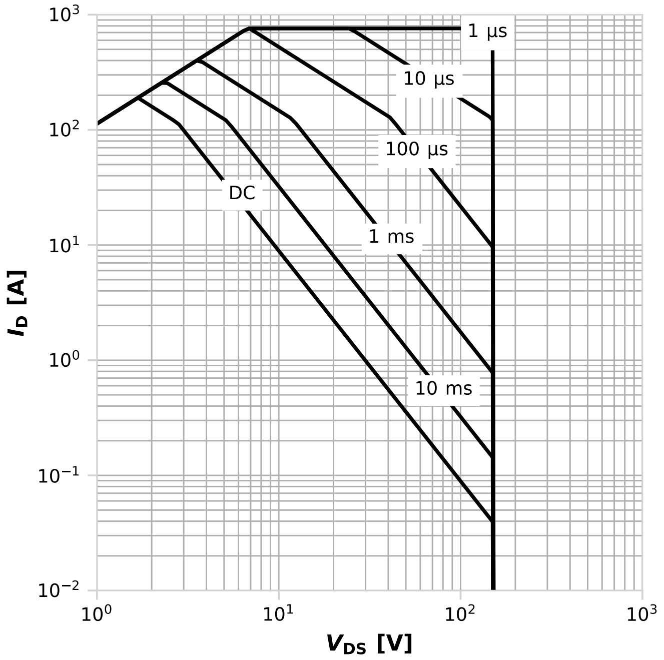
P_{tot}=f(T_C)

Diagram 2: Drain current



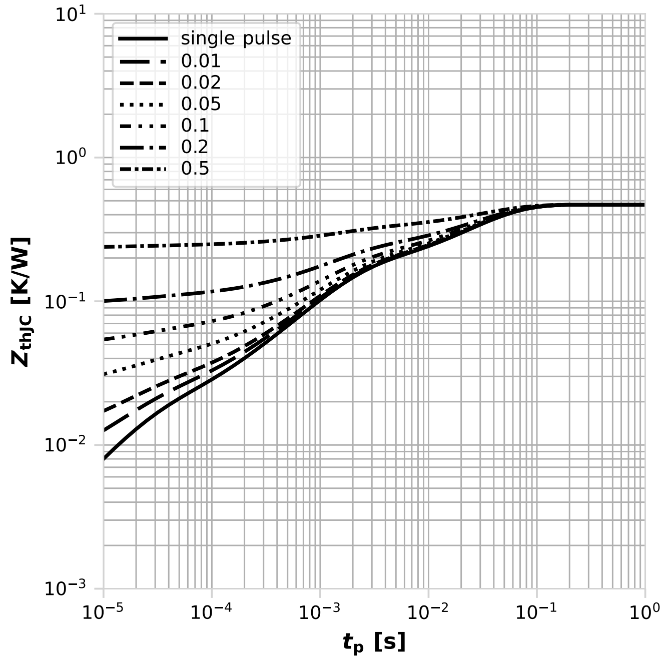
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



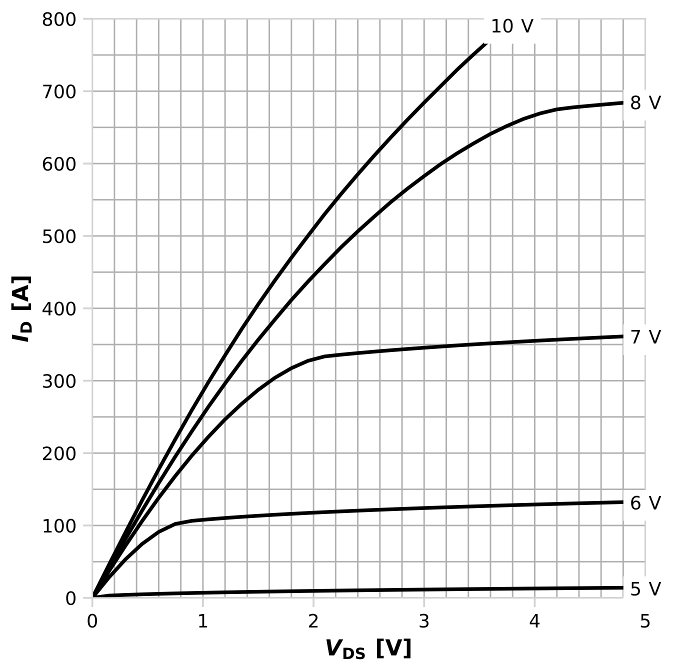
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



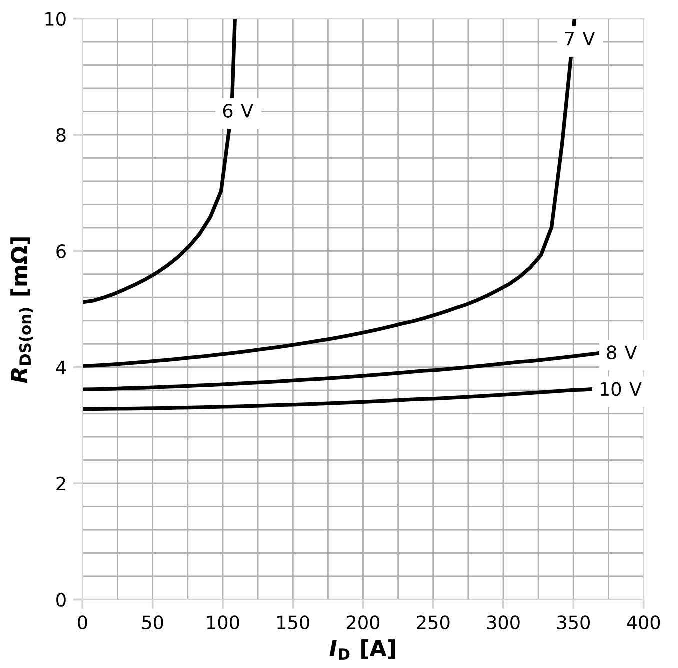
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



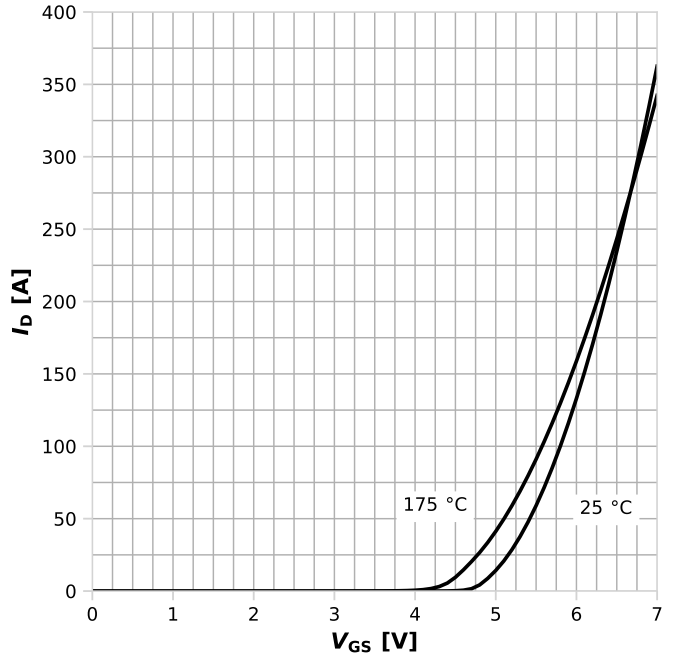
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



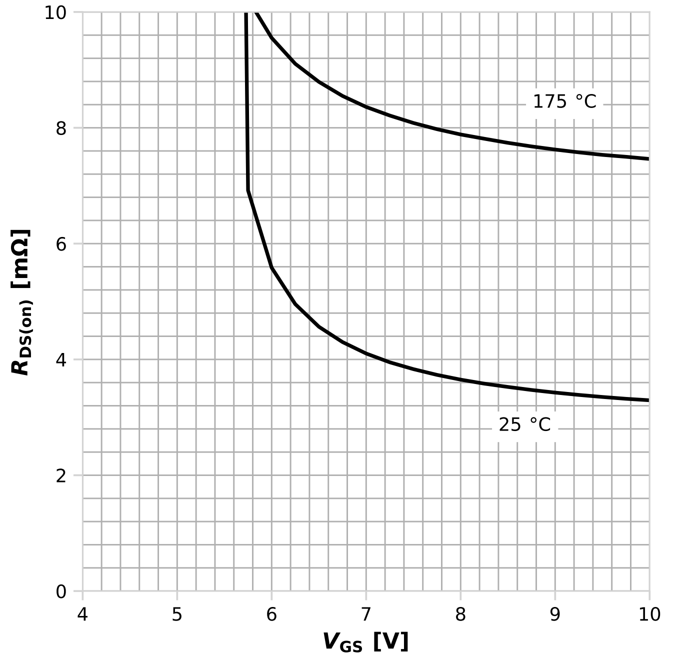
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



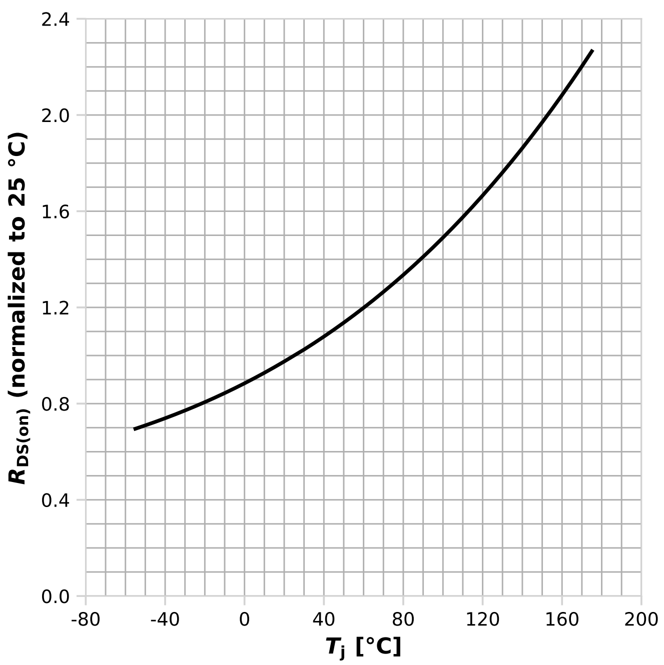
I_D=f(V_{GS}), $|V_{DS}|$>2$|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



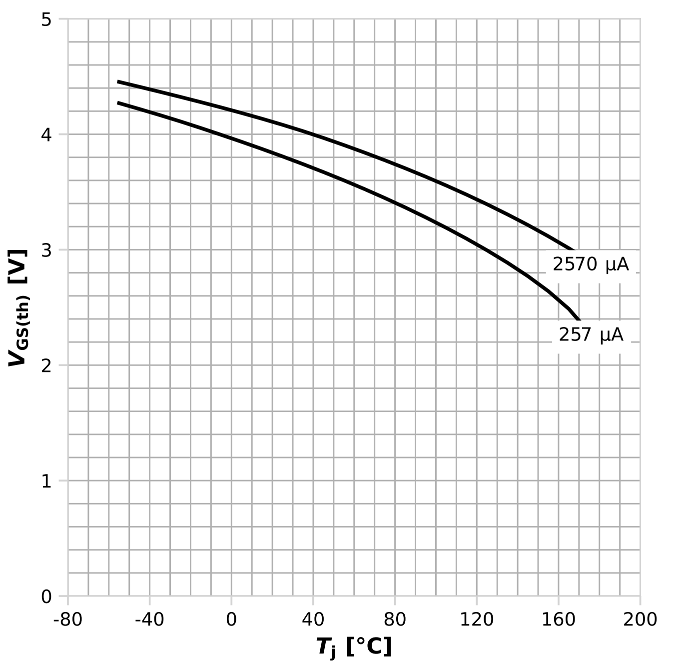
$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



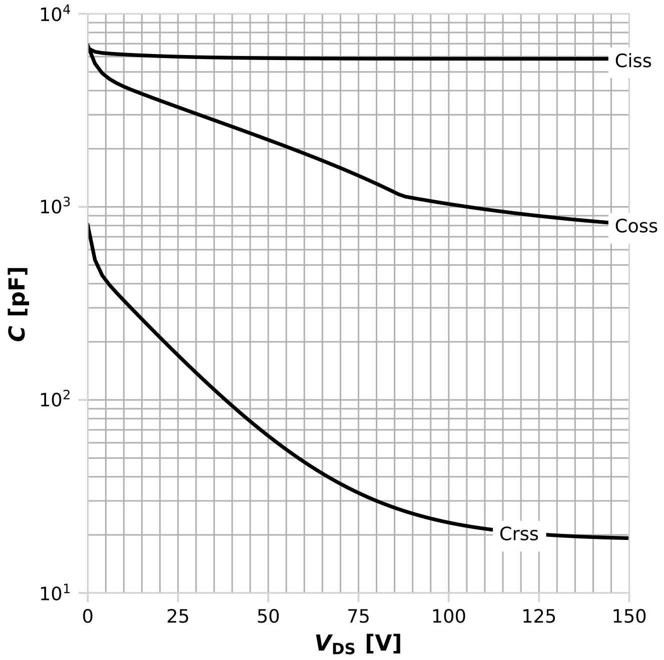
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



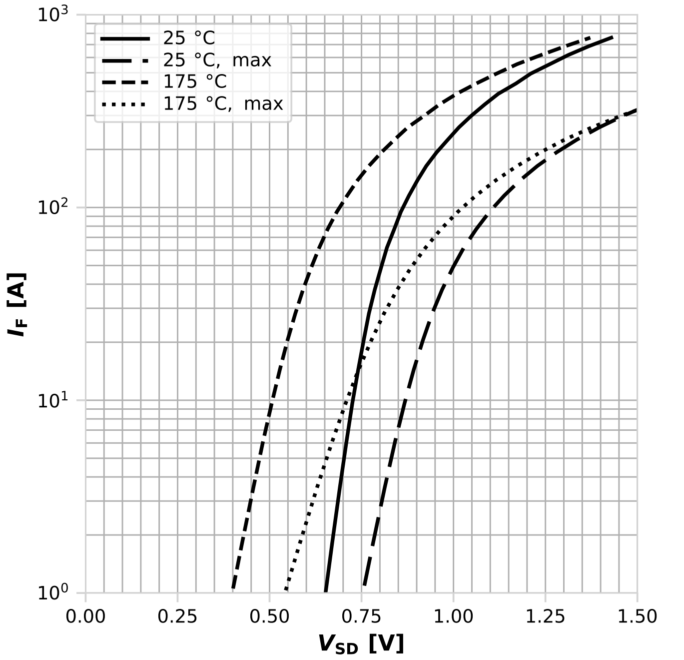
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

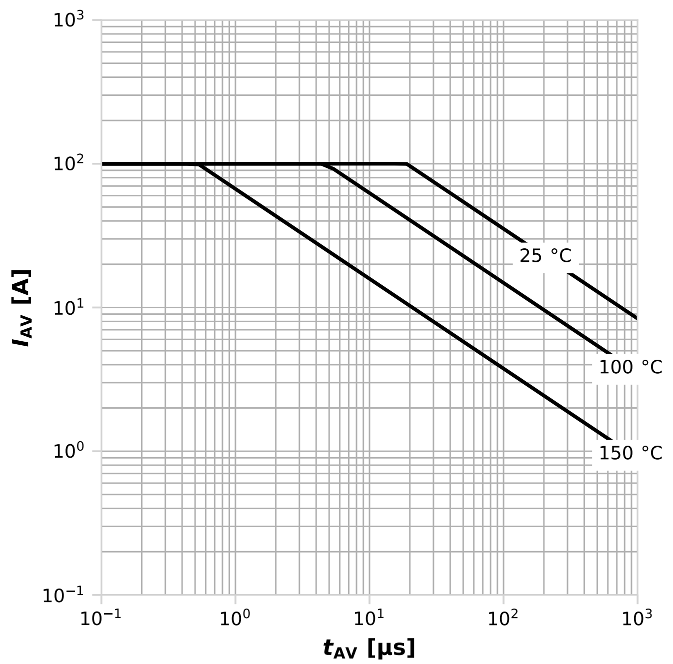
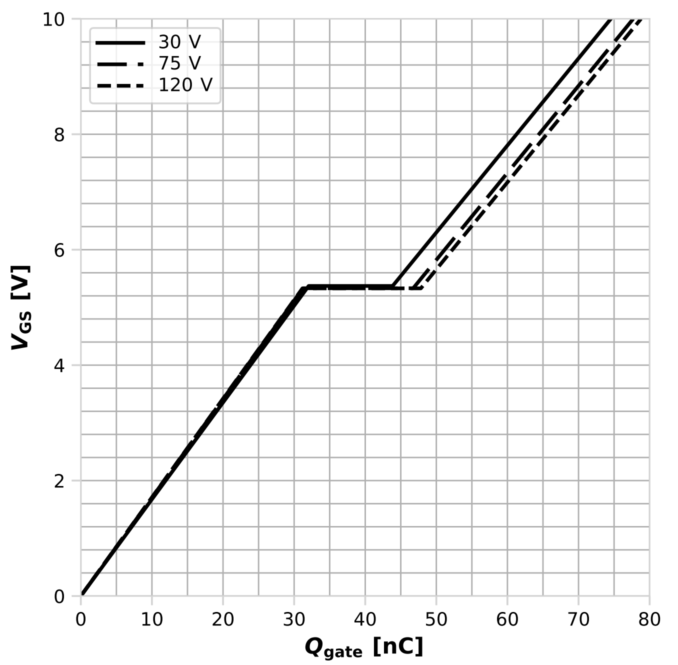
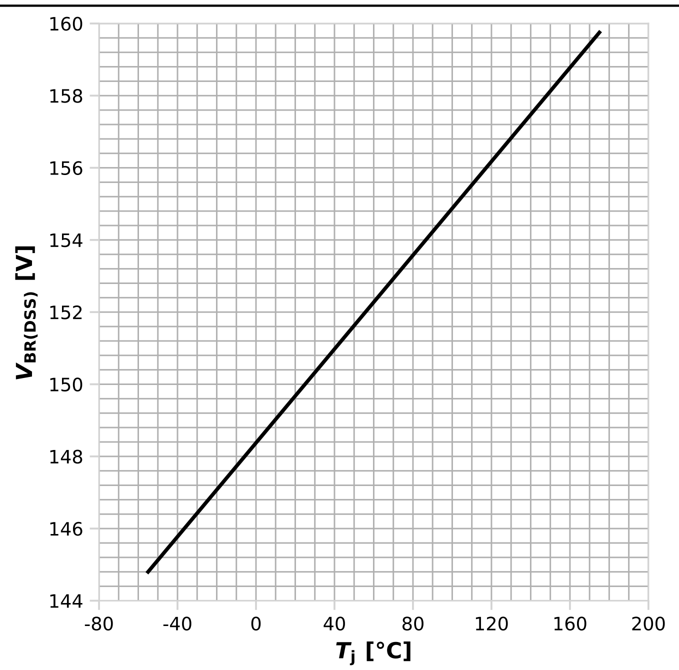
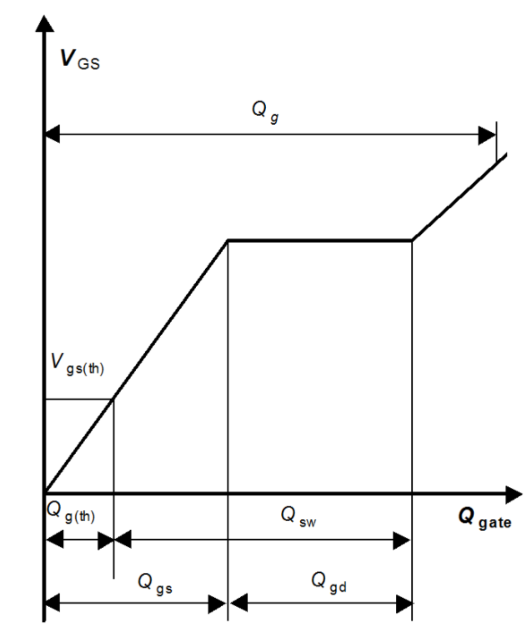
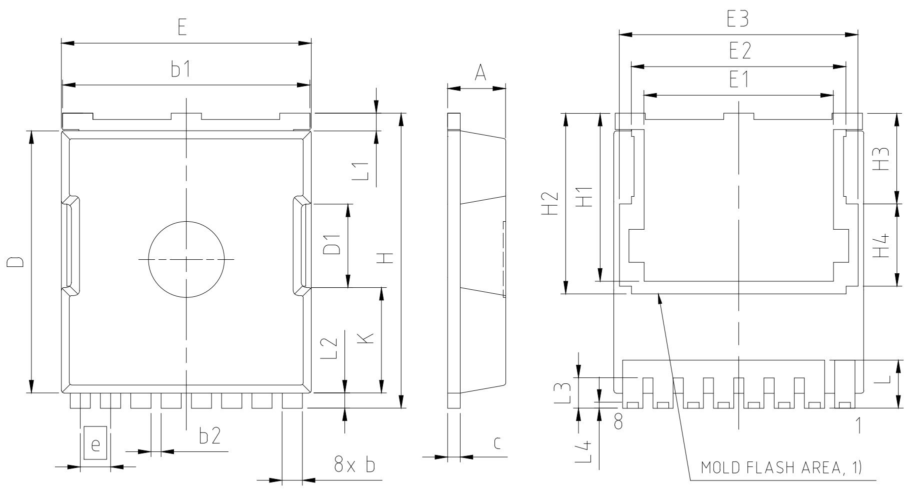
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

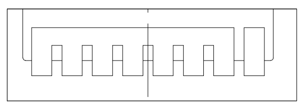
Diagram 15: Drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-HSOF-8-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	
H3	3.59	
H4	3.26	
N	8	
K	4.18	
L	1.60	2.10
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	0.13	0.33

5:1



OPTIONAL LEAD FORM:
WITHOUT LTI OPTION

1) PATIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

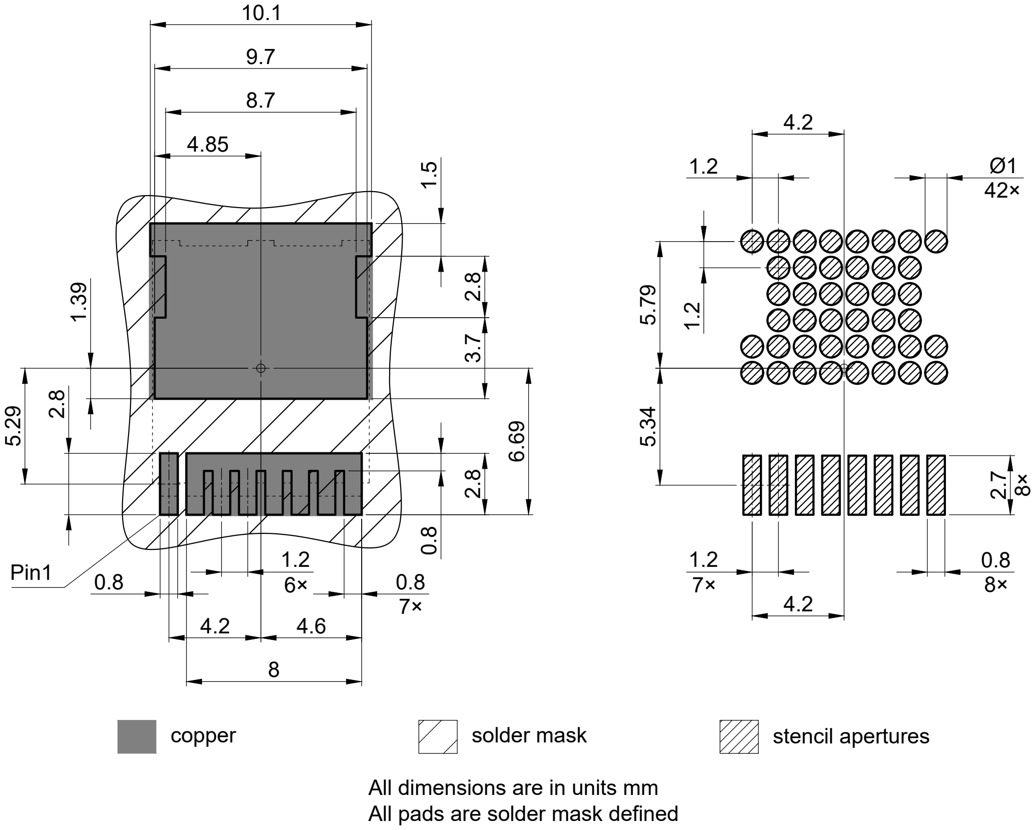
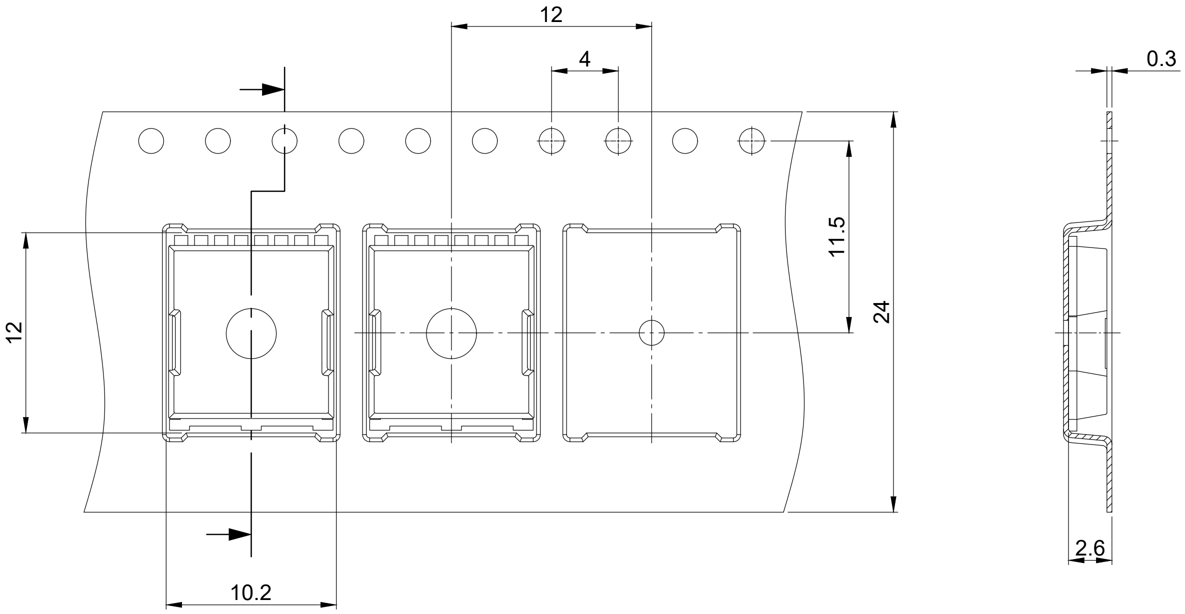


Figure 2 Outline PG-HSOF-8, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 3 Outline PG-HSOF-8, dimensions in mm

Revision History

IPT039N15N5

Revision 2024-06-11, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-09-10	Release of final version
2.1	2023-03-08	Update Coss max
2.2	2024-06-11	Update Rg

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