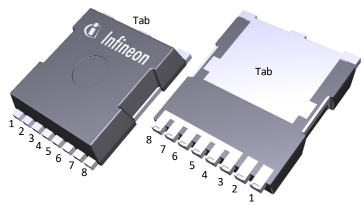
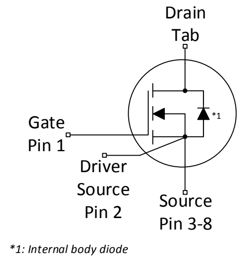
MOSFET

600V CoolMOS™ CFD7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series and is an optimized platform tailored to target soft switching applications such as phase-shift full-bridge (ZVS) and LLC. Resulting from reduced gate charge (Q_g), best-in-class reverse recovery charge (Q_{rr}) and improved turn off behavior CoolMOS™ CFD7 offers highest efficiency in resonant topologies. As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness, without sacrificing easy implementation in the design-in process.

TOLL





Features

- Ultra-fast body diode
- Low gate charge
- Best-in-class reverse recovery charge (Q_{rr})
- Improved MOSFET reverse diode dv/dt and di_F/dt ruggedness
- Lowest FOM $R_{DS(on)}$*Q_g and $R_{DS(on)}$*E_{oss}
- Best-in-class $R_{DS(on)}$ in SMD and THD packages

Benefits

- Excellent hard commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use / performance tradeoff
- Enabling increased power density solutions

Potential applications

Suitable for Soft Switching topologies
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction. For paralleling 4pin MOSFET devices the placement of the gate resistor is generally recommended to be on the Driver Source instead of the Gate.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	125	mΩ
$Q_{g,typ}$	31	nC
$I_{D,pulse}$	58	A
E_{oss} @ 400V	3.6	µJ
Body diode di_F/dt	1300	A/µs

Part number	Package	Marking	Related links
IPT60R125CFD7	PG-HSOF-8	60R125F7	see Appendix A

Table of contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values Min.	Values Typ.	Values Max.	Unit	Note / Test condition
Continuous drain current [1]	I_D	-	-	21	A	T_C=25°C
				13		T_C=100°C
Pulsed drain current [2]	$I_{D,pulse}$	-	-	58	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	68	mJ	I_D=4.1A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}			0.34		
Avalanche current, single pulse	I_{AS}	-	-	4.1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	126	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55		150	°C	
Mounting torque	-	-		n.a.	Ncm	
Continuous diode forward current [1]	I_S	-	-	21	A	T_C=25°C
Diode pulse current [2]	$I_{S,pulse}$			58		
Reverse diode dv/dt [3]	dv/dt	-	-	70	V/ns	V_{DS}=0...400V, I_{SD}≤16A, T_j=25°C see table 8
Maximum diode commutation speed	di_F/dt			1300	A/µs	
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$.
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.99	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values Min.	Values Typ.	Values Max.	Unit	Note / Test condition
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	V_{DS}=V_{GS}, I_D=0.34mA
Zero gate voltage drain current	I_{DSS}	-	-	1	µA	V_{DS}=600V, V_{GS}=0V, T_j=25°C
Zero gate voltage drain current [4]	I_{DSS}	-	7	37	µA	V_{DS}=600V, V_{GS}=0V, T_j=125°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.101	0.125	Ω	V_{GS}=10V, I_D=6.8A, T_j=25°C
			0.229	-		V_{GS}=10V, I_D=6.8A, T_j=150°C
Gate resistance	R_G	-	10	-	Ω	f=1MHz, open drain

[4] Maximum specification is defined by calculated six sigma upper confidence bound

Table 5 Dynamic characteristics

Parameter	Symbol	Values Min.	Values Typ.	Values Max.	Unit	Note / Test condition
Input capacitance	C_{iss}	-	1329	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}		24			
Effective output capacitance, energy related [5]	$C_{o(er)}$	-	44	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related [6]	$C_{o(tr)}$	-	451	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	24	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=8.1A, R_G=5.3Ω; see table 9
Rise time	t_r		13			
Turn-off delay time	$t_{d(off)}$		85			
Fall time	t_f		5			

[5] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

[6] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8	-	nC	V_{DD}=400V, I_D=8.1A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}		11		nC	
Gate charge total	Q_g		31		nC	
Gate plateau voltage	$V_{plateau}$		5.7		V	

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	V_{GS}=0V, I_F=6.8A, T_j=25°C
Reverse recovery time	t_{rr}	-	95	142	ns	V_R=400V, I_F=8.1A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}		0.38	0.76	µC	
Peak reverse recovery current	I_{rrm}		7.2	-	A	

4 Electrical characteristics diagrams

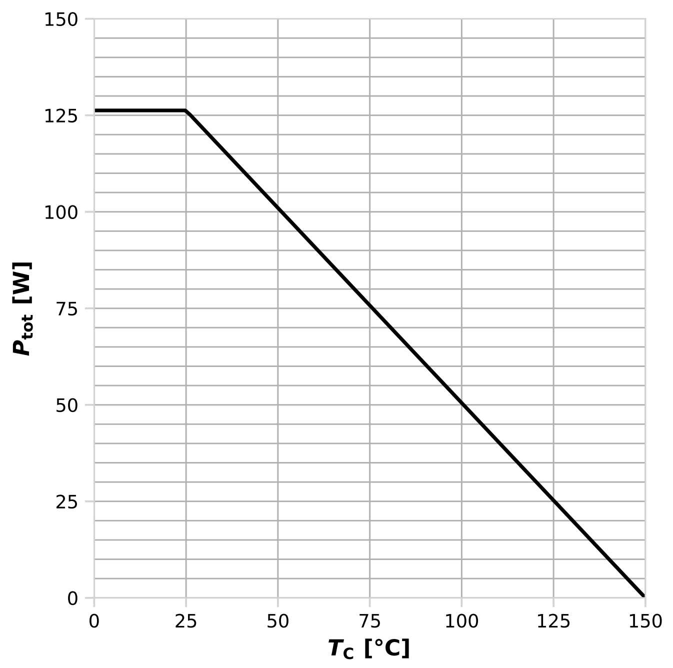
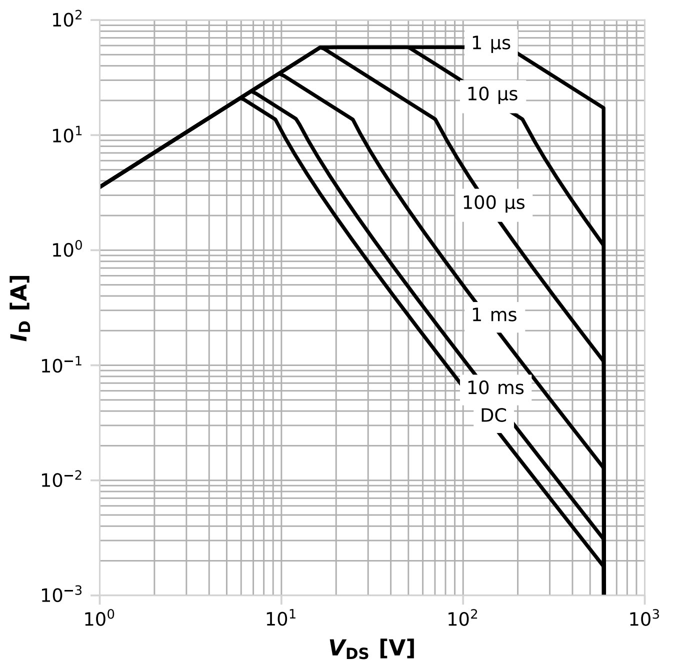
Diagram 1: Power dissipation	Diagram 2: Safe operating area
	
P_{tot}=f(T_C)	I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

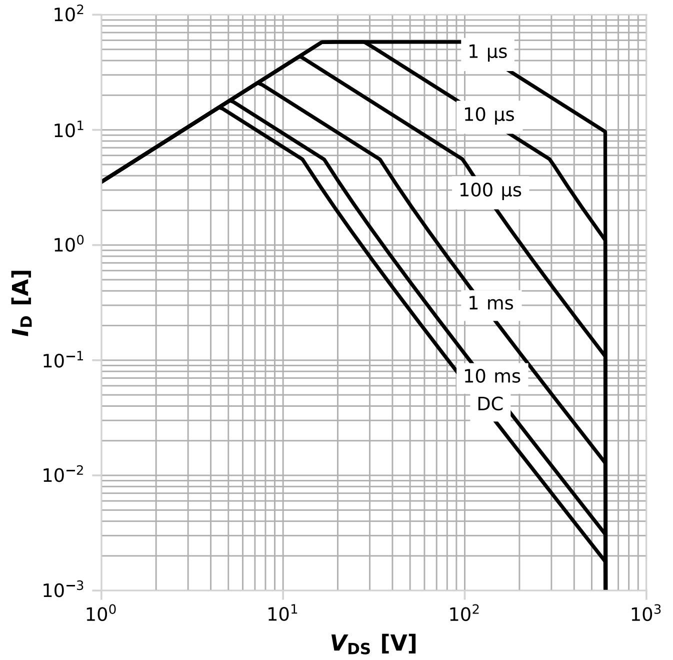
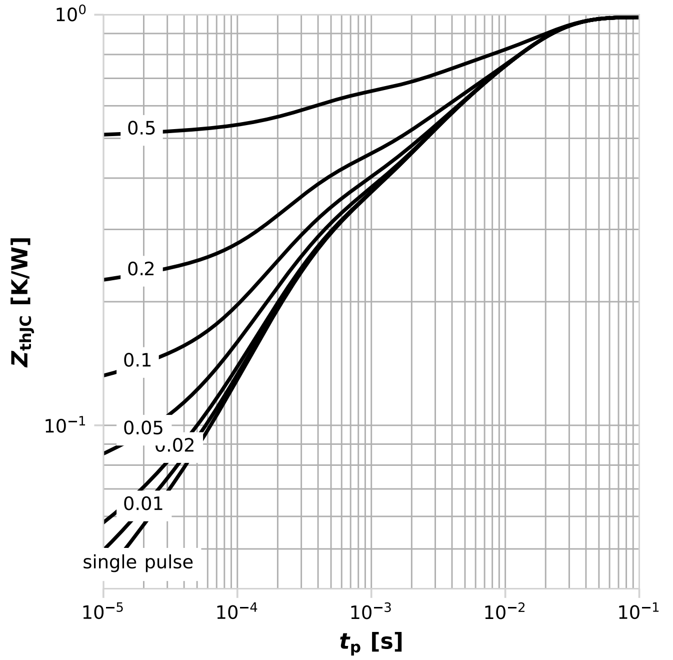
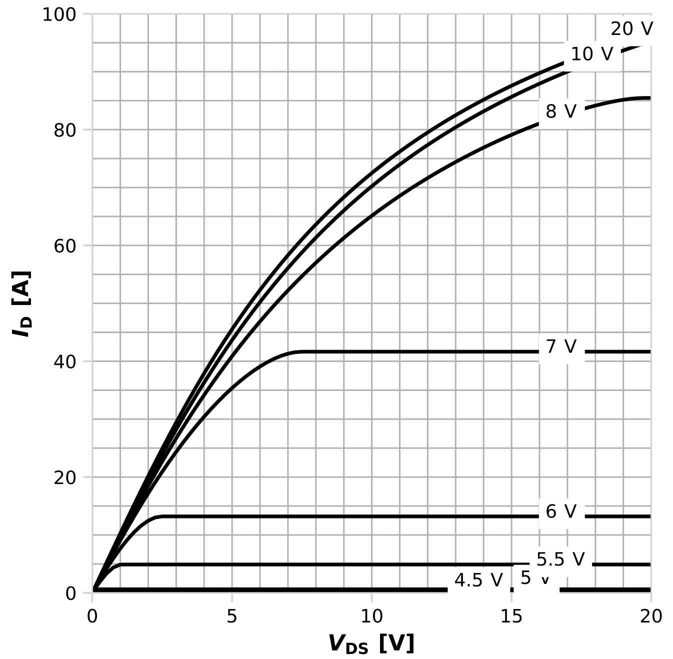
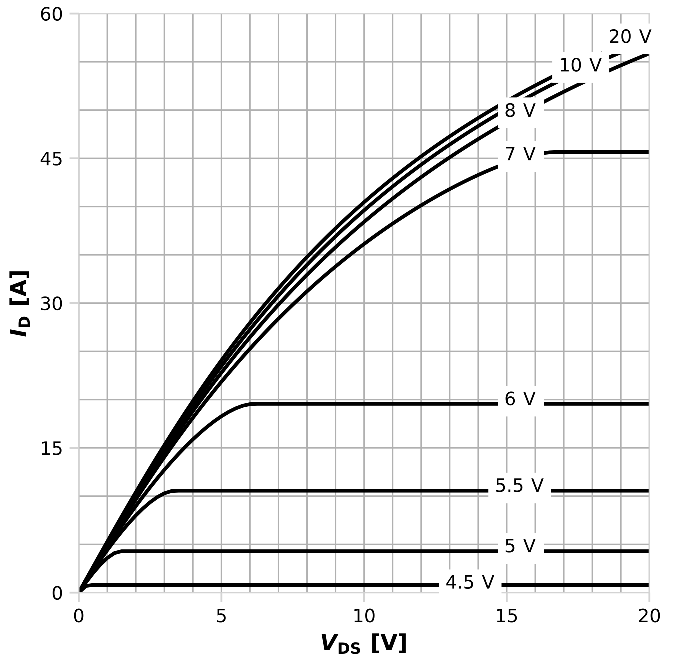
Diagram 3: Safe operating area	Diagram 4: Max. transient thermal impedance
	
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p	Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



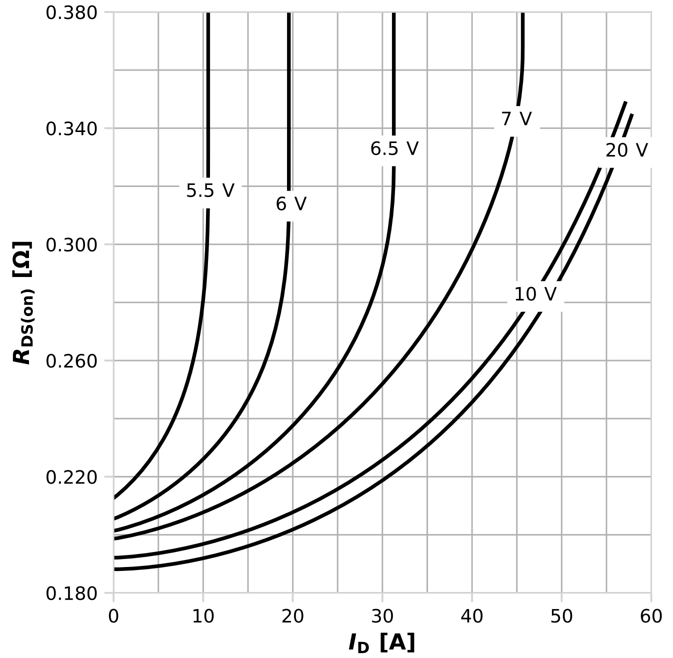
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



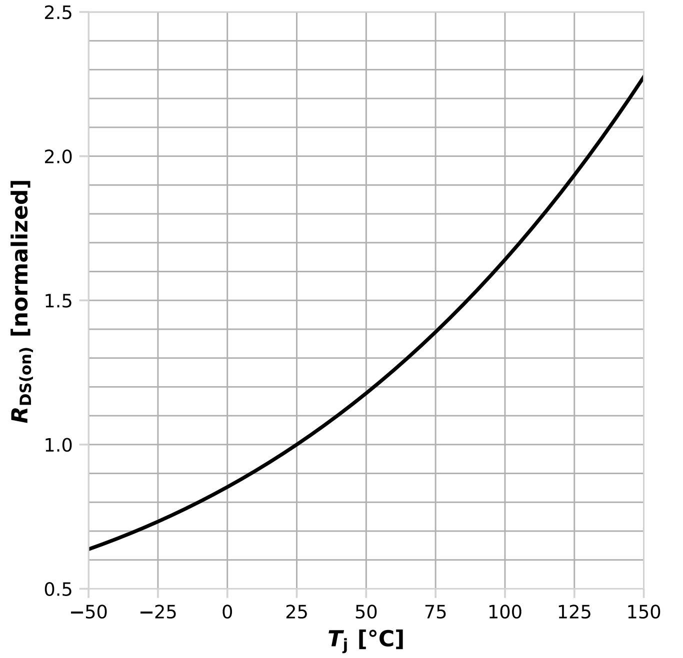
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



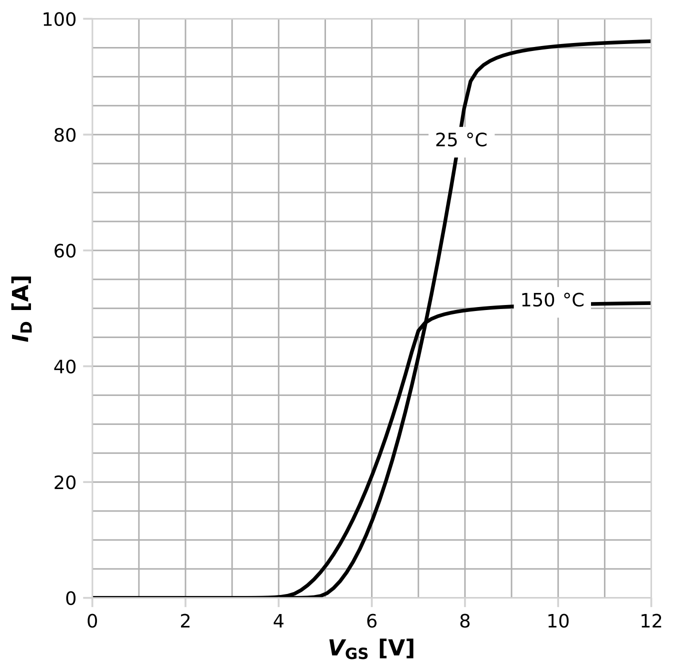
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



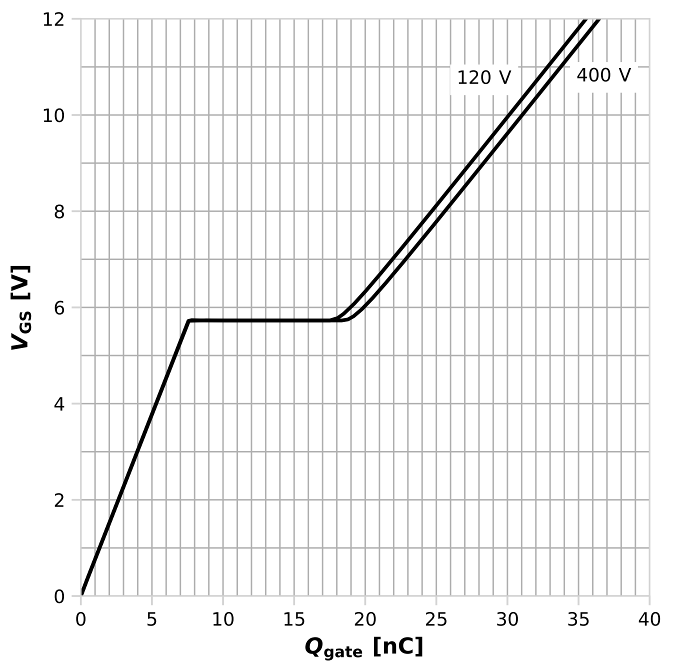
$R_{DS(on)}$=f(T_j); I_D=6.8 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



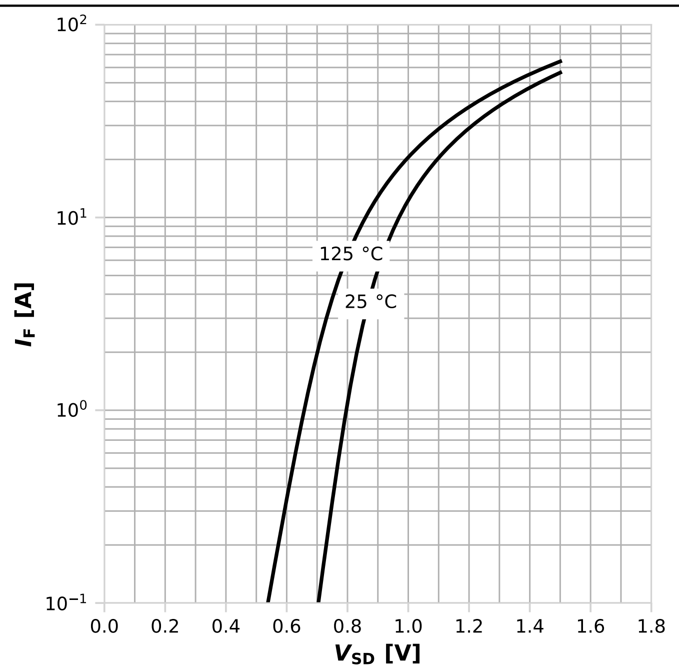
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



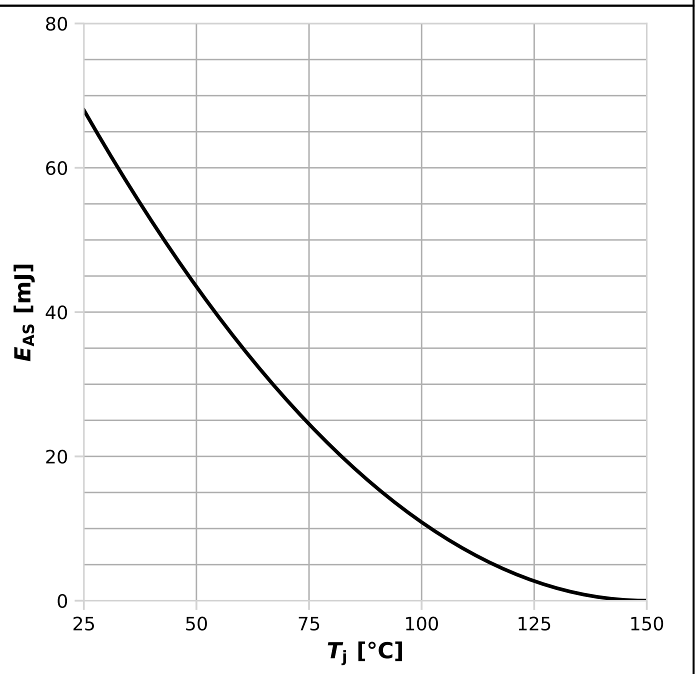
V_{GS}=f(Q_{gate}); I_D=8.1 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



E_{AS}=f(T_j); I_D=4.1 A; V_{DD}=50 V

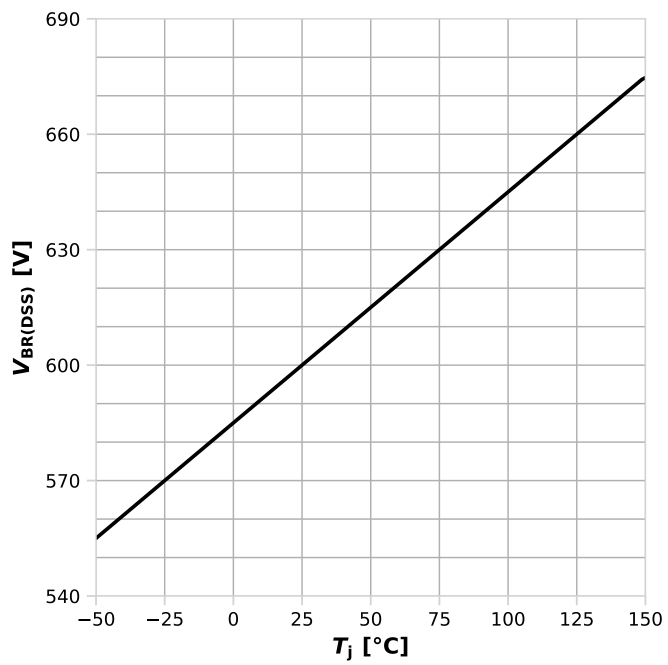
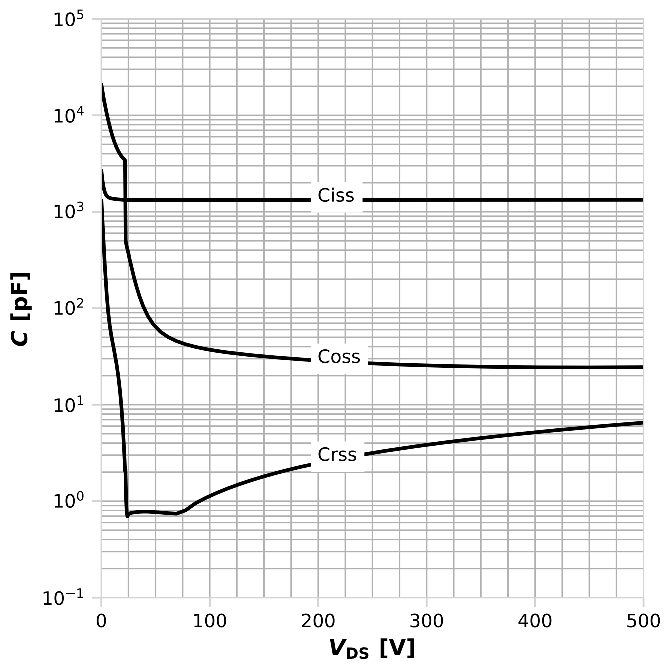
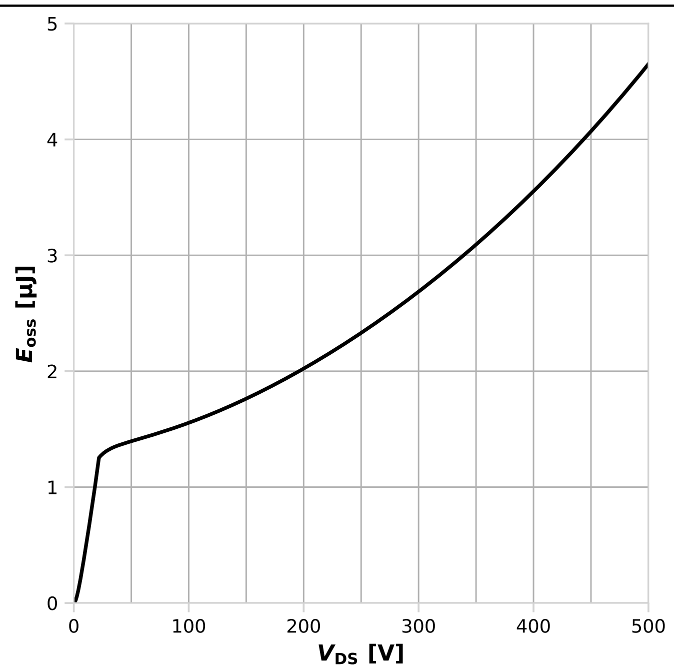
Diagram 13: Drain-source breakdown voltage	Diagram 14: Typ. capacitances
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy

E_{oss}=f(V_{DS})

5 Test circuits

Table 8 Diode characteristics

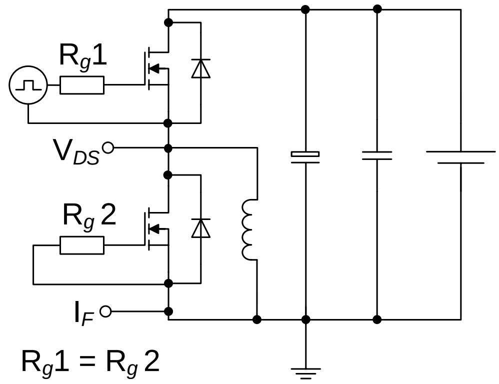
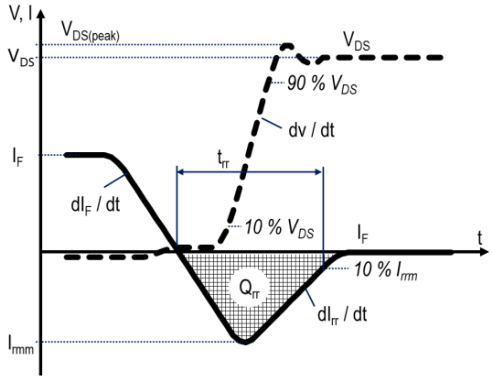
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times (ss)

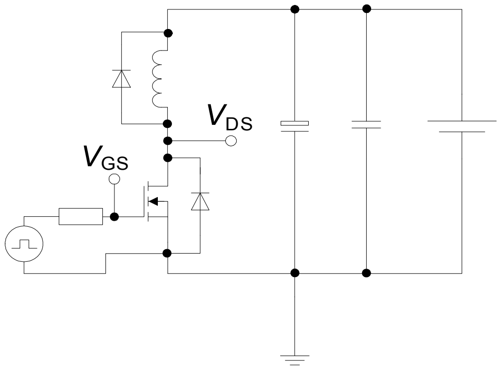
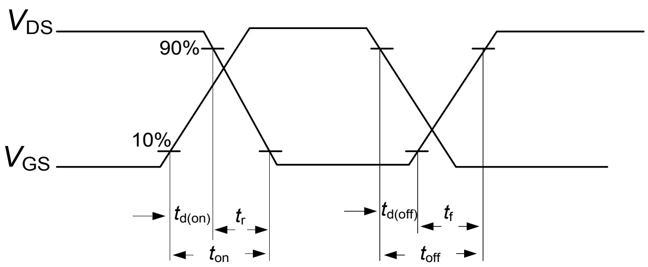
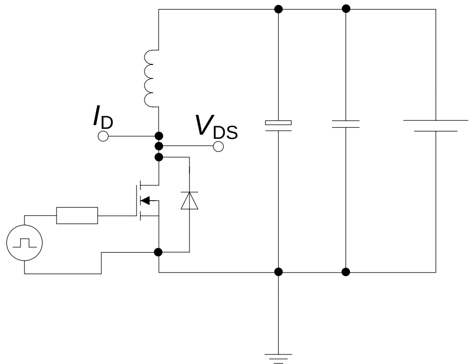
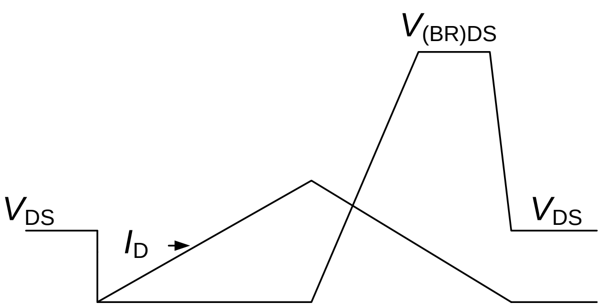
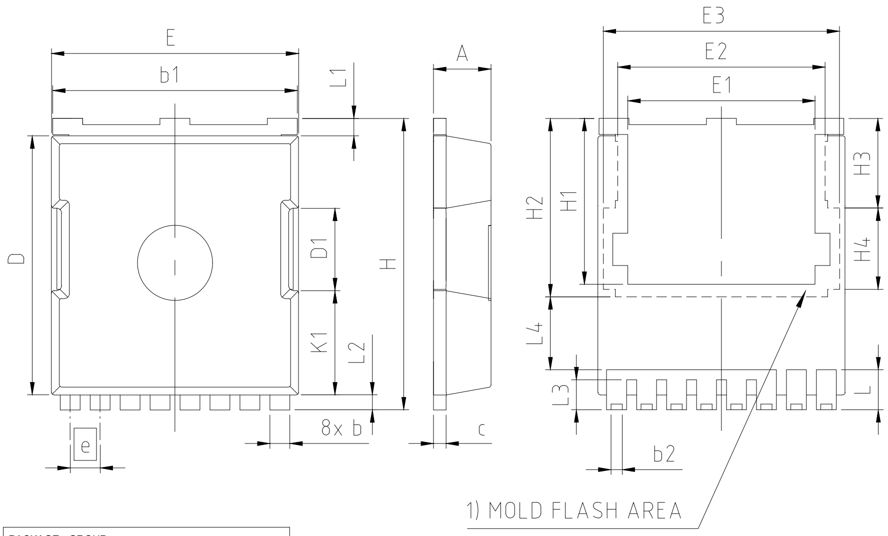
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package outlines



PACKAGE - GROUP NUMBER:	PG-HSOF-8-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	
H3	3.59	
H4	3.26	
N	8	
K1	4.18	
L	1.40	1.80
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	2.62	2.81

1) PARTIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

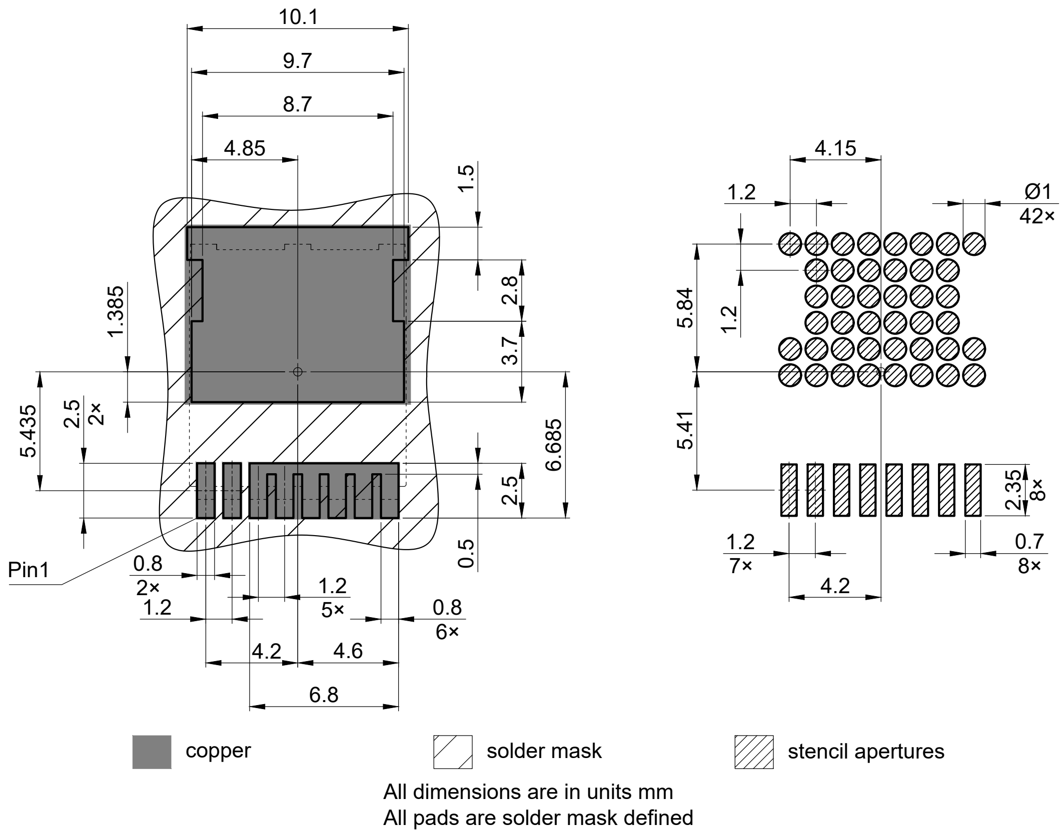
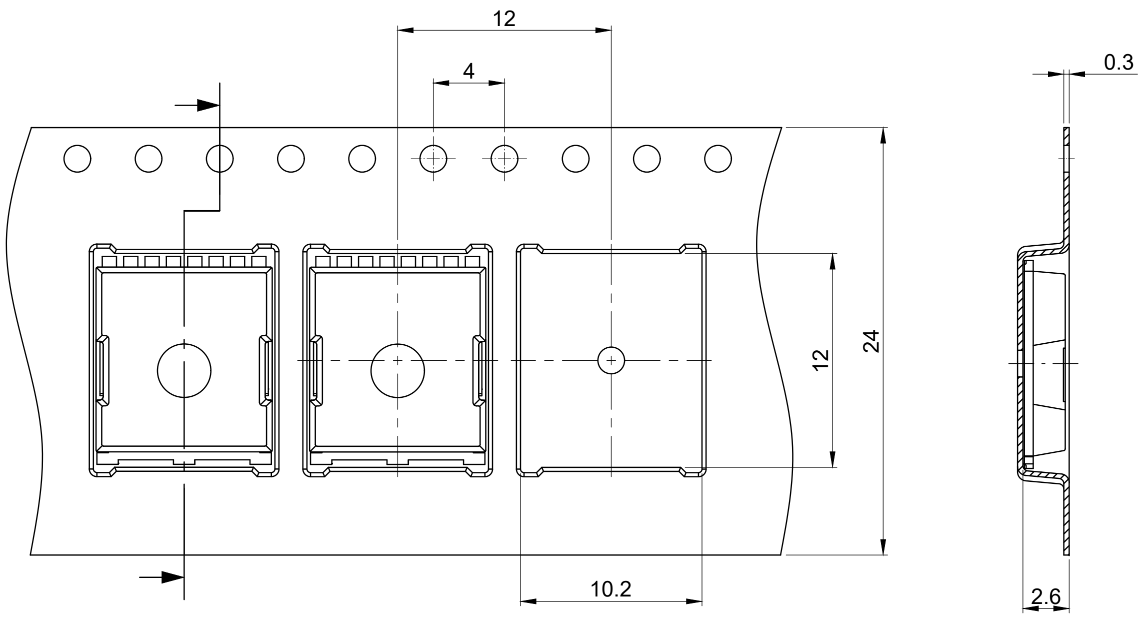


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

7 Appendix A

Table 11 Related links

- IFX CoolMOS™ CFD7 Webpage
- IFX CoolMOS™ CFD7 application note
- IFX CoolMOS™ CFD7 simulation model
- IFX Design tools

Revision history

IPT60R125CFD7

Revision 2025-02-03, Rev. 2.4

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2020-04-22	Release of final version
2.1	2020-06-23	Changed diode commutation speed current
2.2	2020-08-28	Changed trr and Qrr value
2.3	2020-10-22	Changed diagram 2, 3, 7, 8, 9; Changed typical static and dynamic parameters
2.4	2025-02-03	Implementation of standardized Infineon Umbrella-Templates for package drawings. H1 Extension from 6.75 to 6.95 MAX

Trademarks

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Published by
Infineon Technologies AG
81726 München, Germany

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